Simulation and instrumentation for the Roman Pot in the future Electron-Ion Collider

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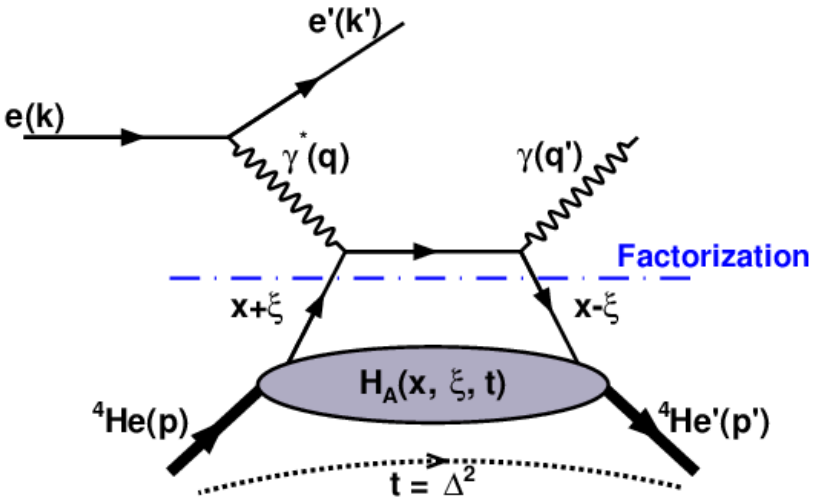
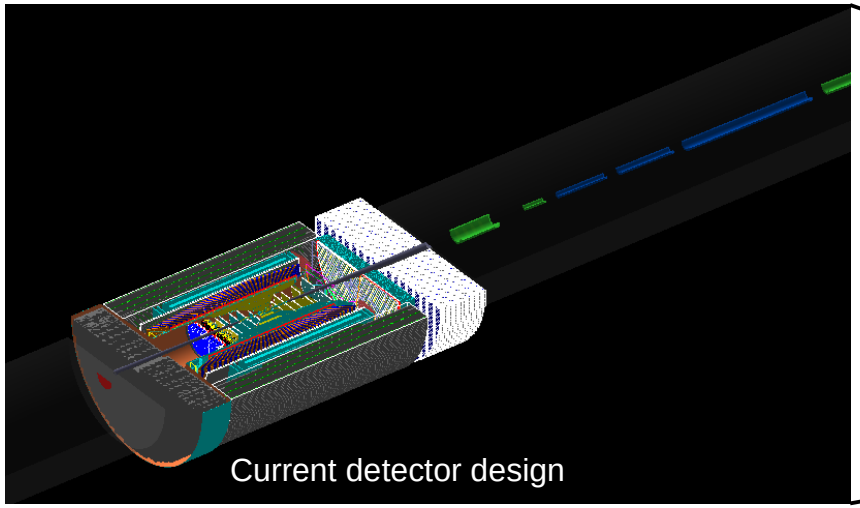
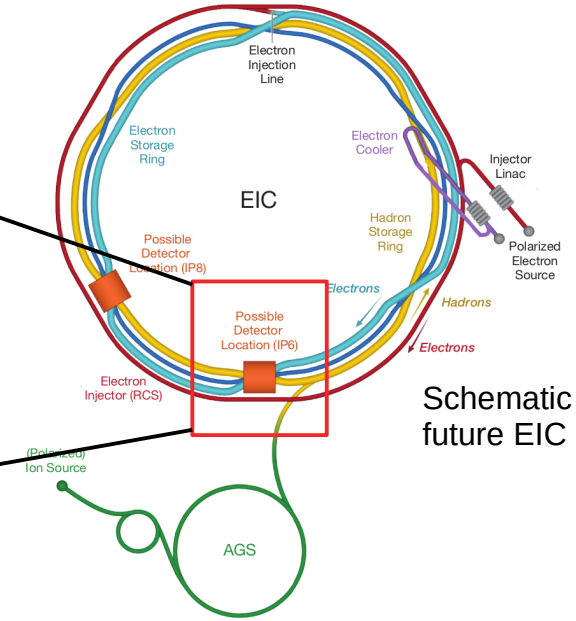
Exclusive process in future EIC

- The Generalized Parton Distribution (GPD) framework is a recent approach to understand the nucleon structure in further detail. It can also be used to study the spin structure of the proton.
- Deep Virtual Compton Scattering (DVCS) is a exclusive process that can provide access to the GPDs of the proton
  $e^- + p \rightarrow e^- + \gamma + p$
- A new electron ring will be added to Relativistic Heavy Ion Collider (RHIC) and the requirements:
  - highly polarized e- beam(~70%) and proton beam(~70%)
  - ion beam from deuteron to gold, lead or uranium
  - high luminosity: 10^{33}~10^{34} $cm^{-2}s^{-1}$
  - e^-+proton center of mass energy up to 140 GeV




Current detector design

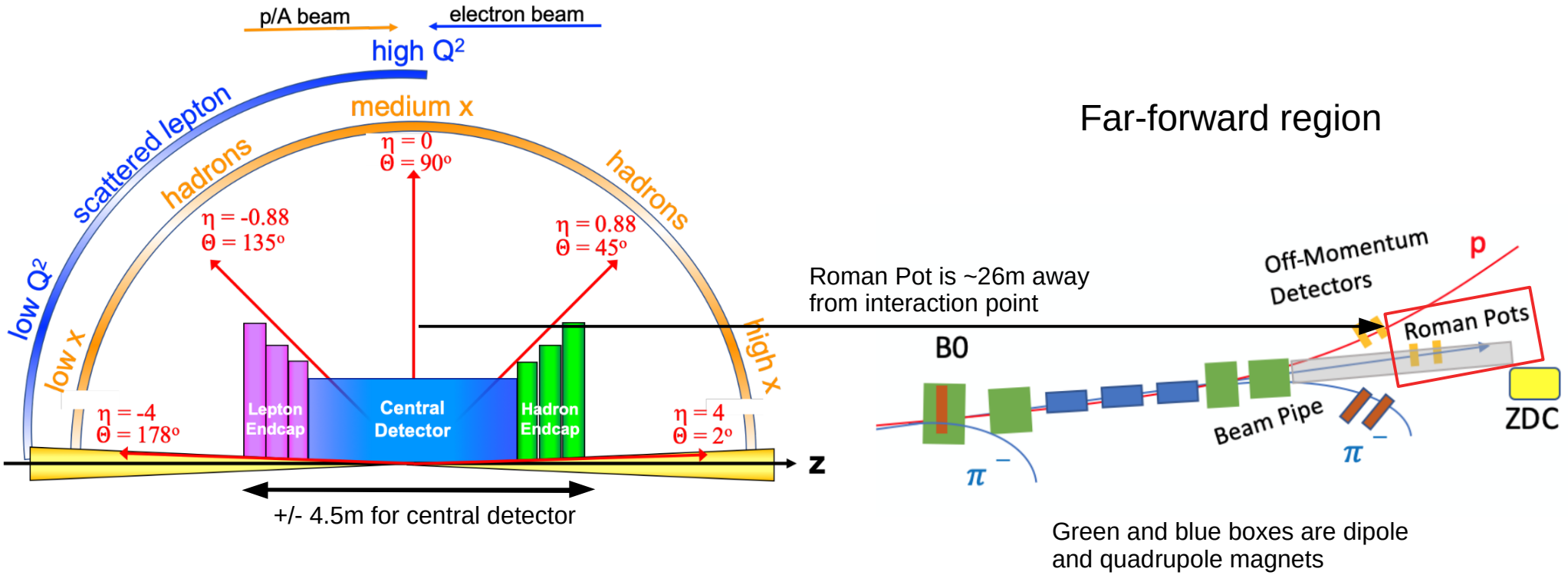
The first data taking will be in 2030



Schematic view of future EIC at BNL

Exclusive process in future EIC

- In the DVCS process, $e^- + p \rightarrow e^- + \gamma + p$
  - most scattered e- and photons go to the lepton Endcap and some toward the barrel detector.
  - The recoil protons go to the far-forward region and will be detected by the Roman Pots



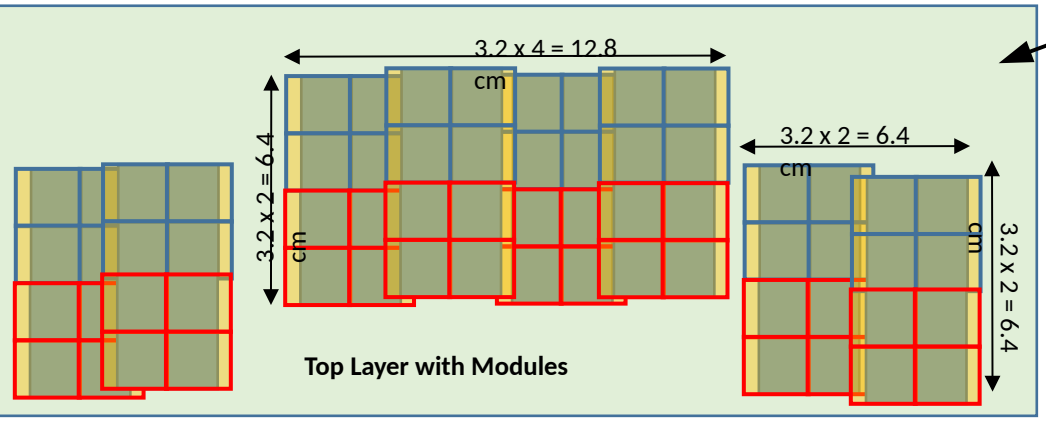
Green and blue boxes are dipole and quadrupole magnets

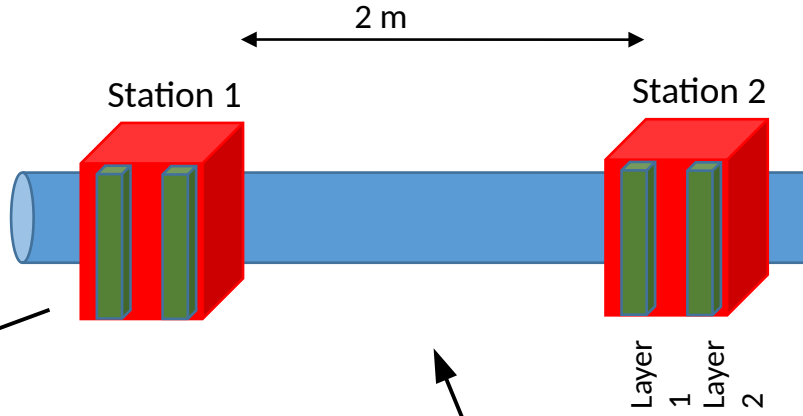
Roman Pots in EIC

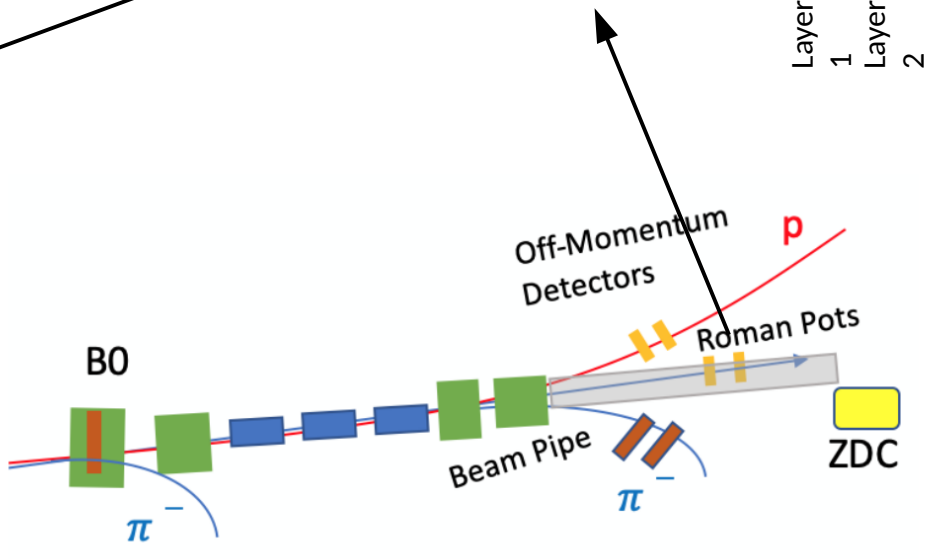
- 2 stations and 4 layers silicon detector to detect the recoiled DVCS proton/ion
- Use AC-LGAD to perform the precised 4D measurements and high speed readout
- Use 1TDC(Time Digital Converter) + 1ADC(Analog Digital Converter)
- Around 0.5 million channels in total are required

station	(0.85, 26) (0.94, 28)
dimension	(25cm, 10cm, n/a)
theta	0. < θ < 5.5 mrad

position resolution requirement	timing resolution requirement	N channels per ASIC	Sensor size	power consumption (W/cm^2)
100μm	30-40ns	1024	500 μm	1.07



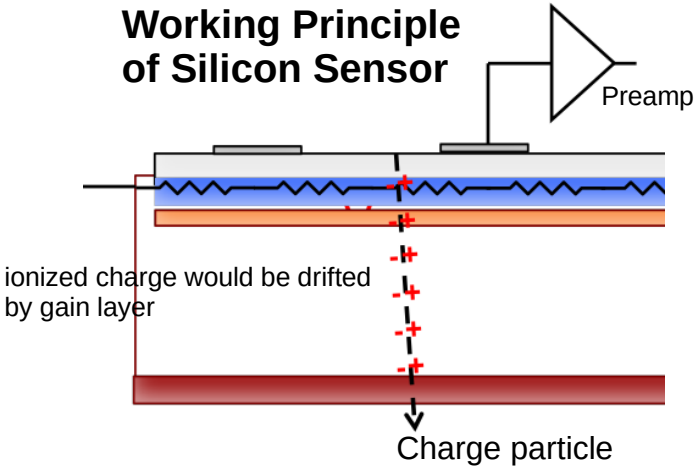


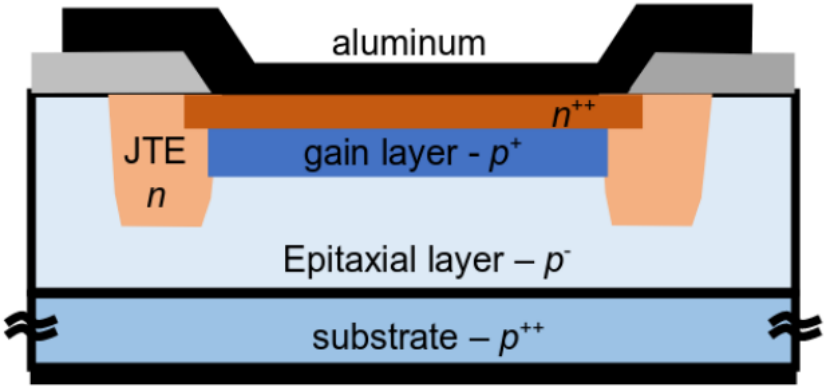


AC Low Gain Avalanche Diode

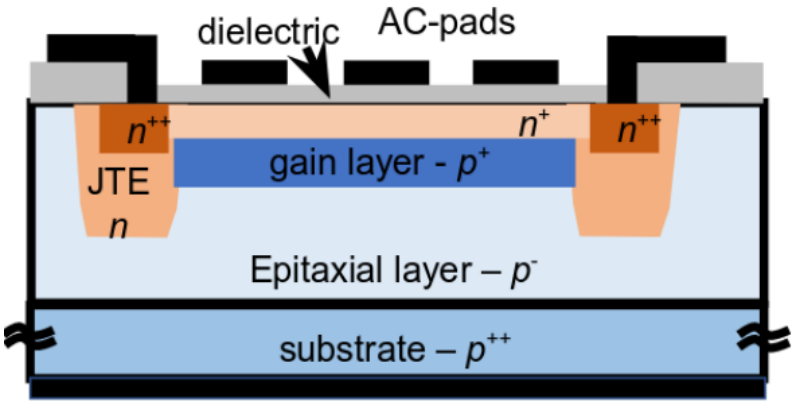
- AC-LGAD is adapted from LGAD, which is used in HGTD in ATLAS
- AC-LGAD features:
  - AC couple signal
  - 100% fill factor(no dead region)
  - fast timing information as LGAD
  - signal sharing between nearby pads to improve position resolution (Barycenter)

} -> 4D measurements





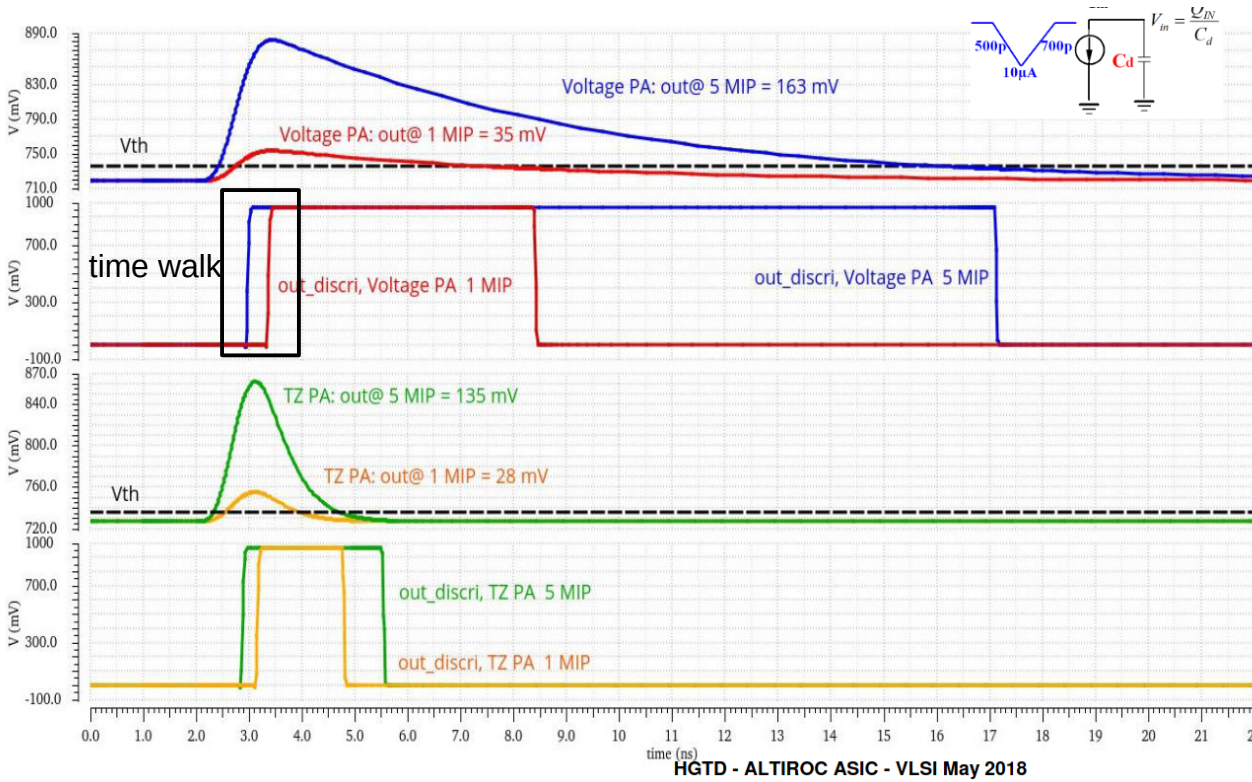
The schematic DC-LGAD



The schematic AC-LGAD

Readout chip of AC-LGAD

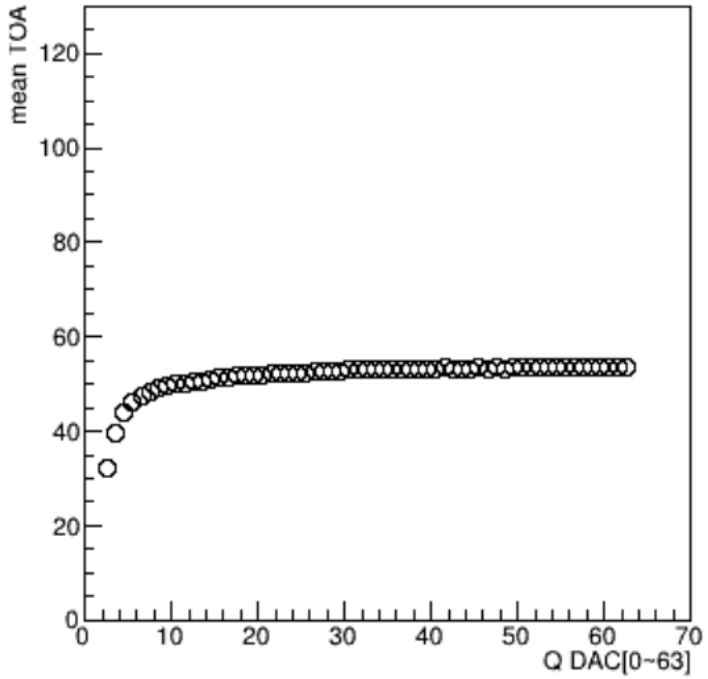
- Now, we use well developed **ALTIROC** to study the property of AC-LGAD , which use **2 TDCs** to measure signal
  - TOA (Time of Arrival)
  - TOT (Time over threshold)
- 2 different types of pre-amplifiers are implemented in the ASIC:
  - TZ (Transimpedance preamp), better in TOT measurements
  - VPA (Voltage preamp)
- Future **EICROC** will use **1TDC+1ADC**, since ADC can perform more precise charge measurements
- The first version of **EICROC** would be available in Sept.



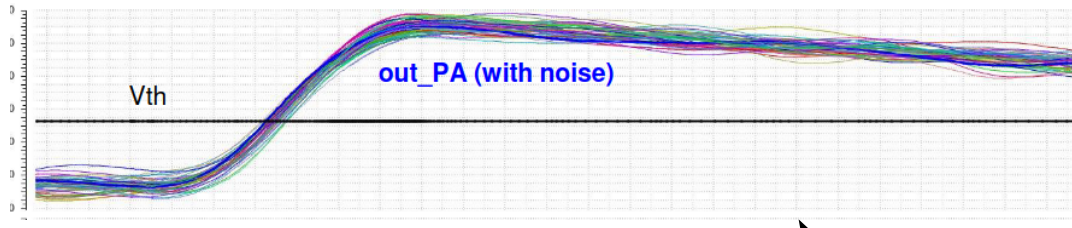
HGTD - ALTIROC ASIC - VLSI May 2018

TDC performance study

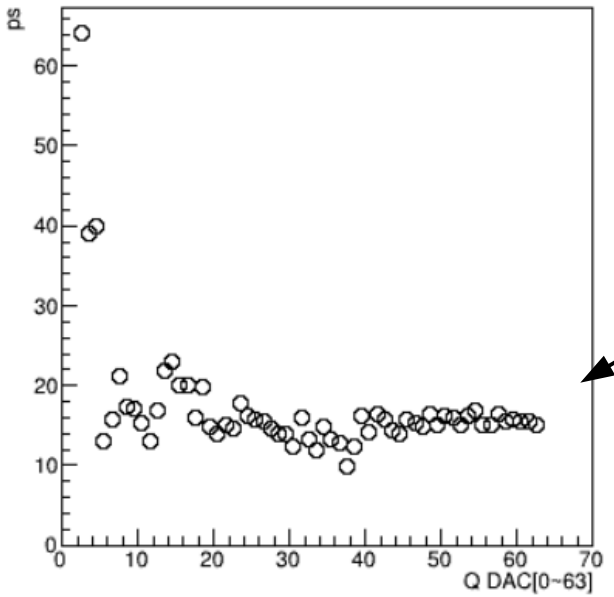
- time resolution electronic: TDC resolution + jitter + time walk
- Jitter: the noise is summed to the signal, causing amplitude variations
- Time walk: under given threshold, different scale of signal would have different time of arrival



Time walk effect under different charge



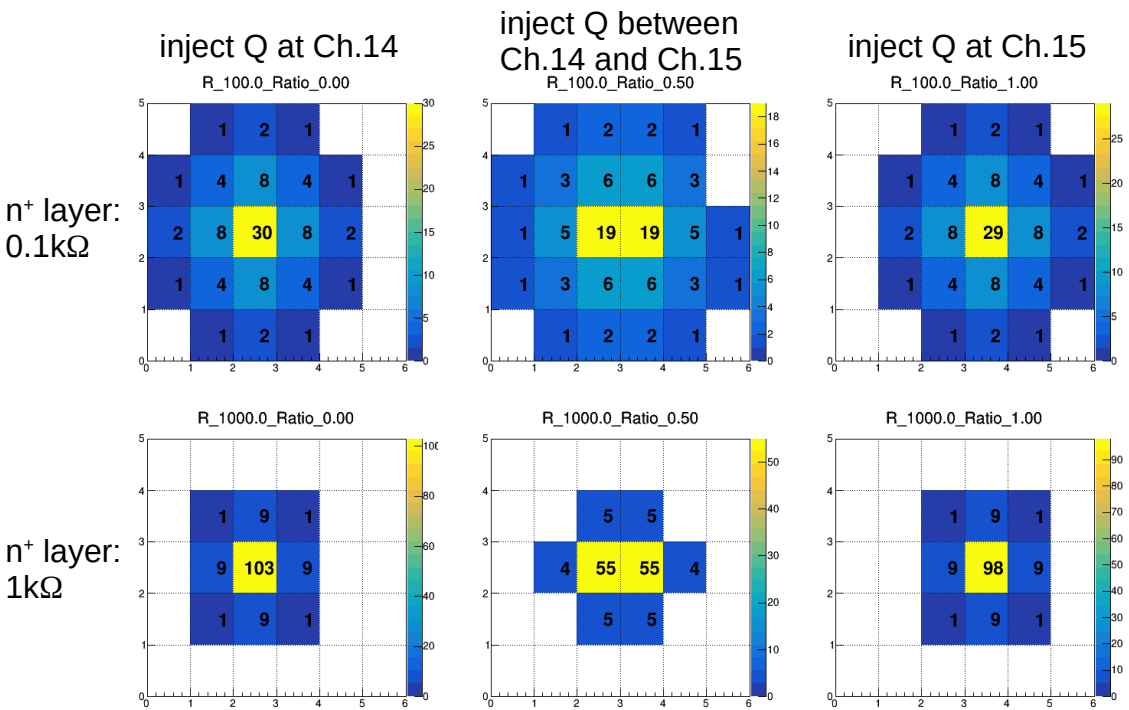
amplitude variation caused by jitter

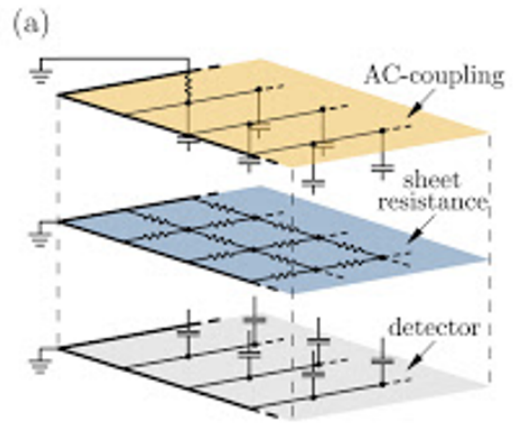


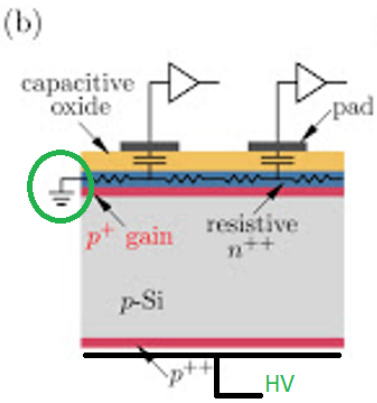
jitter under different charge

AC-LGAD simulation study

- The purpose is to know the optimal ADC resolution(8, 10, 12 bit) for the AC-LGAD readout
- Simulate different resistivity value of n^+ layer, from 0.1k - 10k Ω
- Simulate different inject charge -> saturation happen as limited dynamic range
- Simulate different inject position between two given channels, then using barycenter to reconstruct the inject position and calculate the position resolution.



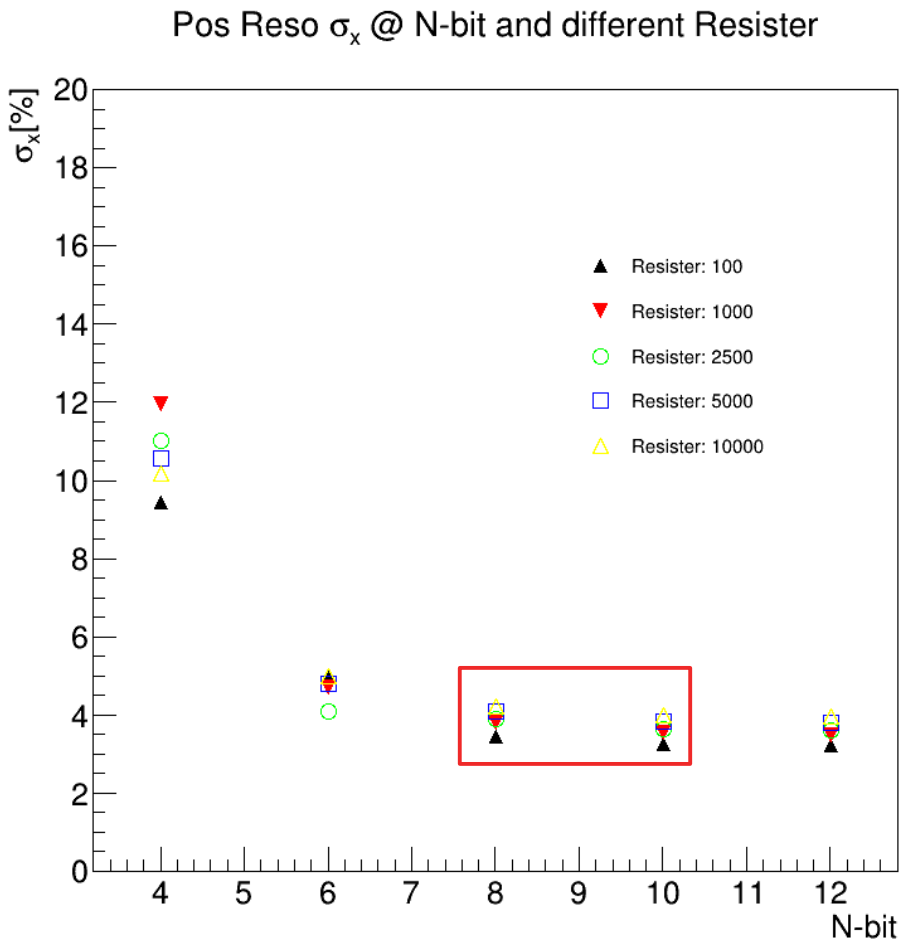




Simulation model of AC-LGAD sensor from our OMEGA

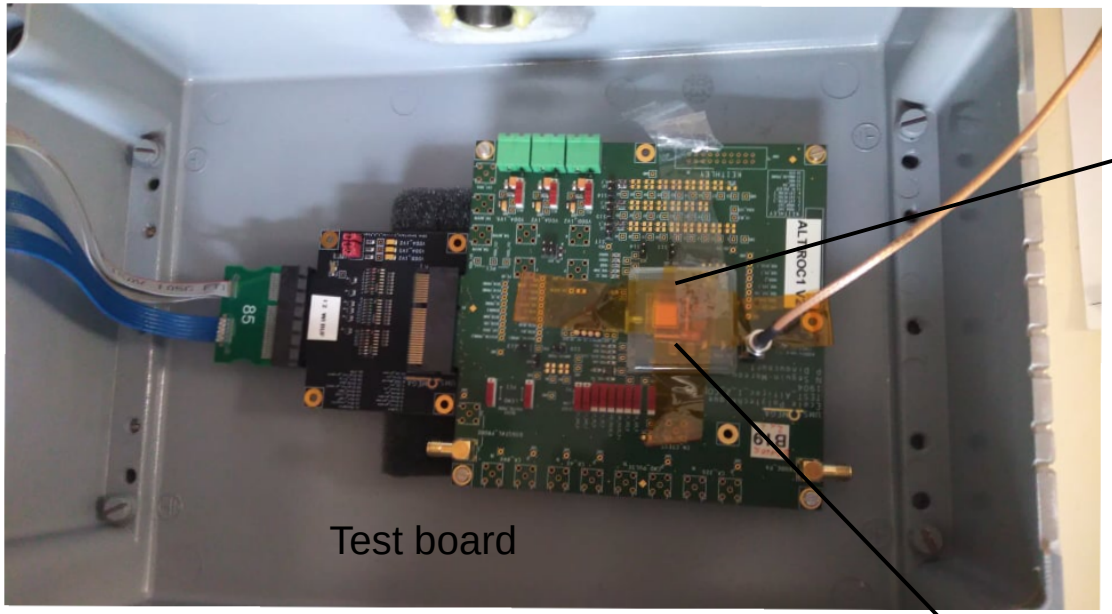
Simulation of signal sharing among neighboring pixels

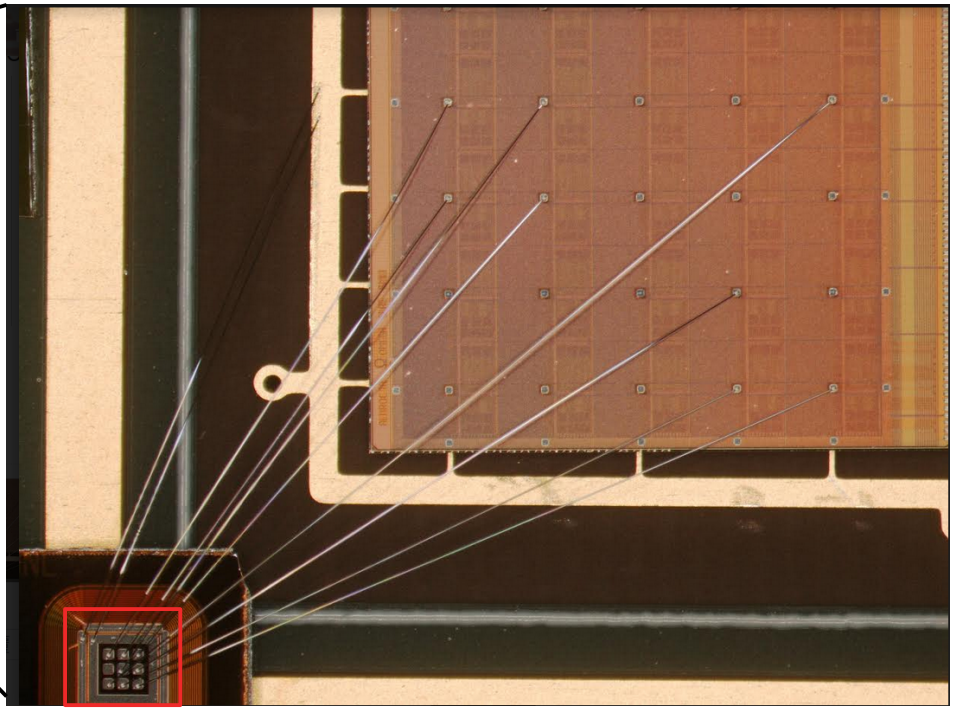
- Smear the charge deposition with landau distribution
- Implement the ADC algorithm, noise, threshold...etc
- We can reconstruct the injected position within 4% of the pixel size



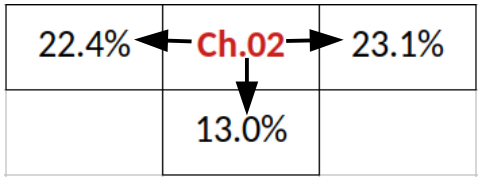
No significant σ_x difference between ADC-8 & 10 bit
And Due to the low power consumption and small size, **ADC-8bit is chosen**

Sharing determination of AC-LGAD by charge injection



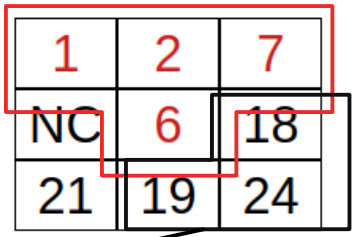


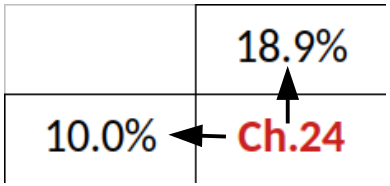
AC-LGAD wire bond to ASIC



Sharing of charge injection

inject 8pF @ ch.02

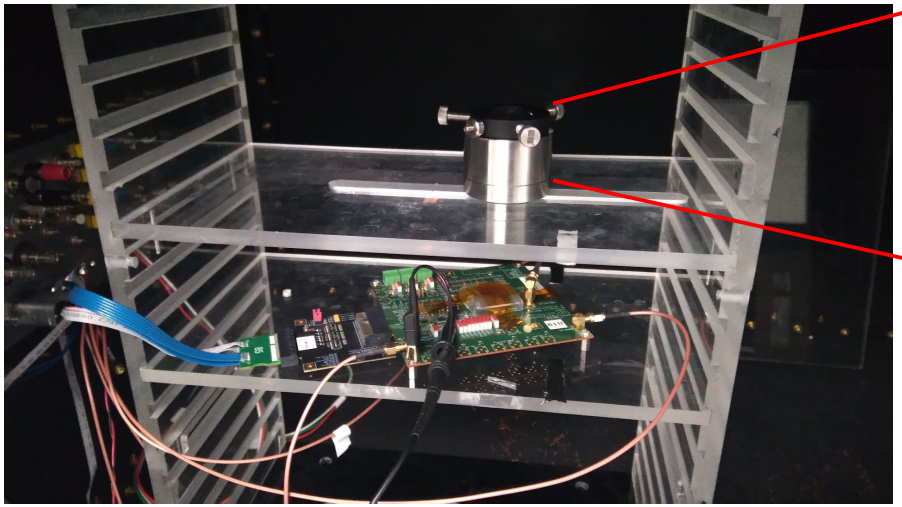


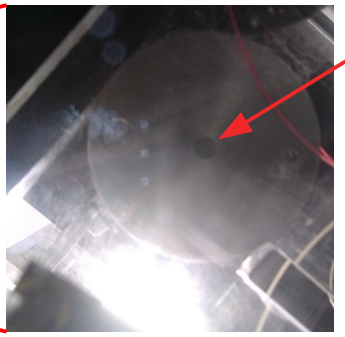


inject 8pF @ ch.24

Quantify the sharing by charge injection

Sharing determination of AC-LGAD by beta source

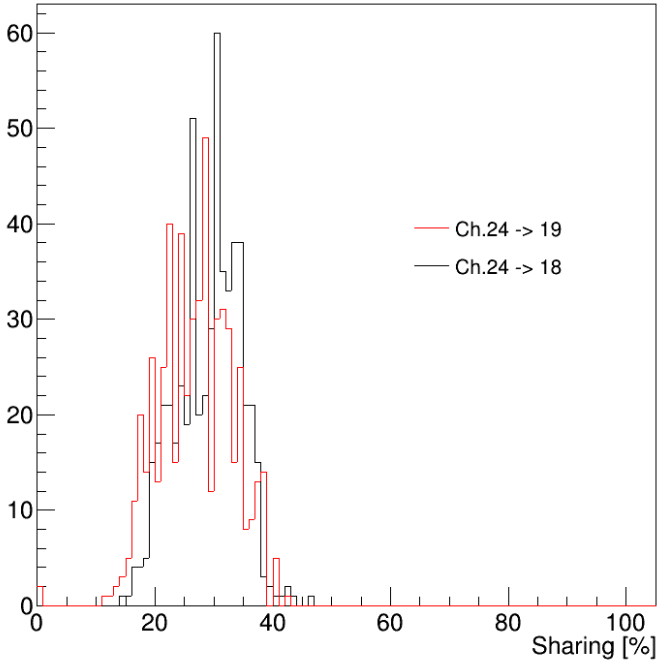




Beam hole for Sr-90 [37MBq]

- The Beta source is placed right above sensor, 5~10 cm away.
- High voltage is -170V
- The whole setup put in black box

Sharing from Ch.24 to 18, 19



1	2	7
NC	6	18
21	19	24

24 share to 18 and 19
$TOT_{24} > TOT_{18}$ and $TOT_{24} > TOT_{19}$

- From the beta source measurement, we can get ~30% of sharing
- The discrepancy in inject charge and beta source measurements comes from the TDC distortion

Summary

- EICROC design and the test are in the progress
- The ADC-8bit will be adapted based on the chip position resolution study
- The sharing of AC-LGAD is determined by both charge injection(~15%) and beta source(~30%).

Outlook:

- Using laser the quantify the sharing of AC-LGAD sensors. Laser can offer desired charge injection and position