Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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Abstract.
The ATLAS Liquid Argon Calorimeter readout electronics will be upgraded to withstand higher radiation doses and harsher conditions during the HL-LHC. In this context, the upgraded readout chain will include front-end, calibration, processing, and timing control boards. The front-end boards will amplify and digitize the ionization signal with high precision and low noise. Custom made chips for amplifying, shaping and digitize the calorimeter signals have been developed, demonstrating stability under irradiation tests. Calibration boards will ensure precise calibration across all channels by using custom ASICs which will be also stable under irradiation. The digitized signal will be processed for energy estimation and time stamping purposes by using boards featuring FPGAs connected via high-speed links. To enhance their functionality, we are exploring using artificial neural networks within the FPGAs. Lastly, the timing and control system will ensure the synchronization across the different boards. The current status of the prototype boards and testing efforts are presented.

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1 Introduction

A new era of hadron collisions will start around 2029 with the High-Luminosity LHC (HL-LHC), enabling ten times more data collection than what has been collected during the 10 years of operation at LHC. The HL-LHC is set to achieve an integrated luminosity of 4000 fb^{-1}, resulting in a significantly higher pile-up, reaching up to 5-7 times the nominal LHC luminosity of $1 \times 10^{34} cm^{-2} s^{-1}$. This increased rate would yield up to 200 proton-proton collisions per bunch crossing.

As part of the ATLAS experiment [1], the Liquid Argon (LAr) calorimeter serves as a sampling calorimeter to accurately measure the energy deposited by electrons, photons, and hadronic jets [2]. The active medium of the calorimeter is liquid argon. The calorimeter covers the pseudo-rapidity range of $|\eta| > 4.9$, and has approximately 182,500 readout channels, enabling detailed energy reconstruction and particle identification. The upgrades on the LAr calorimeter electronics are meant to withstand the high radiation doses, accommodate the triggering requirements, and efficiently process the data in the HL-LHC conditions.

Figure 1 presents a detailed block diagram illustrating the architecture of the LAr calorimeter readout system after the upgrades. The Phase-I upgrades of the LAr calorimeter

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readout system [3], shown in the bottom part including LTDB and LDPS boards, was focused on enhancing trigger digitization and processing and it is currently in operation in ATLAS. This document focuses on Phase-II [4], which covers upgrades related to calibration, signal amplification and digitization, as well as processing data for energy reconstruction.

The following sections provide descriptions of the corresponding boards involved in these upgrades. The system is divided into on-detector and off-detector electronics to distinguish the boards that are exposed to radiation from those that will be installed away from the beam.

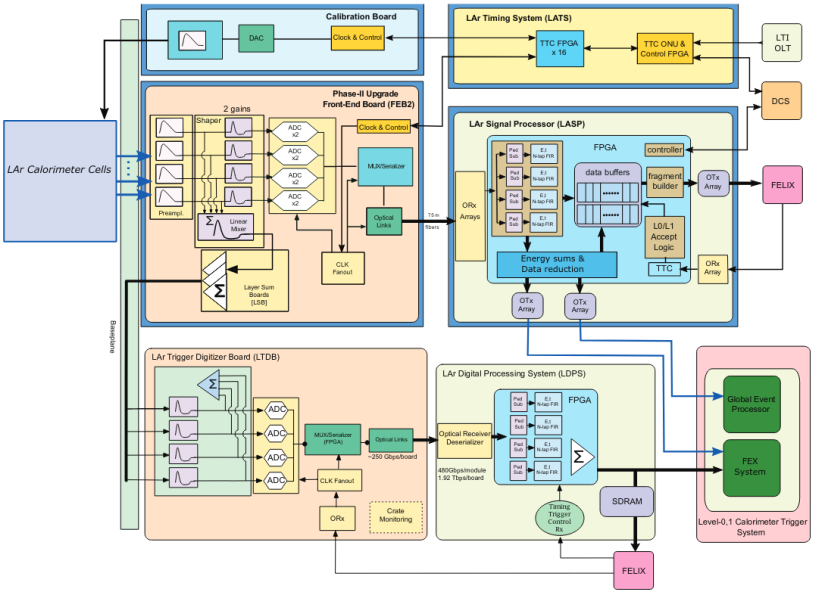

Figure 1. LAr calorimeter readout upgrades for HL-LHC era. Calibration, Front-End and Signal Processing boards are under development for the Phase-II upgrades covered in this document.

2 On-detector electronics

The components described in this section are the calibration and front-end boards, with a common requirement of maintaining stable operation under a maximum irradiation of 4.1×10^{13} n_{eq}/cm^2 (NIEL). This has led to the design, fabrication and testing of custom made chips for amplifying and digitizing signals, as well as for generating a pulse for readout calibration purposes.

2.1 Front-end boards

The purpose of the Front-End board v2 (FEB2) is to amplify and digitize signals for both trigger and energy reconstruction. The board has being designed to effectively manage the 16-bit dynamic range of calorimeters operating at 40 MHz, accommodating two gain scales. The digitized data is serialized and transmitted to the processing boards boards via the high speed and radiation hard lpGBT (Low Power Gigabit Transceiver) protocol developed at CERN [5]. Each board will digitize 128 channels for a total of 1524 boards required for the Phase-II upgrades. A Layer Sum Board (LSB) is connected to the FEB2 and will provide analog trigger sums for trigger digitization and processing.

The FEB2 will feature two custom made ASICs, the pre-amplifier and shaper ALFE2 and the COLUTA V4 ADC [6]. The **ALFE** chip is fabricated in 130 nm CMOS technology with a 16-bit analog dynamic range. It performs a CR-RC^2 pulse shaping to transform the triangular ionization signal from the calorimeter into a bipolar pulse in two gain scales with a gain ratio ~ 23.

The ALFE v2, the most recent version of the chip, has met the specifications. Measurements, including Integral Non-Linearity (INL) of under 0.2%, and Equivalent Noise Current (ENI) of less than 2 uA, among other fulfilled requirements have allowed it to pass the Final Design Review (FDR) in November 2022.

Signals in the FEB2 will be digitized by the **COLUTA** chip, which is an 8-channel, 15-bit, 40-MHz ADC fabricated in 65 nm CMOS technology following an MDAC-SAR architecture. Two of the key specifications are the Effective Number Of Bits (ENOB) to be above 11 and a non-linearity below 0.1%, which have been recently achieved along with other specifications, demonstrating the chip readiness for the next phase during the FDR held in October 2022.

Both ASICs are currently in pre-production stage after extensive testing campaigns that included irradiation testing. To ensure consistent and reliable performance across a large batch of chips, dedicated testbenches are under developing for mass production testing. Furthermore, a 32-channel testboard that integrates the ALFE v2, COLUTA v4, and lpGBTs has been designed, fabricated and validated, meeting specifications for energy resolution (~0.02%), and time resolution (~50 ps) when LAr pulses are injected. The successful integration efforts have lead to the design of the first FEB2 prototype boards which are currently under fabrication process.

2.2 Calibration

Two custom ASIC chips, namely CLAROC and LADOC, will be used in the calibration board to inject physics-like pulses for read-out electronics calibration. **CLAROC**, fabricated on HV SOI CMOS XFAB 180nm technology, serves as a high-frequency switch, generating pulses that closely resemble the output of the LAr detector. The **LADOC** chip, fabricated using TSMC 130 nm technology, controls the current and a digital-to-analog converter (DAC) to produce a precise pulse height for calibration. Both chips must be stable under same levels of irradiation as the FEB2 chips.

The latest iterations of the ASICs, the CLAROC v4 and LADOC v2, have successfully met specifications concerning linearity. Notably, the LADOC v2 surpasses specifications by a factor ranging from 2 to 10 times, when driving up to 40 mA, demonstrating exceptional performance. Similarly, the CLAROC v4 achieves a factor up to 10 times better than specifications for linearity, when working on a range of up to 320 mA. Currently, these chips are undergoing irradiation testing while the initial version of the calibration board design is in progress.

3 Off-detector electronics

The off-detector electronics consist of the processing and the timing systems, which are designed to ensure efficient signal processing, data handling, and precise timing synchronization.

3.1 Processing system

The off-detector electronics will process signals from the front-end boards and will be responsible for computing signal energy and time stamping. In the context of the Phase-II upgrades,

a dedicated off-detector electronics system known as the LAr Signal Processor (LASP) has been developed. The LASP consists of an Advanced Telecommunications Computing Architecture (ATCA) blade equipped with two Field-Programmable Gate Arrays (FPGAs) and a Smart Rear Transition Module (SRTM).

The development of FPGA's firmware for the LASP is currently in progress, ensuring the system's readiness for deployment. The firmware is designed to accomplish multiple tasks, which are summarized as follows: first, the digitized waveforms from the FEB boards are received. Once the waveforms are received, digital filtering techniques are applied to compute the energy for each bunch crossing. The values are then transmitted to the trigger system. In parallel, the data are buffered until a trigger decision is received. Finally, the firmware will ensure the reliable transmission of data to the DAQ and trigger systems. Currently, several demonstrators of the LASP board are undergoing testing, which includes the described firmware.

3.1.1 RNNs on LASP

With the increased demands of the Phase-II Upgrade, the off-detector electronics will receive an enormous amount of data. In total, the system will handle 345 Tbps of data transmitted via 33,000 links, each operating at a speed of 10 Gbps. To cope with the challenges posed by the expected increase in pile-up, artificial neural networks (ANNs) are being explored to be implemented in the FPGAs. These algorithms aim to mitigate the impact of pile-up on energy reconstruction processes.The initial investigations in this field have demonstrated the superior performance of neural networks over current energy and timing computation methods [7]. Specifically, they have shown promising results in accurately assigning reconstructed energy to a proton bunch crossing and improving energy resolution.

Building upon these findings, a recurrent neural network (RNN) was implemented on a demonstrator FPGA board, which paves the way for a comprehensive evaluation of the neural networks algorithms' effectiveness across various levels of abstraction, ranging from high-level software representation to low-level hardware description languages tailored for FPGAs [8]. This approach allowed for the development of a workflow that accommodates the complexity of the RNN algorithms while utilizing the available FPGA resources, achieving the requirements by reconstructing 384 channels per FPGA with a latency smaller than 125 ns. These efforts have successfully showcased the feasibility of implementing ANNs on FPGAs for the LAr Phase-II upgrades.

3.2 Timing system

The Off-Detector Electronics also include the LAr Timing System (LATS), which plays an important role in providing trigger, timing, and control (TTC) functionality to the on-detector boards using the lpGBT protocol.

Currently, the development of the LATournett boards is underway for the implementation of the LATS. This board includes a central control FPGA and 12 matrix FPGAs responsible for communication with the FEB2. These components allow efficient data transfer and synchronization.

To validate the functionality of the firmware, testing has been conducted using the Cyclone10 DevKit. This verification process ensures that the firmware operates as intended and meets the required specifications. Additionally, the power-up sequence has been successfully verified using the POWERv2 board, ensuring reliable and consistent operation. Also, in order to test the communication between the Cyclone10 FPGA and the lpGBT, the LpGBTv0 FMC board has been developed.

An important milestone in the LATS development is the fabrication of the first LATournett PCB, which is scheduled to take place this year.

4 Conclusions

The Phase-II upgrades for the LAr detector are addressing several challenges imposed by the HL-LHC conditions. Key advancements have been achieved, for example, in the development of radiation-tolerant custom-made ASICs for on-detector electronics, which have undergone rigorous testing campaigns to ensure their reliability and robustness. Furthermore, significant progress has been made in integrating these ASICs and other essential components into test boards for comprehensive performance evaluations and to facilitate firmware and software development. The imminent fabrication of the first versions of the FEB2, calibration and LATs boards, represent a significant progress in the development of hardware components.

Regarding the improvement in processing capabilities and the fulfillment of trigger goals, the progress on firmware development, testboard development and the integration of ANN algorithms on FPGAs for the LASP boards will enable more efficient and accurate data analysis. By leveraging ANN algorithms and models, the LASP FPGAs will be empowered to effectively estimate signal energy and accurately timestamp events, contributing to enhanced event reconstruction and overall performance of the system.

In summary, these collective efforts and progress across various aspects of the project demonstrates that the Phase-II upgrades are well on track for their targeted deployment during the LS3.

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