Taming the Menagerie

Benefits of Microarchitecture levels in disturbed clusters

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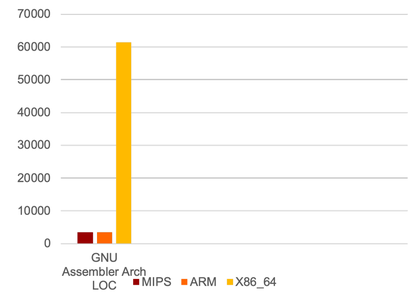
CPU Architecture Complexity

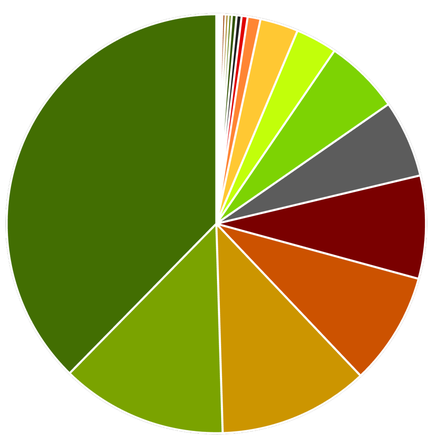


Year	Name	Family	Description
2011	SMX	Nehalem	Safer Mode Extensions;
2011	AES	Westmere	AES operations
2012	TBM	Piledriver	Trailing Bit Manipulation
2013	BMI1	Jaguar	Bit Manipulation Instruction1
2013	BMI2	Haswell	Bit Manipulation Instruction2
2013	FMA3	Haswell	3-operands fused mac
2013	TSX	Haswell	Transactional Extensions;
2013	AVX2	Haswell	Advanced Vector Extensions;
2014	ADX	Broadwell	Multi-Precision Add-Carry
2014	RdRand	Broadwell	Secure Key Technology

http://wikichips.org

Year	Name	Family	Description
2014	PREFETCH	Broadwell	PREFETCH
2015	AVX-512	Airmont	512 bit reg
2015	MPX	Skylake	Memory Protection
2015	SGX	Skylake	Software Guard
2016	SHA	Goldmont	SHA Extensions
2017	SME	Zen	Secure Memory Extensions
2019	TME	Ice Lake	Total Memory Encryption

CPUs in OSPool by Model



OSPool

Problems with Hetereogenous CPUs

-- Programs crash with SIGILL
very hard to debug
-- Some machines too slow to be useful
hard to describe
-- Unclear which compiler options to use

Solution: MicroArchitecture

Microarchitecture
- learn it
- use it
- teach it

Effort lead by RedHat and Intel to distill all the variant down to four hierarchical groups:

(Can be used in both gcc and LLVM)

x86_64-v1, x86_64-v2, x86_64-v3, x86_64-v4

- SSE2
- SSE4
- POPCNT
- …
- AVX
- AVX2
- FMA
- BMI
- F16C
- AVX512

HTCondor and Open Science Grid

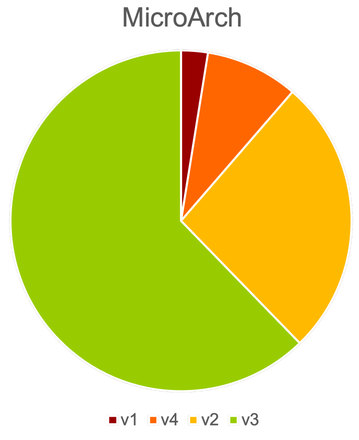
HTCondor in OSG detects and advertises the microarch

Allow for matching (requirements and rank) on microarch

Allows for *talking* about architecture in a meaningful way

HTCondor Software Suite

MicroArch in OSPool



Future work

› Would like 3rd party binaries to identify their required microach automatically

› Need to detect microarch of binary programmatically

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