Validation of the new hardware trigger processor at NA62 experiment

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and

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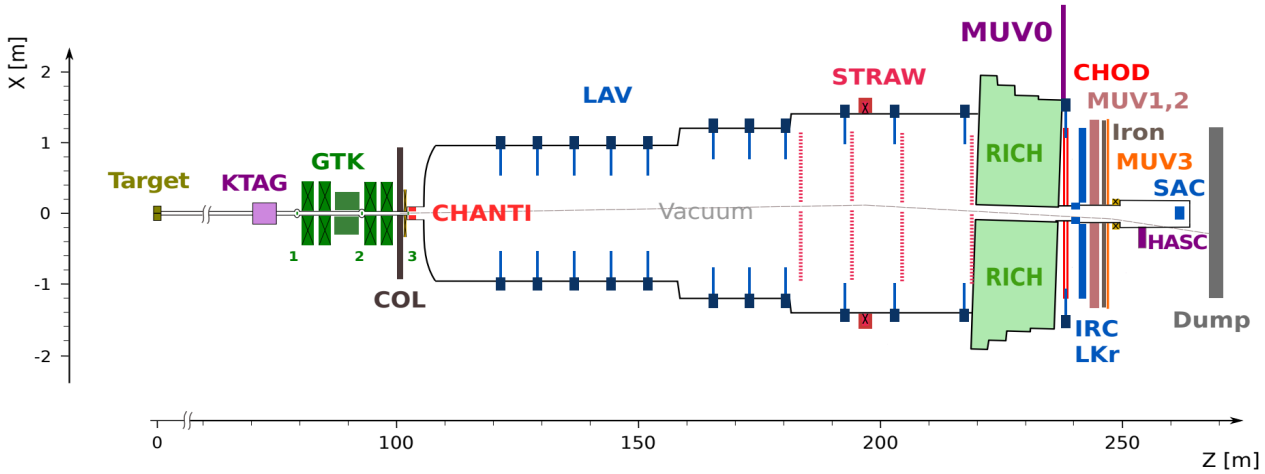
CHEP 2023
Norfolk – 11th May 2023

NA62



NA62 Experiment

- Fixed target experiment located in the North Area of CERN dedicated to the study of charged kaon decays.
- Measurement of $BR(K^+ \to \pi^+ \nu\bar{\nu})$, through decay-in-flight tecnique.
- Last result (from 2016-2018 data) at 68% CL

$$BR(K^+ \to \pi^+ \nu\bar{\nu}) = (10.6^{+4.0}_{-3.4}|_{stat} \pm 0.9_{syst}) \times 10^{-11}$$

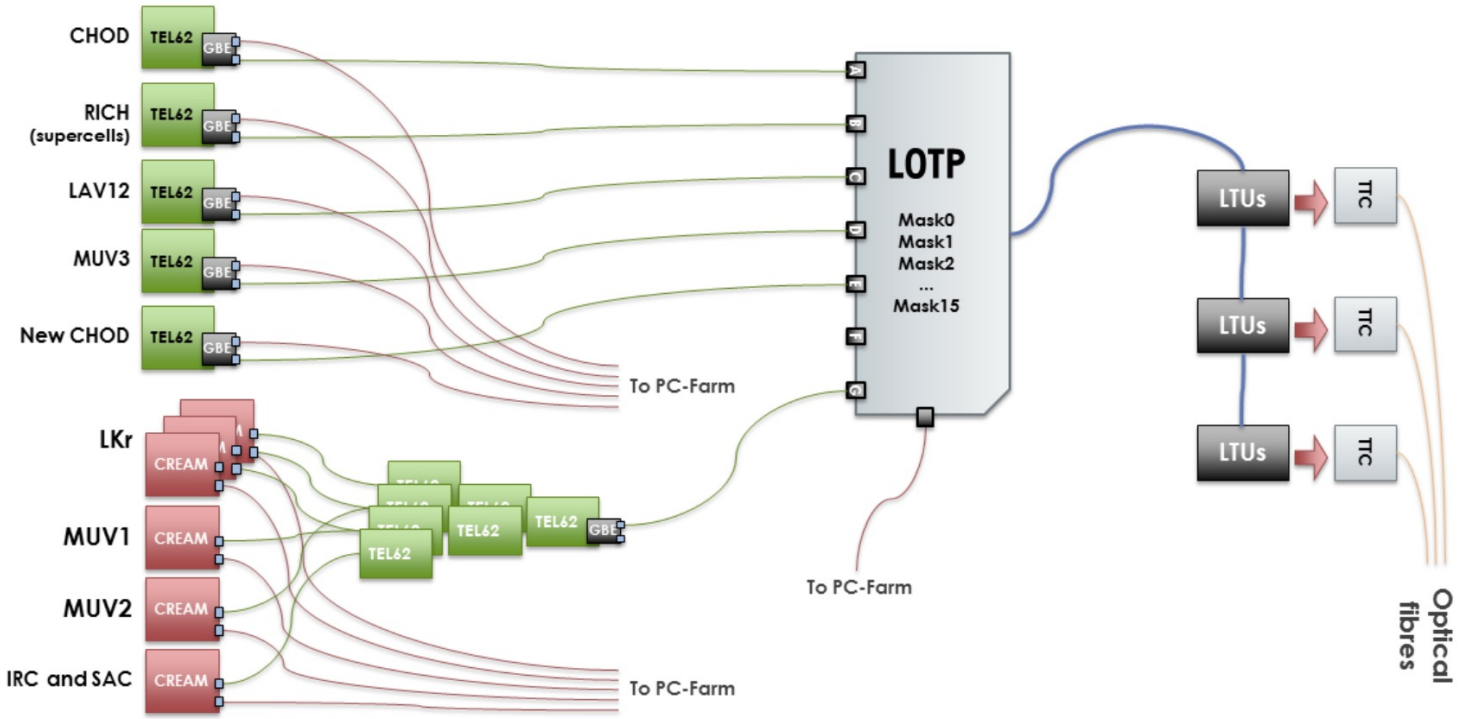
- Nominal beam rate: **750 MHz**
  - ➔ K^+ rate: 45 MHz
  - ➔ ~5 MHz K^+ decays in fiducial volume

Multi-level trigger

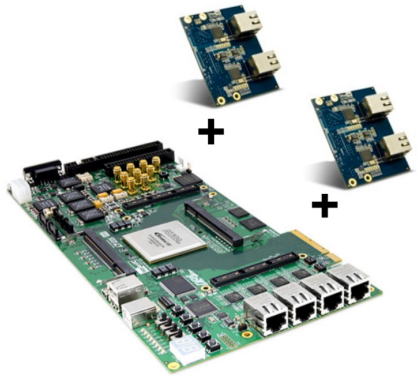
- Level-0 **(L0TP,** Level 0 Trigger Processor) HW trigger on FPGA (input 10 MHz-> output 1MHz)
- Level-1/2 software trigger running in DAQ farm (1MHz –> 100kHz)

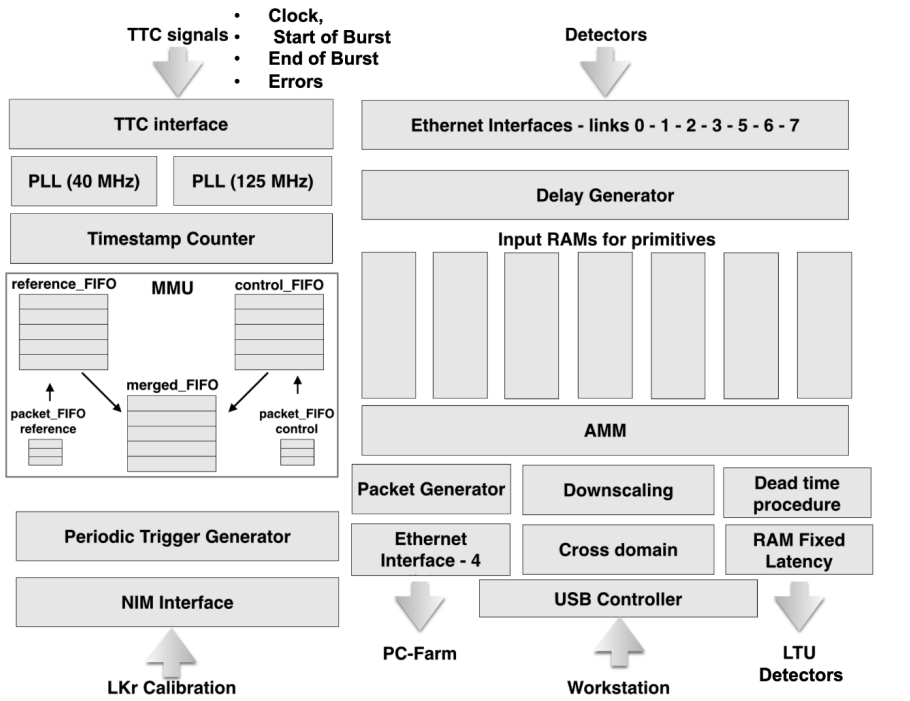
DAQ

- Data bursts are ~6s long
- Some detectors primitives (generated from TEL62 readout boards) are sent to L0TP over 1GbE UDP channels
- L0TP generates trigger with max latency of 1ms
- 40 MHz synchronous operation



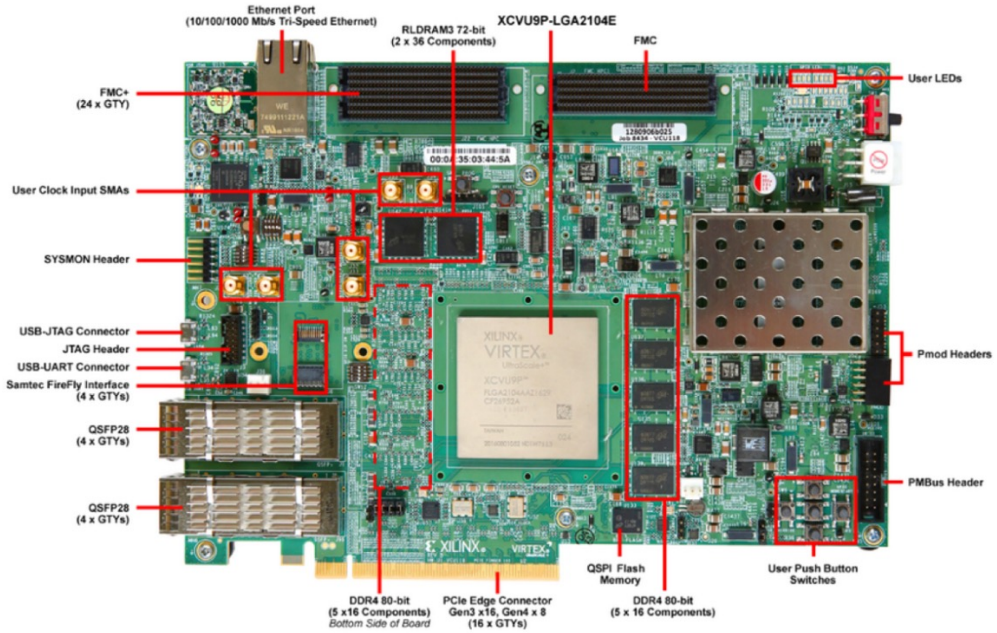
L0TP (2015-2022) ➔L0TP+ (2023-…)





- NA62 L0TP system suffered the shortcomings due to the **10 years old technology** of the adopted platform
  - Adopted Terasic DE4 board were nearly obsolete
- Migrate the system in order to follow the increases in the experiment luminosity
  - L0TP Altera Stratix IV GX FPGA resources barely enough to support full intensity, no way to scale to **x4 in intensity** with this platform
- Need to exploit **higher performances** (clock frequency, memory, high speed serial links) and **new design flow** (high level synthesis) introduced with recent FPGAs.

LOTP+ selected device



Xilinx Virtex UltraScale+ FPGA VCU118 Evaluation Kit

Featured Xilinx Devices

Featuring the **VCU118 XCVU9P-L2FLGA2104E FPGA**

System Logic Cells (K)	2,586
DSP Slices	6,840
Memory (Mb)	345.9
GTY 32.75 Gb/s Transceivers	120
I/O	832

Communication & Networking

- 10/100/1000 Mbps Ethernet (SGMII)
- Dual 4x28Gbps QSFP28 cages
- Samtec FireFly 4x28Gbps Interface
- Dual USB-to-UART Bridge with mico-B USB connector
- RJ45 Ethernet connector
- PCI Express endpoint Gen3 x 16

Clocking

- SI5335A Quad Clock Generator
- Si570 IIC Programmable LVDS Clock Generator
- SI5328C Clock Multiplier and Jitter Attenuator
- 2x SMA MGT Reference Clock inputs
- 1 SMA User Clock input

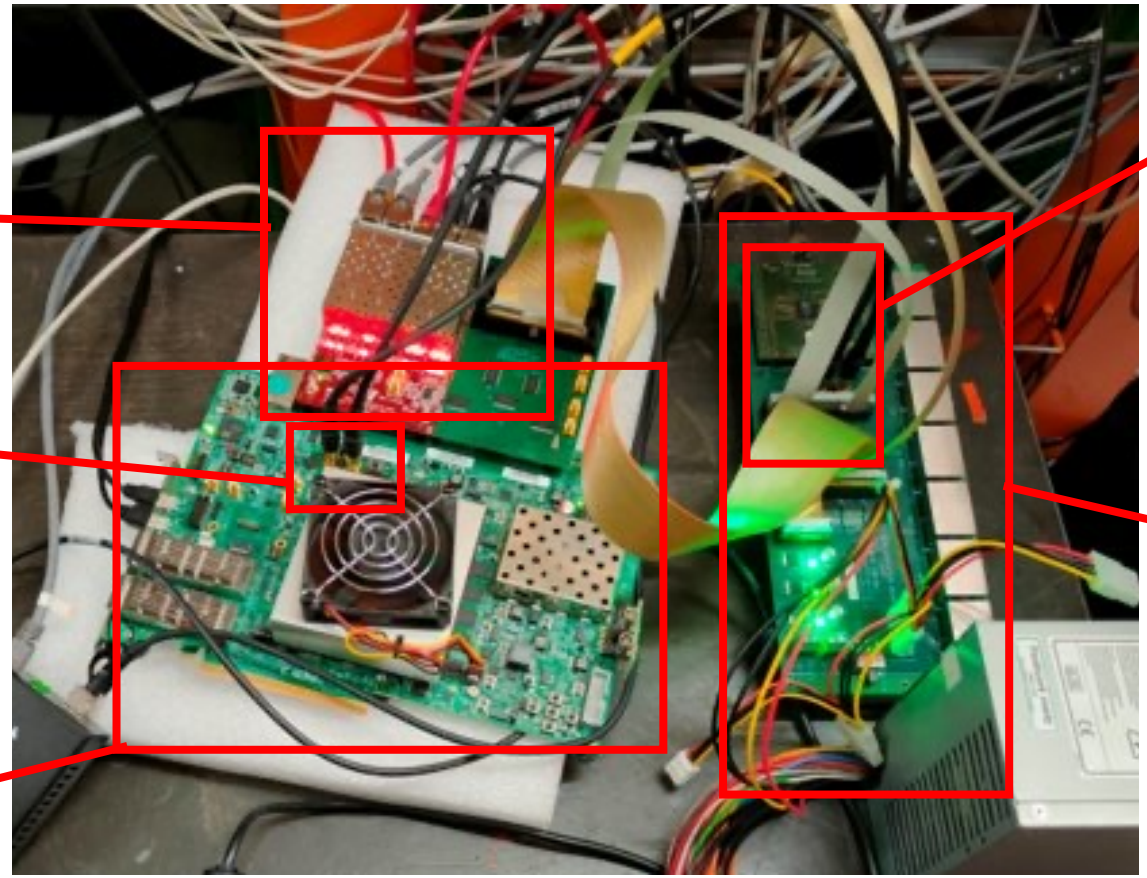
Memory

- Two 4 GB DDR4 component memory interfaces (five [256 Mb x 16] devices each)
- 4 MB RLD3 component memory interfaces (five [256 Mb x 16] devices each)IIC EEPROM: 8Kb
- Micro Secure Digital (SD) connector 1Gb Quad SPI Flash

Expansion Connectors

- FMC+ HSPC connector (24 – 28Gbps GTY Transceivers, 80 differential user defined pairs)
- FMC HPC1 connector (58 differential user defined pairs)
- PMOD header
- IIC

LOTP+ setup



10-port
SFP+(10x10G)
FMC Module

System Clock
@40MHz on SMA

VCU118 (DUT)

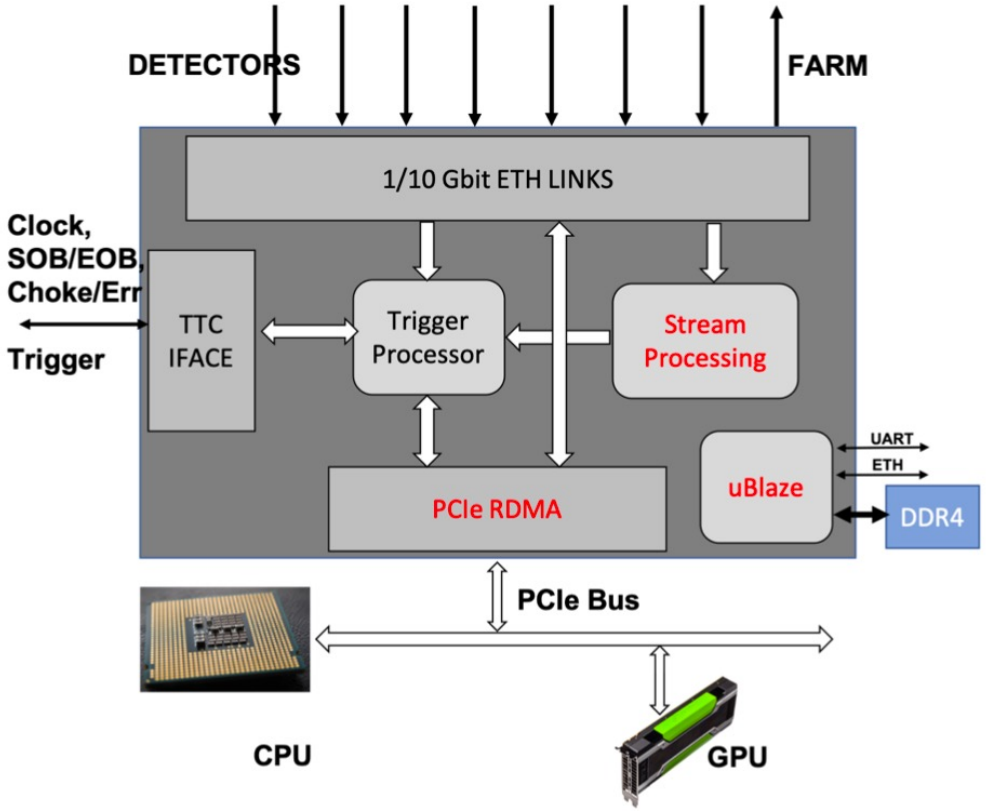
LTU interface

Auxiliary board
(with SOB, EOB, and
CHOKE signals)

L0TP+ new functionalities

L0TP+ reproduces all L0TP function and adds several capabilities to the original design

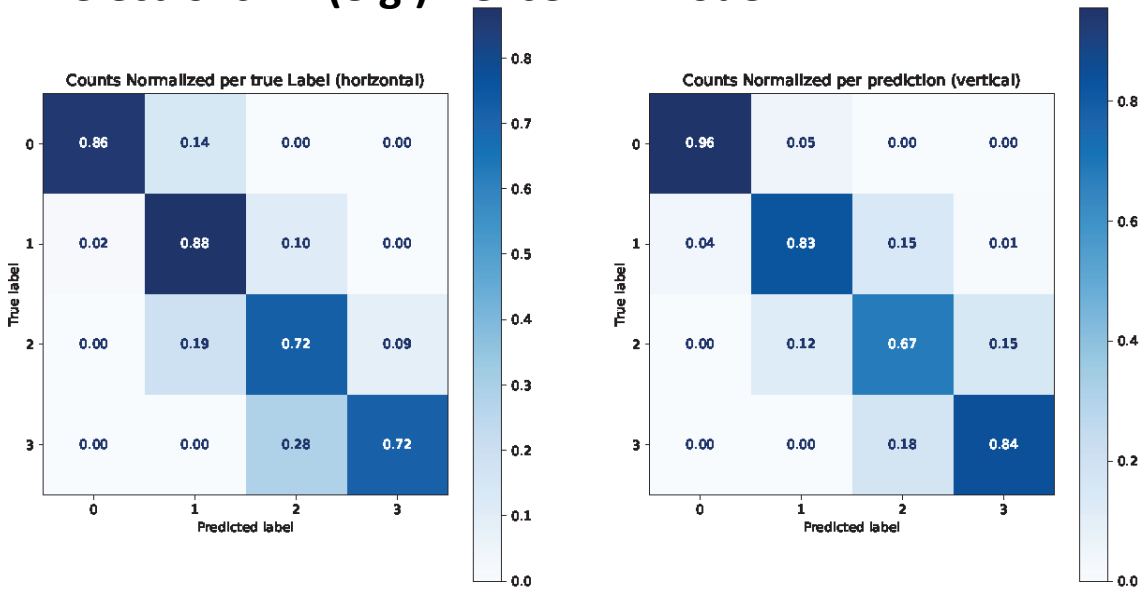
- **DATA LINKS**:
  the system is able to support eight 1/10 GbE links through the FMC+ daughtercard, while the two QSFP28 ports on the VCU118 can be used either to connect up to eight additional data links from the detectors or to expand the platform capabilities by interconnecting multiple boards via 100 Gbps low latency links.
- **MICROCONTROLLER:**
  a 32-bit MicroBlaze Soft-Core Micro Controller was integrated for debug and configuration purposes. Applications can be deployed onto it either bare metal or by Xilinx Petalinux.
- **STREAM PROCESSING MODULE:**
  with the outlook of processing primitive streams from additional subdetectors and thus improving the efficiency of the trigger, we designed a test case to leverage on the new features allowed by L0TP+ with HLS (e.g. online PID in RICH via HLS4ML Neural Networks)
- **PCIe HOST INTERFACE**

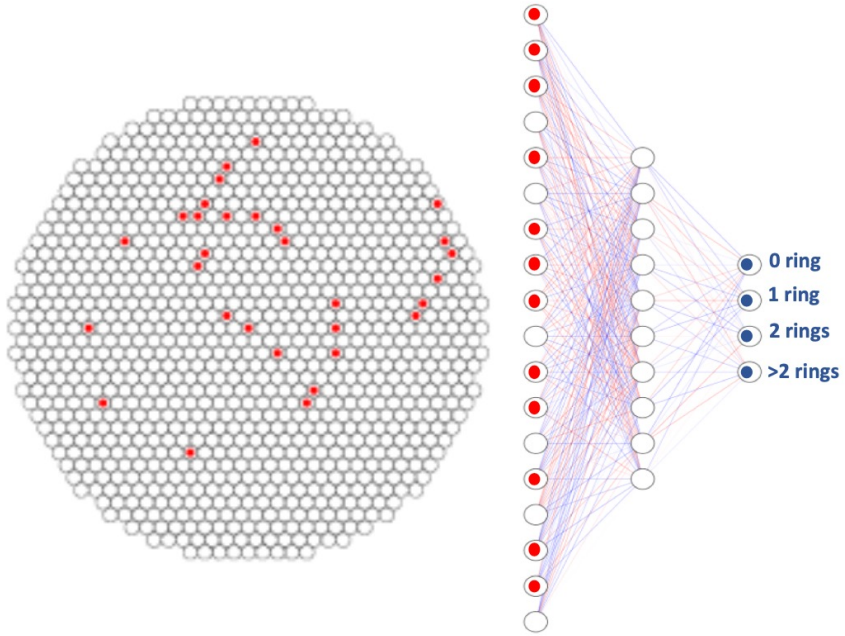


L0TP+ new features: ML on FPGA for trigger computing

TensorFlow → Keras → QKeras → hls4ml → Vivado™ HLS

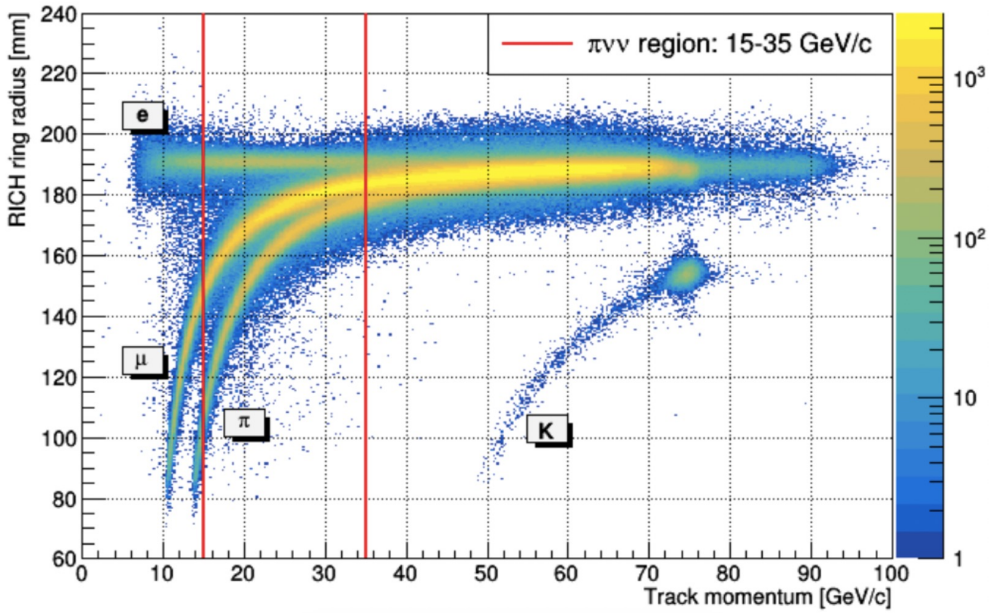
- **Exploration of Vivado HLS-based method to derive ML FPGA embedded hardware for trigger computing on data stream**
- **Goal**: for any event detected by the RICH provide an estimate for the **number charged particles** and the **number of electrons ➔ (e.g.) Dense NN model**





L0TP+ new features: ML on FPGA for trigger computing

- Preliminary results for online classification of the **number of "electrons"** show that even the very simple NN architectures that we tested are capable, below 35 GeV/c momentum, of reaching a non-negligible performance (see terminal picture below).
- It can be improved for the online unfiltered event stream using a **dedicated NN receiving in input data from other detectors** (e.g. L0CALO).




```
Total Events   163905
Total events of class 0 is    84628   (51.63 %)
Total events of class 1 is    76822   (46.87 %)
Total events of class 2 is     2432   (1.48 %)
Total events of class 3 is       23   (0.01 %)
Total events classified as 0 is    75533   (46.08 %)
Total events classified as 1 is    75209   (45.89 %)
Total events classified as 2 is    11920   (7.27 %)
Total events classified as 3 is     1243   (0.76 %)
Class  0  Efficiency 82.6  Purity 92.5  OverContamination  7.5  UnderContamination   0.0
Class  1  Efficiency 80.6  Purity 82.3  OverContamination  0.2  UnderContamination  17.5
Class  2  Efficiency 74.6  Purity 15.2  OverContamination  0.0  UnderContamination  84.8
Class  3  Efficiency 91.3  Purity  1.7  OverContamination  0.0  UnderContamination  98.3
```

APEIRON: a Framework for High Level Programming of Dataflow Applications on Multi-FPGA Systems

11 May 2023, 12:30
15m
Marriott Ballroom VII (Norfolk Waterside Marriott)

Oral | Track 11 - Heteroge... | Track X - Exascale Scie...

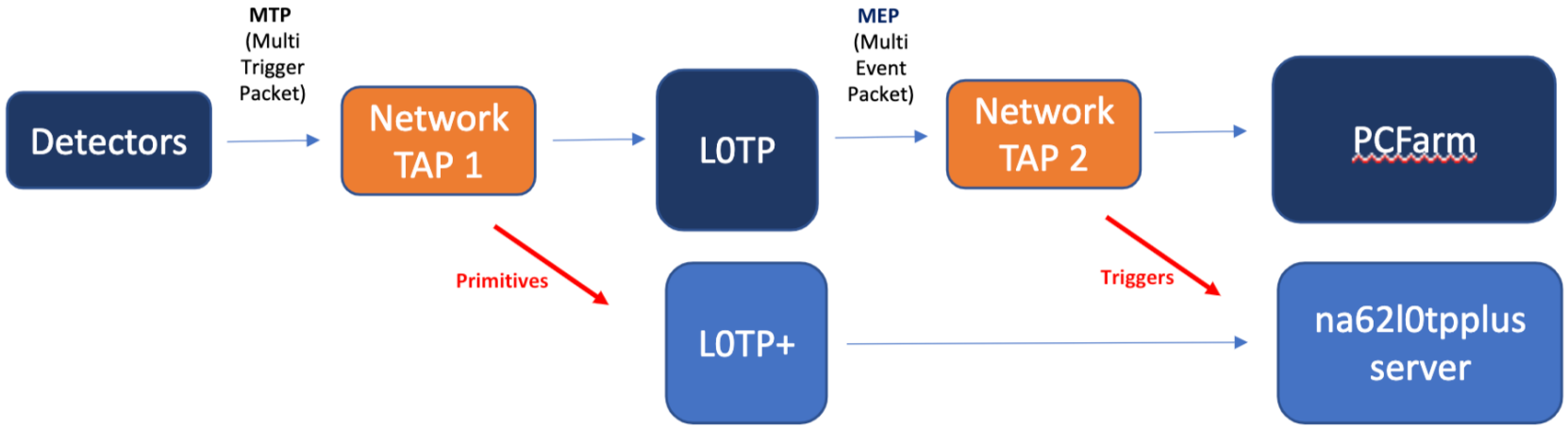
L0TP+ validation steps

2022

- Parasitic mode test
- Beam test online in November

2023

- Dry test in January/February
  (Integration completed)



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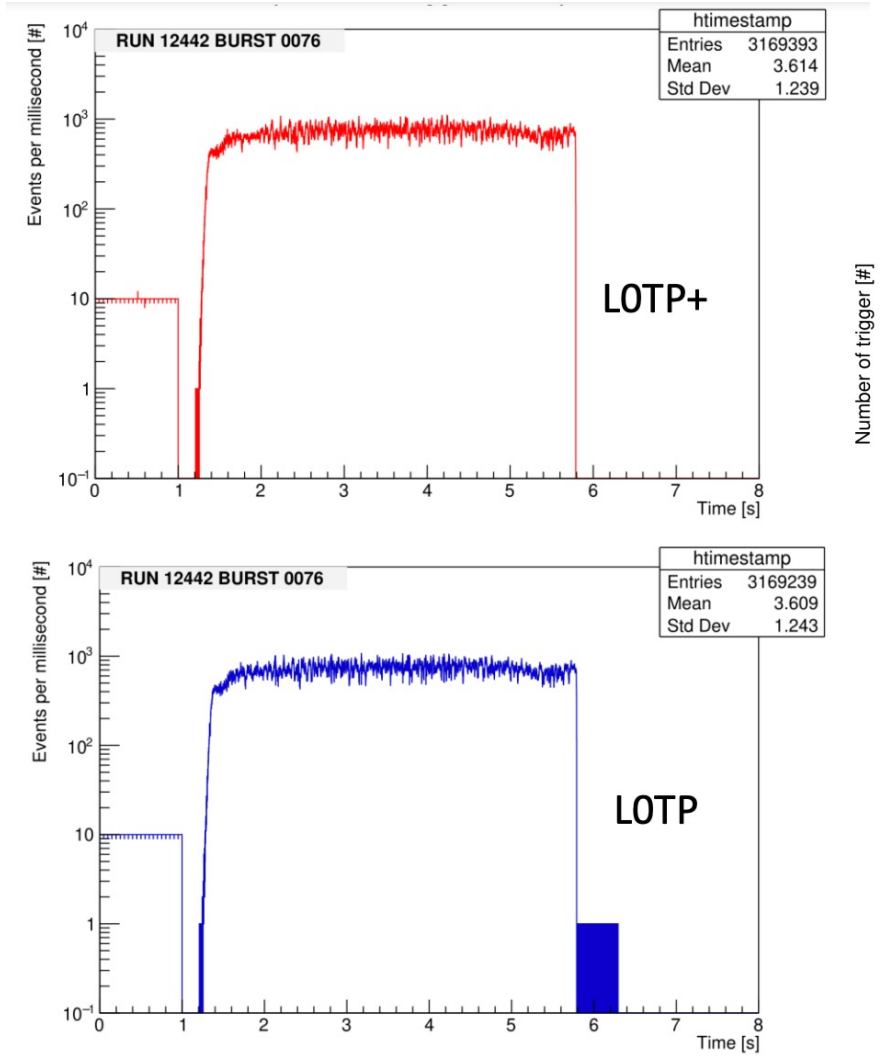

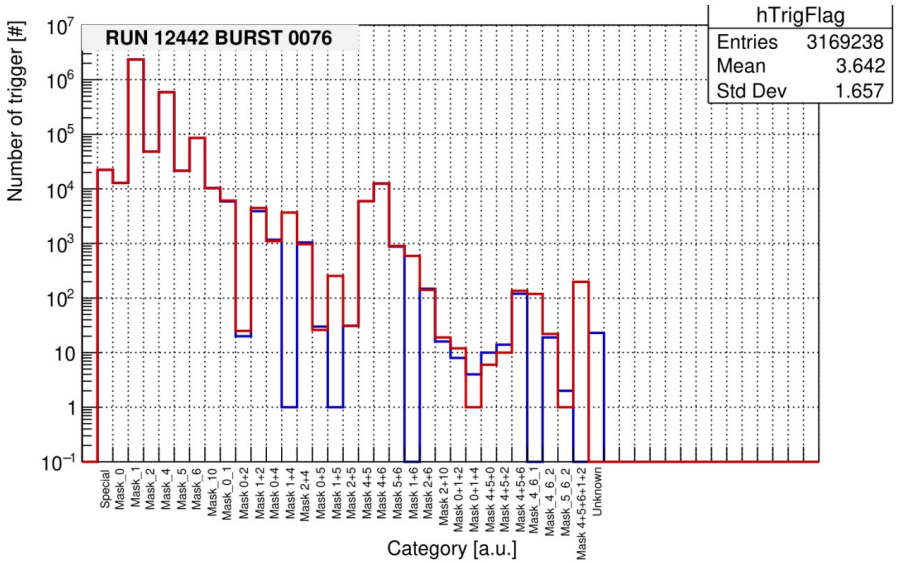

L0TP+ validation steps

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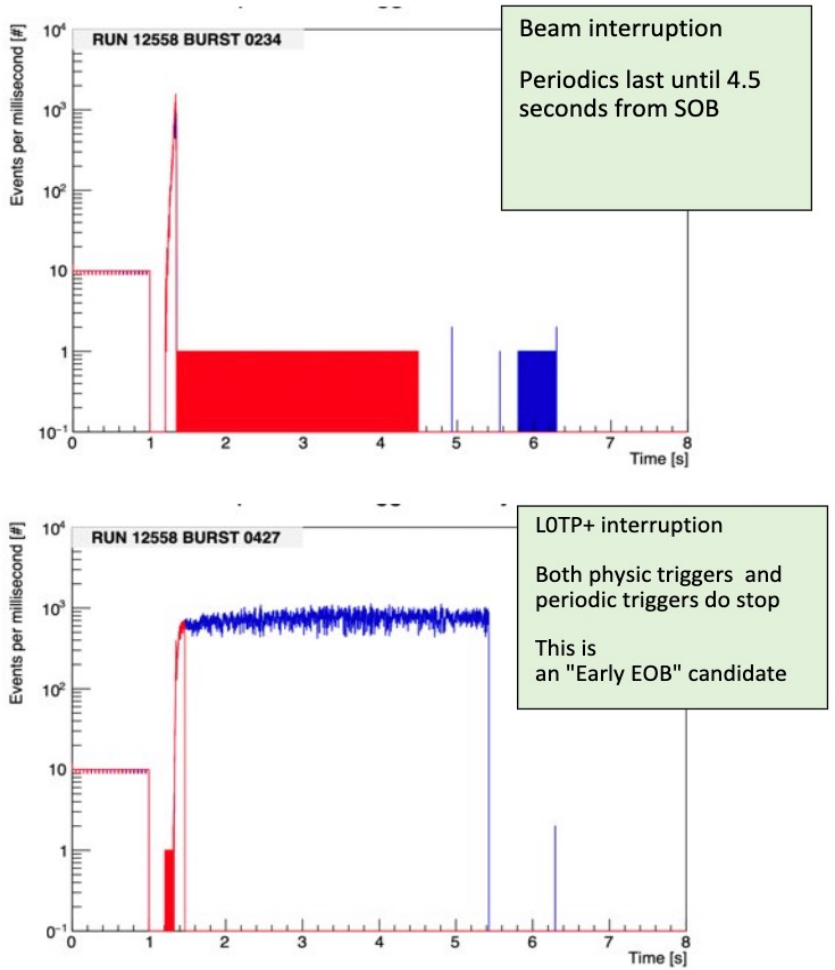
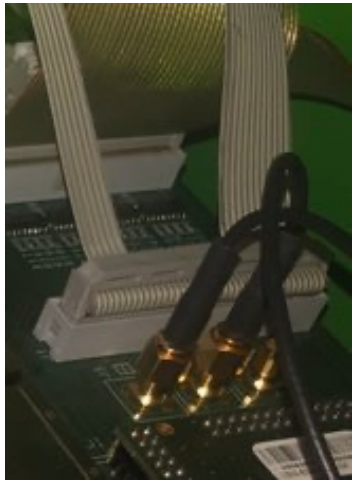
Number of trigger per millisecond, superimposed L0TP (blue) and L0TP+ (red)



What was observed was compatible with **fake SOB** (11 induced) and with **fake EOB** (01 induced)
This also match with the presence of a modified ribbon cable to reduce **crosstalk** in L0TP old setup, differently from the flat ribbon cable of the first L0TP+ parasitc setup



L0TP+ validation steps

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  (Integration completed)

- Last tests were performed in no beam (**dry run**) condition, swapping L0TP+ online and disconnecting L0TP

- System output was aligned with the standard NA62 data flow (from L0TP+ to PCFarms, fixed old issue on IP and MAC addresses) ➔ L0TP+ supports load balancing to PC Farm directly in hardware while L0TP uses a software program on server)

L0TP+ validation steps: Hardware

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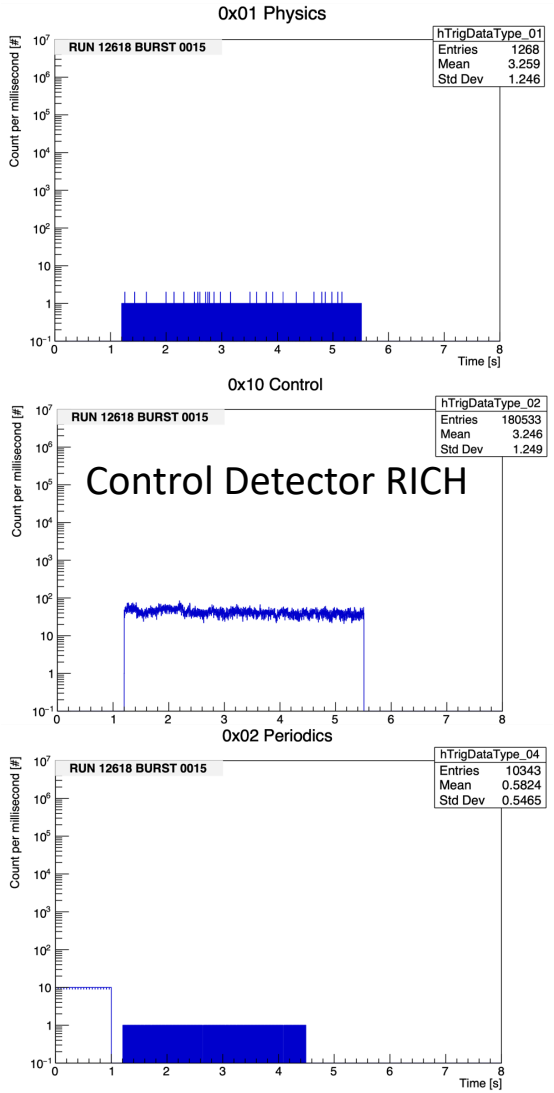

Few TDAQ boards on (RICH,MUV3,NCHOD) were used to send primitives to L0TP+.
The HV was switched off, so data acquired came from **electronic noise** due to low thresholds on TEL62

Conclusions

- Validation moved forward ➔ Fake EOB issue solved, CHOKE ON/OFF validated, Lkr Calib validated
- Fully integrated in NA62 data flow ➔ PC Farm Load balancing, RC command validated
  ➔ **L0TP+ IS NOW ONLINE** (since February last tests)

- **Next Step 1**: L0TP equivalent system at day zero (beam engineering run) ➔ in process during these days
- Continue testing until the start of Run ➔ increase confidence and test stability of L0TP+, debugging some new issues that may occurs before

- **Next Step 2**: keep parasitic setup as development platform during 2023
  ➔ ML PID on FPGA

BACKUP SLIDES

L0TP+ validation steps

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2023

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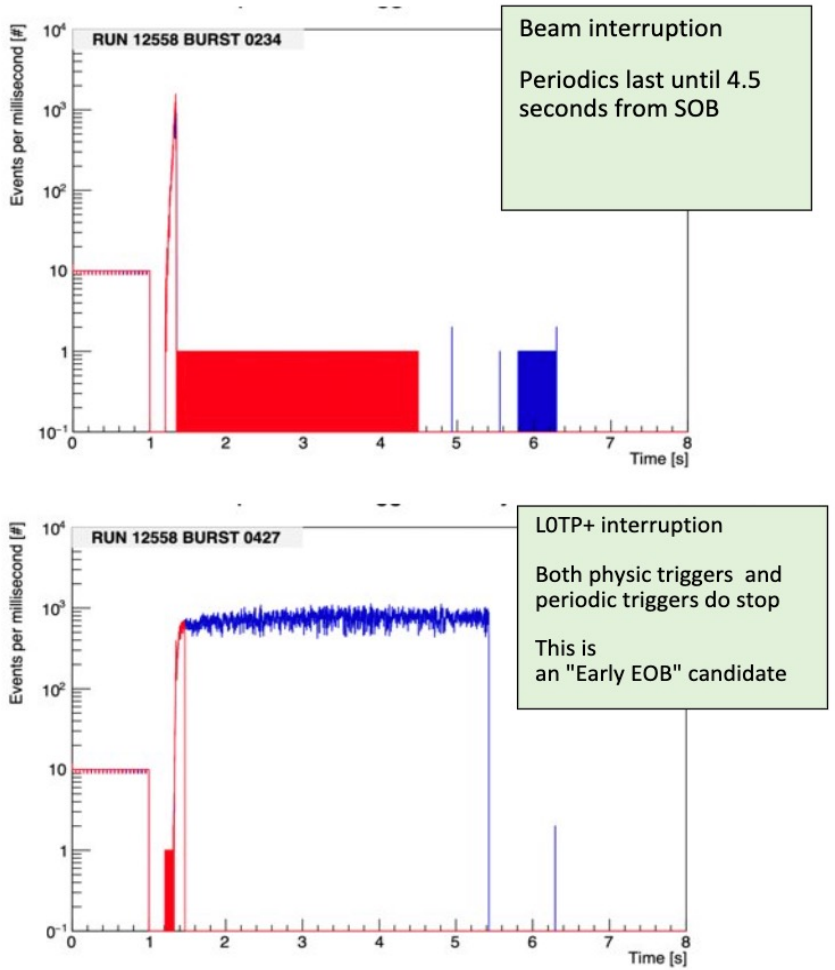
  (Integration completed)

Number of trigger per millisecond, superimposed L0TP (blue) and L0TP+ (red)



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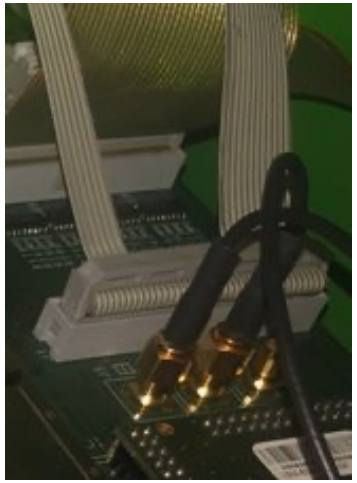

L0TP+ validation steps: Hardware

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2023

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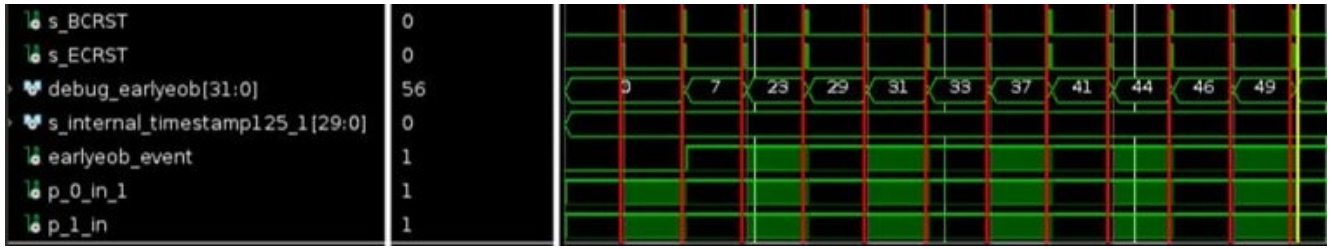
  (Integration completed)

"SOB-EOB" issues: **Crosstalk Hypothesis on flat ribbon cables**

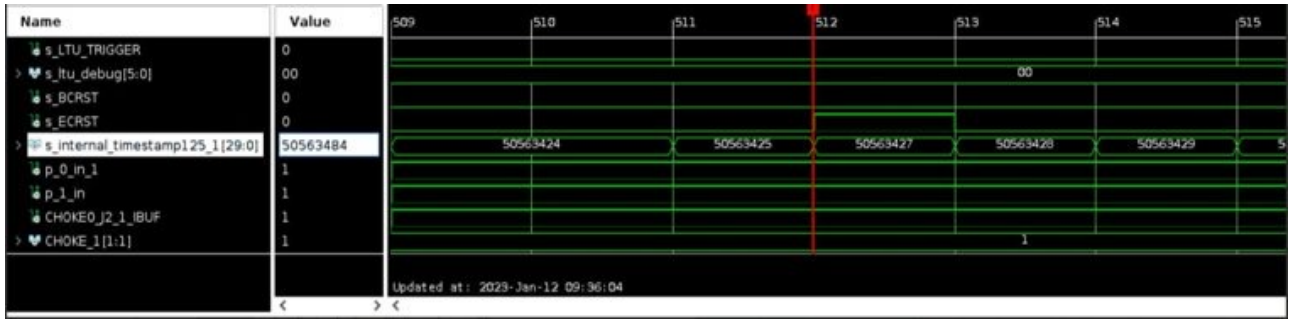
Confirmation strategy

Fake EOB counter logic on L0TP+ to quantify their relative frequency and to reproduce the Crosstalk issue



Solution

Switching to the custom L0TP Cable, Crosstalk issue seemed to be solved from the counter logic side.



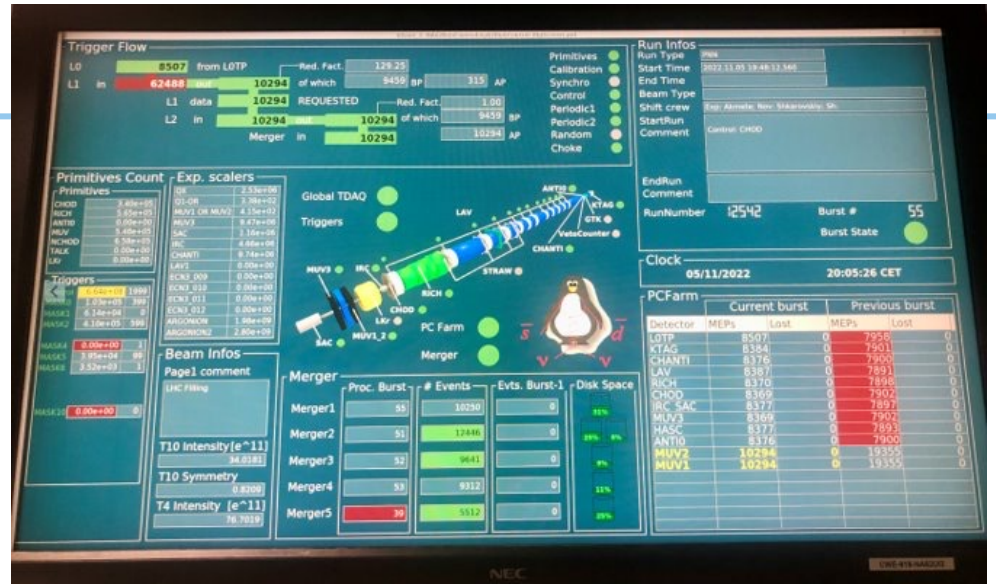
L0TP+ validation steps: Software

2022
- Parasitic mode test
- Beam test online in November

2023
- Dry test in January/February
  (Integration completed)

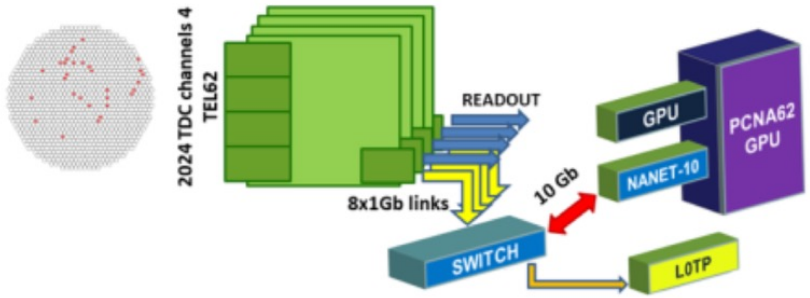
Big Screen display:
- Correct propagation of RC GUI changes through L0TP+ DIM Server (and last, its registers).
- Big Screen correctly reports all meaningful values for L0TP+ (as for L0TP)

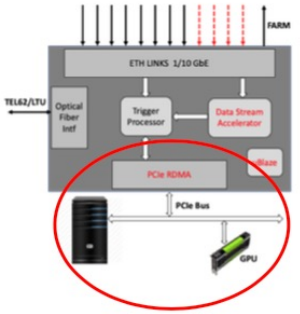
PC Farm load balancing (DIM):
Since L0TP+ supports load balancing (in a round-robin fashion) to PC Farm directly in hardware, once validated the correct utilization of the total number of PC Farms by L0TP+, we verified the correct behaviour also switching off some PC Farms and then reincluding them back.

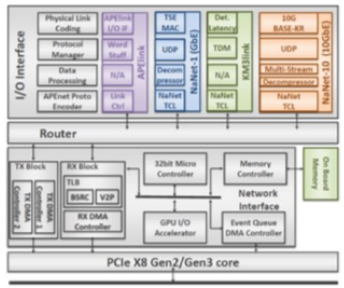


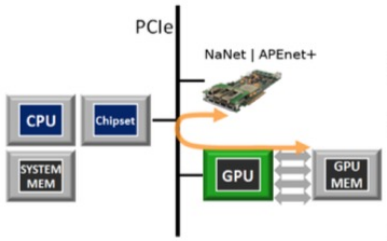
L0TP+ new features: GPU for trigger computing

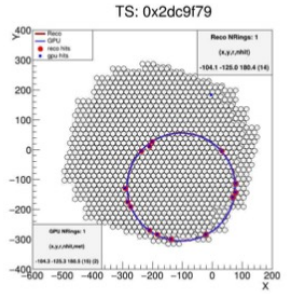
Heterogenous Computing Node for HEP low level trigger

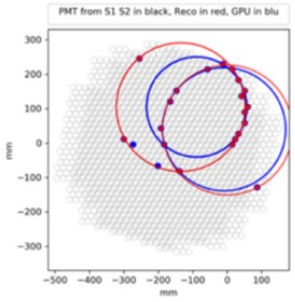












Leverage on NaNet project design

- Hardwired GPU Direct engine in FPGA implementing a low latency, low jitter data transfer between FPGA-based readout channels (Tel62) based on commodity protocol (UDP) and GPU
- GPU optimized application for identification of RICH Cherenkov ring
- Demonstrated in parasitic mode on NA62 experiment

A single device for L0TP GPU-accelerated to lower system complexity, to reduce trigger latencies and to enhance trigger performance. By product:

- L0TP+ complex diagnostic for hardware verification
- Backup primitives on trigger host server to get large statistics of trigger behavior and performance

L0TP+: porting of L0TP design

- The original design of L0TP processor has been ported on L0TP+ testbed
- TP coded in behavioral VHDL --> porting was "painless"
  - Synthesis ok, simulation in progress
- Integration with new ETH-UDP block (inherited from NaNet project) is in progress
- Achievements:
  - Clock speed > 130MHz (vs 125MHz old L0TP clock)
  - Very low resource occupancy --> room for hardware implementing additional features

Name	CLB LUTs (1182240)	Block RAM Tile (2160)	DSPs (6840)	Bonded IOB (832)
top_L0tp	2.15%	8.13%	0.15%	4.57%
CDC_inst2 (NIMInterface)	<0.01%	0.00%	0.00%	0.00%
clocks_resets_inst (axi_eth_1G_clocks_resets)	<0.01%	0.00%	0.00%	0.00%
CTSTMP (altcountertimestamp)	0.00%	0.02%	0.00%	0.00%
dbg_hub (dbg_hub)	0.05%	0.00%	0.00%	0.00%
ethlink_inst (ethlink)	1.99%	7.38%	0.15%	0.00%
jtag_inst (jtag_axi_master)	0.04%	0.12%	0.00%	0.00%
pll_40Mhz_inst (pll_40Mhz_diff_in)	0.00%	0.00%	0.00%	0.00%
Reg_inst (Register_intf_v1_0_S00_AXI)	0.01%	0.00%	0.00%	0.00%
syn_top.virt_IO (vio_0)	0.04%	0.00%	0.00%	0.00%
trigger_inst (Trigger)	0.03%	0.60%	0.00%	0.00%