Validation of the new hardware trigger processor at NA62 experiment

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and

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26th International Conference on Computing in High Energy & Nuclear Physics
CHEP 2023
Norfolk – 11th May 2023
NA62 Experiment

- Fixed target experiment located in the North Area of CERN dedicated to the study of charged kaon decays.
- Measurement of $BR(K^+ \to \pi^+ \nu \bar{\nu})$, through decay-in-flight technique.
- Last result (from 2016-2018 data) at 68% CL

$$BR(K^+ \to \pi^+ \nu \bar{\nu}) = (10.6^{+4.0}_{-3.4}\ stat \pm 0.9\ syst) \times 10^{-11}$$

- Nominal beam rate: 750 MHz
- $K^+$ rate: 45 MHz
- ~5 MHz $K^+$ decays in fiducial volume
Multi-level trigger
• Level-0 (L0TP, Level 0 Trigger Processor) HW trigger on FPGA (input 10 MHz -> output 1MHz)
• Level-1/2 software trigger running in DAQ farm (1MHz -> 100kHz)

DAQ
• Data bursts are ~6s long
• Some detectors primitives (generated from TEL62 readout boards) are sent to L0TP over 1GbE UDP channels
• L0TP generates trigger with max latency of 1ms
• 40 MHz synchronous operation
LOTP (2015-2022) ➔ LOTP+ (2023-...)

- NA62 LOTP system suffered the shortcomings due to the 10 years old technology of the adopted platform
  - Adopted Terasic DE4 board were nearly obsolete

- Migrate the system in order to follow the increases in the experiment luminosity
  - LOTP Altera Stratix IV GX FPGA resources barely enough to support full intensity, no way to scale to x4 in intensity with this platform

- Need to exploit higher performances (clock frequency, memory, high speed serial links) and new design flow (high level synthesis) introduced with recent FPGAs.
Xilinx Virtex UltraScale+ FPGA VCU118 Evaluation Kit

**Featured Xilinx Devices**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Logic Cells (K)</td>
<td>2,586</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>6,840</td>
</tr>
<tr>
<td>Memory (Mb)</td>
<td>345.9</td>
</tr>
<tr>
<td>GTY 32.75 Gb/s Transceivers</td>
<td>120</td>
</tr>
<tr>
<td>I/O</td>
<td>832</td>
</tr>
</tbody>
</table>

**Expansion Connectors**

- FMC+ HSPC connector (24 – 28Gbps GTY Transceivers, 80 differential user defined pairs)
- FMC HPC1 connector (58 differential user defined pairs)
- PMOD header
- IIC

**Communication & Networking**

- 10/100/1000 Mbps Ethernet (SGMII)
- Dual 4x28Gbps QSFP28 cages
- Samtec FireFly 4x28Gbps Interface
- Dual USB-to-UART Bridge with micro-B USB connector
- RJ45 Ethernet connector
- PCI Express endpoint Gen3 x 16

**Clocking**

- SI5335A Quad Clock Generator
- SI570 IIC Programmable LVDS Clock Generator
- SI5328C Clock Multiplier and Jitter Attenuator
- 2x SMA MGT Reference Clock inputs
- 1 SMA User Clock input

**Memory**

- Two 4 GB DDR4 component memory interfaces (five [256 Mb x 16] devices each)
- 4 MB RLD3 component memory interfaces (five [256 Mb x 16] devices each)
  - IIC EEPROM: 8Kb
  - Micro Secure Digital (SD) connector 1Gb Quad SPI Flash
LOTP+ setup

10-port SFP+(10x10G) FMC Module

System Clock @40MHz on SMA

VCU118 (DUT)

LTU interface

Auxiliary board (with SOB, EOB, and CHOKE signals)
LOTP+ new functionalities

LOTP+ reproduces all LOTP function and adds several capabilities to the original design

- **DATA LINKS:**
  the system is able to support eight 1/10 GbE links through the FMC+ daughtercard, while the two QSFP28 ports on the VCU118 can be used either to connect up to eight additional data links from the detectors or to expand the platform capabilities by interconnecting multiple boards via 100 Gbps low latency links.

- **MICROCONTROLLER:**
  a 32-bit MicroBlaze Soft-Core Micro Controller was integrated for debug and configuration purposes. Applications can be deployed onto it either bare metal or by Xilinx Petalinux.

- **STREAM PROCESSING MODULE:**
  with the outlook of processing primitive streams from additional subdetectors and thus improving the efficiency of the trigger, we designed a test case to leverage on the new features allowed by L0TP+ with HLS (e.g. online PID in RICH via HLS4ML Neural Networks)

- **PCIe HOST INTERFACE**
LOTP+ new features: ML on FPGA for trigger computing

- Exploration of Vivado HLS-based method to derive ML FPGA embedded hardware for trigger computing on data stream
- Goal: for any event detected by the RICH provide an estimate for the number charged particles and the number of electrons (e.g.) Dense NN model
L0TP+ new features: ML on FPGA for trigger computing

- Preliminary results for online classification of the number of "electrons" show that even the very simple NN architectures that we tested are capable, below 35 GeV/c momentum, of reaching a non-negligible performance (see terminal picture below).
- It can be improved for the online unfiltered event stream using a dedicated NN receiving in input data from other detectors (e.g. L0CALO).
LOTP+ validation steps

2022
- Parasitic mode test
- Beam test online in November

2023
- Dry test in January/February
  (Integration completed)
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What was observed was compatible with fake SOB (11 induced) and with fake EOB (01 induced)
This also match with the presence of a modified ribbon cable to reduce crosstalk in L0TP old setup, differently from the flat ribbon cable of the first L0TP+ parasitic setup
LOTP+ validation steps

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2023
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• Last tests were performed in no beam (dry run) condition, swapping L0TP+ online and disconnecting L0TP

• System output was aligned with the standard NA62 data flow (from L0TP+ to PCFarms, fixed old issue on IP and MAC addresses) ➔ L0TP+ supports load balancing to PC Farm directly in hardware while L0TP uses a software program on server)
LOTP+ validation steps: Hardware

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2023
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Few TDAQ boards on (RICH, MUV3, NCHOD) were used to send primitives to L0TP+.
The HV was switched off, so data acquired came from **electronic noise** due to low thresholds on TEL62.
Conclusions

- Validation moved forward ➔ Fake EOB issue solved, CHOKE ON/OFF validated, Lkr Calib validated
- Fully integrated in NA62 data flow ➔ PC Farm Load balancing, RC command validated ➔ **L0TP+ IS NOW ONLINE** (since February last tests)

- **Next Step 1**: L0TP equivalent system at day zero (beam engineering run) ➔ in process during these days
- Continue testing until the start of Run ➔ increase confidence and test stability of L0TP+, debugging some new issues that may occurs before

- **Next Step 2**: keep parasitic setup as development platform during 2023 ➔ ML PID on FPGA
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"SOB-EOB" issues: Crosstalk Hypothesis on flat ribbon cables

Confirmation strategy
Fake EOB counter logic on L0TP+ to quantify their relative frequency and to reproduce the Crosstalk issue

Solution
Switching to the custom L0TP Cable, Crosstalk issue seemed to be solved from the counter logic side.
LOTP+ validation steps: Software

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2023
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Big Screen display:
• Correct propagation of RC GUI changes through LOTP+ DIM Server (and last, its registers).
• Big Screen correctly reports all meaningful values for LOTP+ (as for LOTP)

PC Farm load balancing (DIM):
Since LOTP+ supports load balancing (in a round-robin fashion) to PC Farm directly in hardware, once validated the correct utilization of the total number of PC Farms by LOTP+, we verified the correct behaviour also switching off some PC Farms and then reincluding them back.
**LOTP+ new features: GPU for trigger computing**

**Heterogenous Computing Node for HEP low level trigger**

Leverage on NaNet project design

- Hardwired GPU Direct engine in FPGA implementing a low latency, low jitter data transfer between FPGA-based readout channels (Tel62) based on commodity protocol (UDP) and GPU
- GPU optimized application for identification of RICH Cherenkov ring
- Demonstrated in parasitic mode on NA62 experiment

A single device for L0TP GPU-accelerated to lower system complexity, to reduce trigger latencies and to enhance trigger performance. By product:

- L0TP+ complex diagnostic for hardware verification
- Backup primitives on trigger host server to get large statistics of trigger behavior and performance
LOTP+: porting of L0TP design

- The original design of L0TP processor has been ported on L0TP+ testbed
- TP coded in behavioral VHDL --> porting was "painless"
  - Synthesis ok, simulation in progress
- Integration with new ETH-UDP block (inherited from NaNet project) is in progress
- Achievements:
  - Clock speed > 130MHz (vs 125MHz old L0TP clock)
  - Very low resource occupancy --> room for hardware implementing additional features