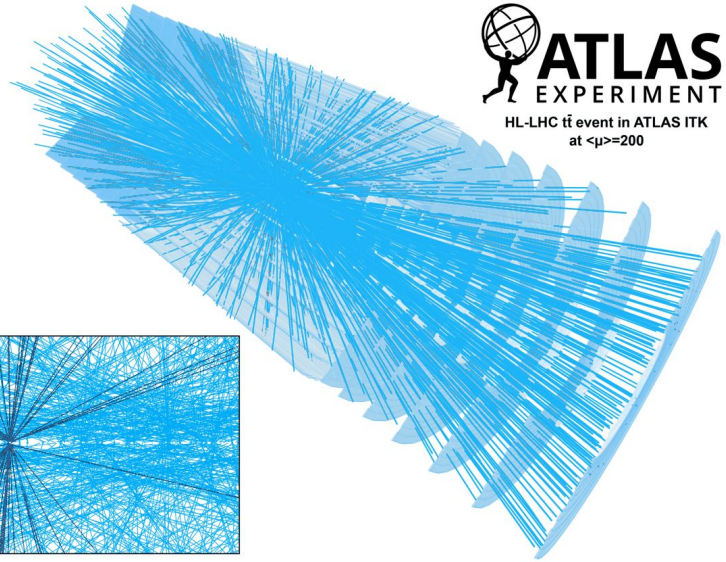
ATLAS Trigger and Data Acquisition Upgrades for the High Luminosity LHC

Andrea Negri
(University and INFN Pavia)
on behalf of the
ATLAS Collaboration

High Luminosity LHC

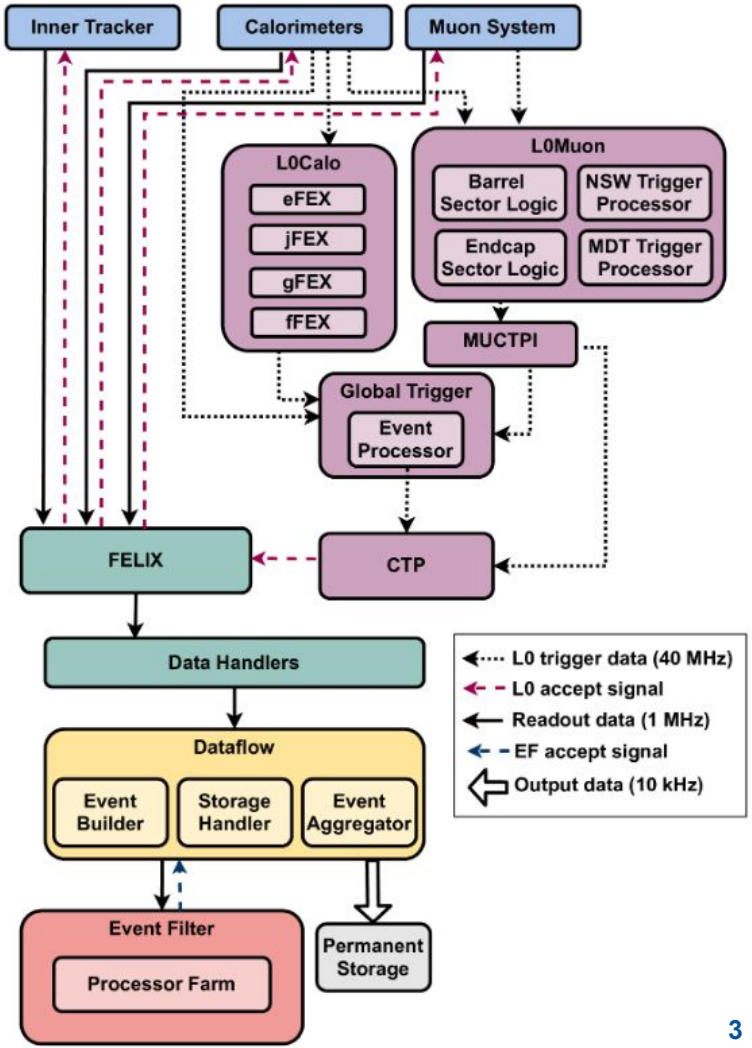


- Trigger & data acquisition challenge
  - Luminosity: $2 \mapsto 7.5 \cdot 10^{34}$ $cm^{-2}s^{-1}$
  - Pileup: $60 \mapsto 200$
    - more time consuming

- ATLAS detector upgrade
  - new Tracker, new Timing Detector,
    additional muon chambers, new Tile electronics, …

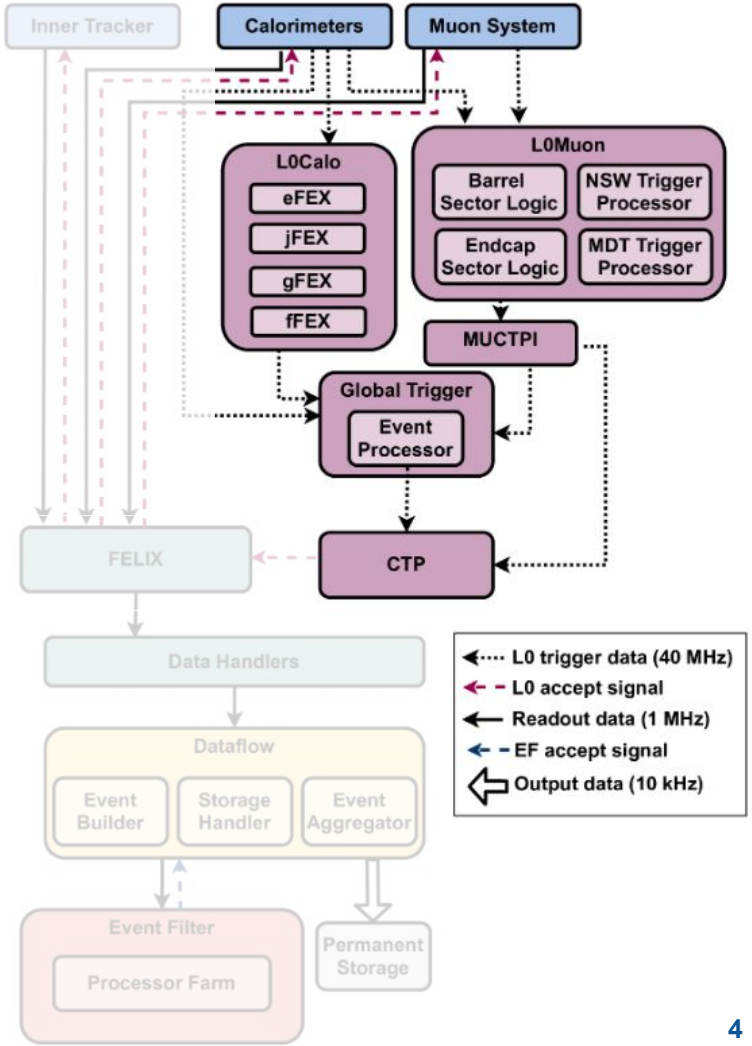
Trigger DAQ upgrades

- Hardware based L0 trigger
  - Data reduction: 40 MHz ⟶ 1 MHz
    - 100 kHz in Run 3
  - Latency: 10 μs
    - 2.5 μs in Run 3
- Software based Event Filter
  - Data reduction: 1 MHz ⟶ 10 kHz
    - ~ 3 kHz in Run 3

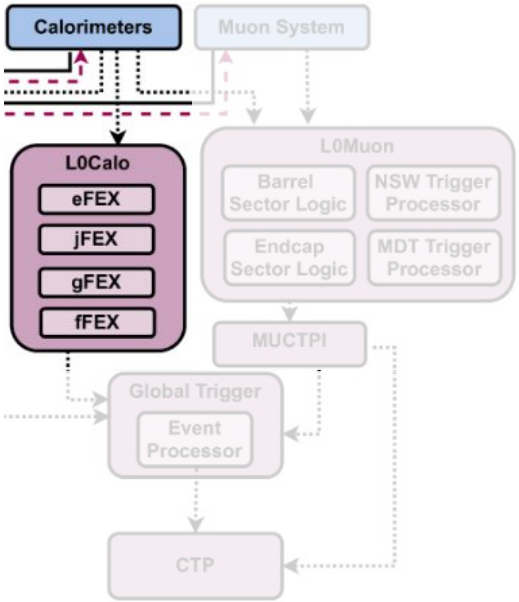


Level-0 Trigger

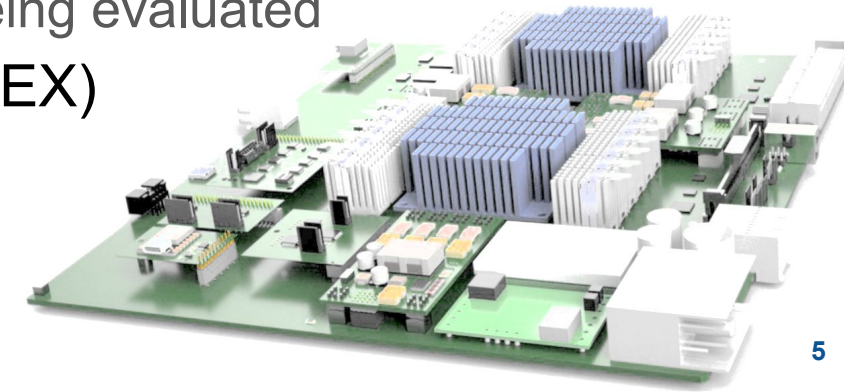
- Data from calorimeters and muon detectors processed by dedicated trigger systems
  - L0Calo and L0Muon
- Global trigger runs full granularity offline-like reconstruction
  - @ 40 MHz
- Outputs sent to Central Trigger Processor to make L0 decision
  - Accepted events sent to Event Filter



Level-0 Calo

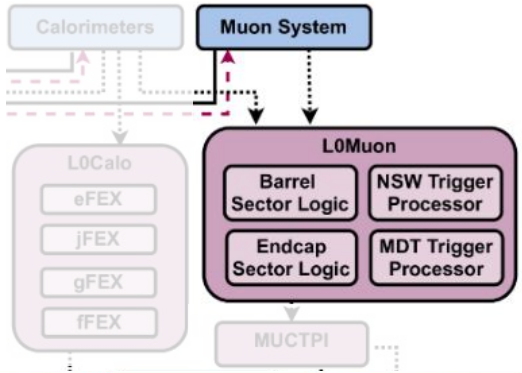


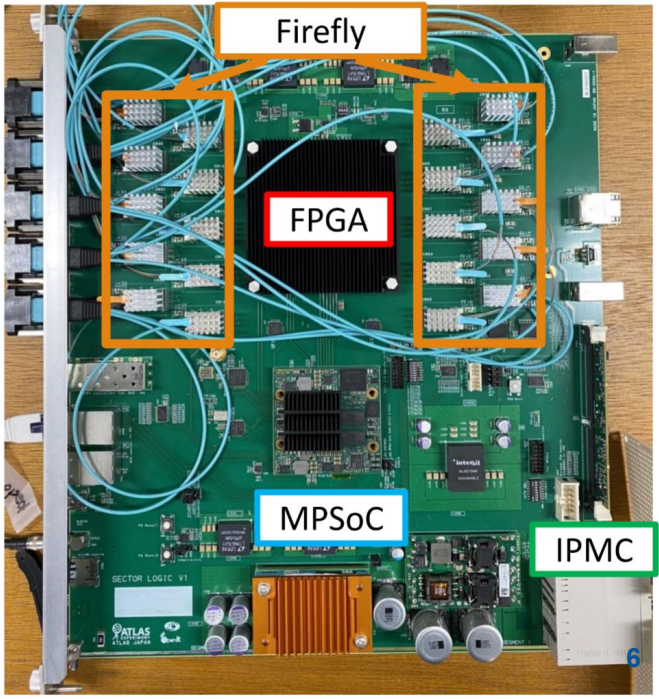
- **F**eature **EX**tractors
  - FPGA-based trigger boards optimized to trigger on different physics objects
- **F**eature **EX**tractors from Run 3
  - e(lectron)FEX, j(et)FEX, g(lobal)FEX
  - Hardware retained with upgraded firmware
  - Needed modifications currently being evaluated
- New forward Feature EXtractor (fFEX)
  - EM triggers for $|\eta| > 2.5$
  - Jet triggers for $|\eta| > 3.3$
  - Preliminary design being studied



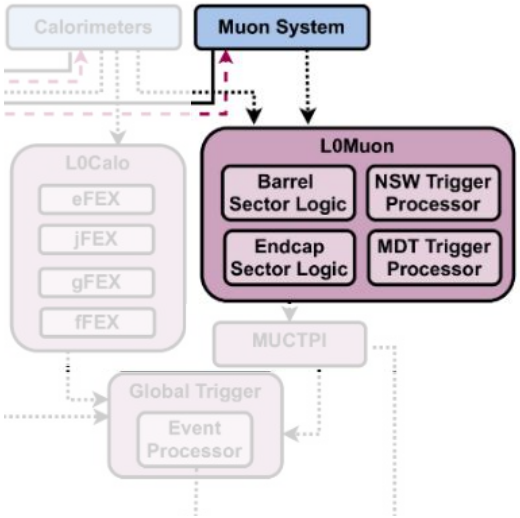
Level-0 Muon

- Sector Logic
  - FPGA-based off-detector trigger logic
- Common hardware platform for Barrel and End-Cap
  - 1st prototype tested →
    - integration with on-detector board, from trigger chambers to Sector Logic
  - 2nd prototype design started

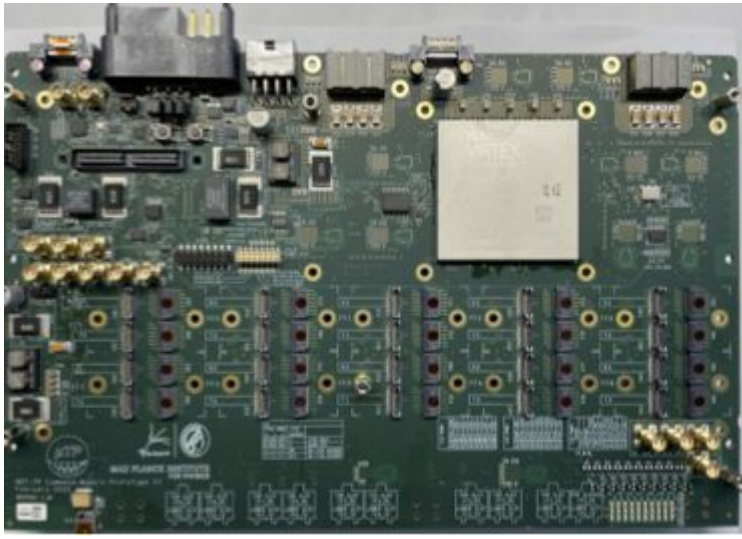




Level-0 Muon

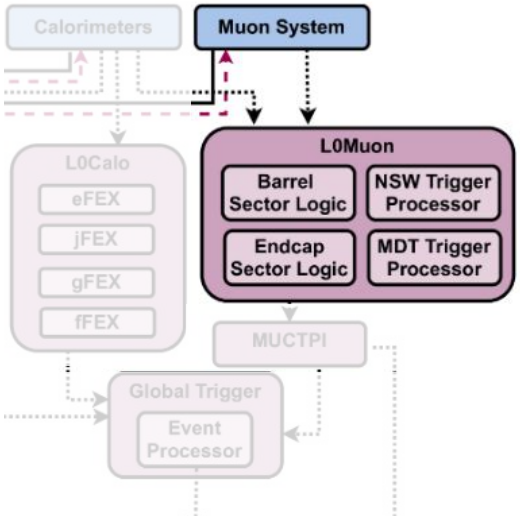


- Trigger Processors
  - receive data from precision muon chambers and new small wheel muon chambers
  - interact with sector logic
- ATCA blades based on a common open source platform (Apollo*), that simplifies custom ATCA blade design
  - Service module for common services
  - Command module containing application specific elements

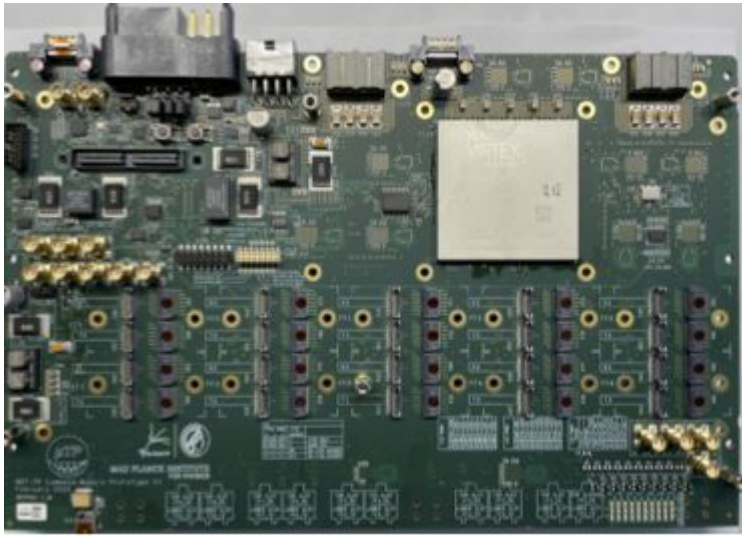


* https://doi.org/10.48550/arXiv.1911.06452

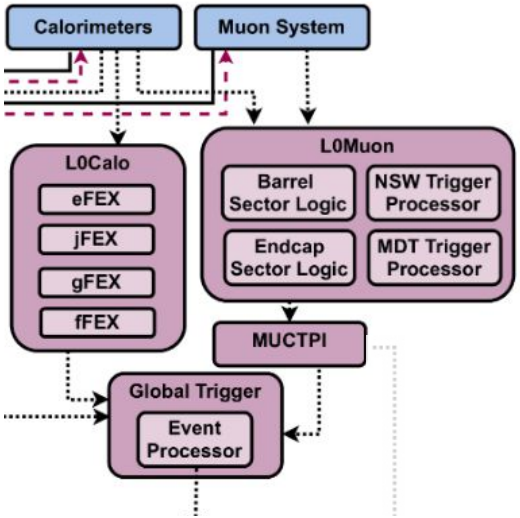
Level-0 Muon



- Trigger Processors
  - receive data from precision muon chambers and new small wheel muon chambers
  - interact with sector logic
- Barrel: MDT precision chambers
  - v1 Command Module prototype under test
- End-Cap: New Small Wheel
  - schedule completely overhauled based on Run 3 experience



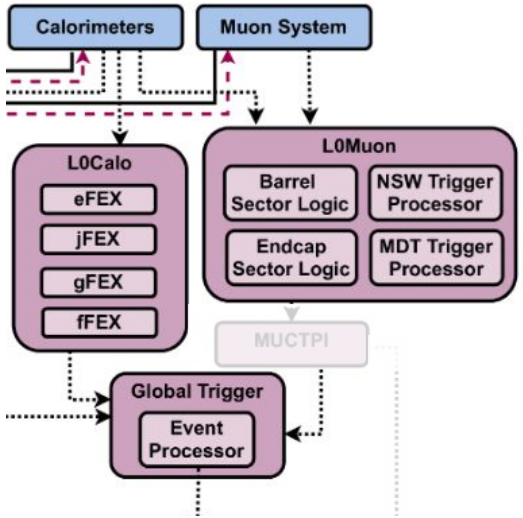
Level-0 Global Trigger

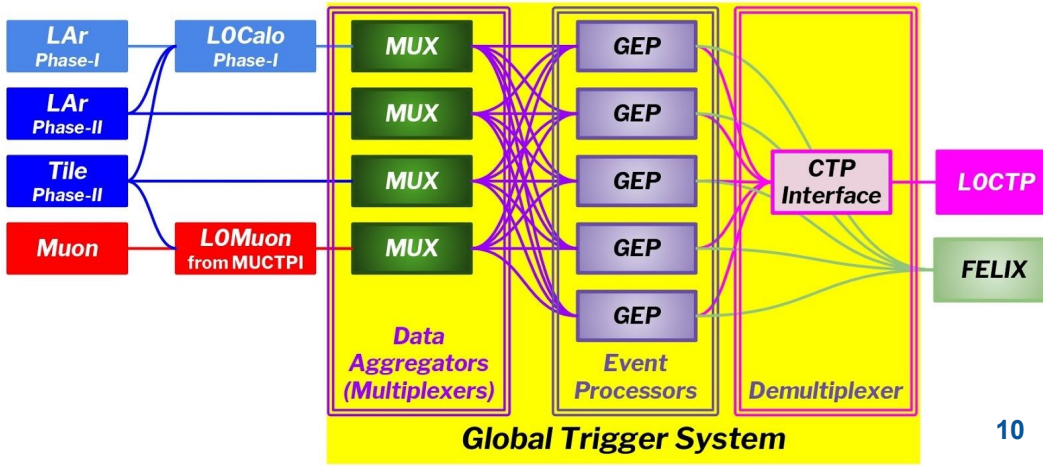


- Low-level analogue to Event Filter (EF)
  - HLT-like object-level and event-level reconstruction and analysis at 40 MHz
  - it will replace Run 3 topological processor
  - input: 50 Tb/s
- Algorithms organized as trigger signatures in parallel w/ EF
  - calo, muon, topological cluster, e/γ, τ, jets, E_T^{miss} and other topological quantities
  - Initial trigger menu will start from Run 3 signatures
  - Additional triggers will be added during commissioning

L0 Global Trigger

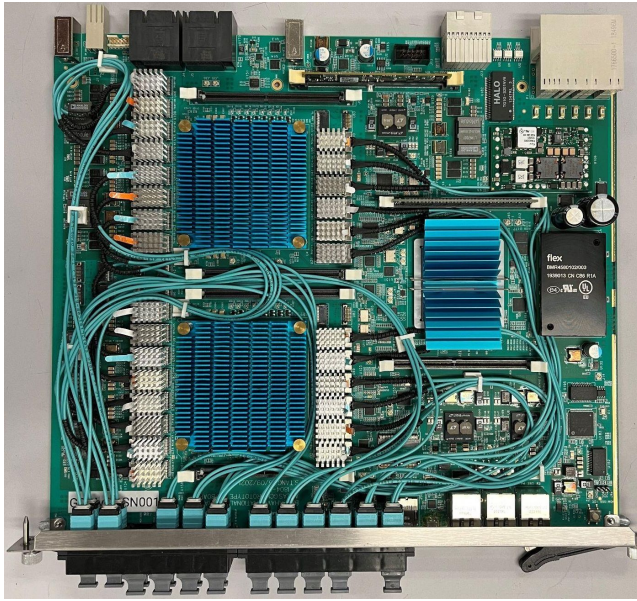
- Farm of processing units
- Collect all data from a single event onto one FPGA
  - data aggregation and time multiplexing (MUX)
  - each Global Event Processors (GEP) process one event
  - demultiplexing step to collect GEP outputs and feed the Central Trigger Processor

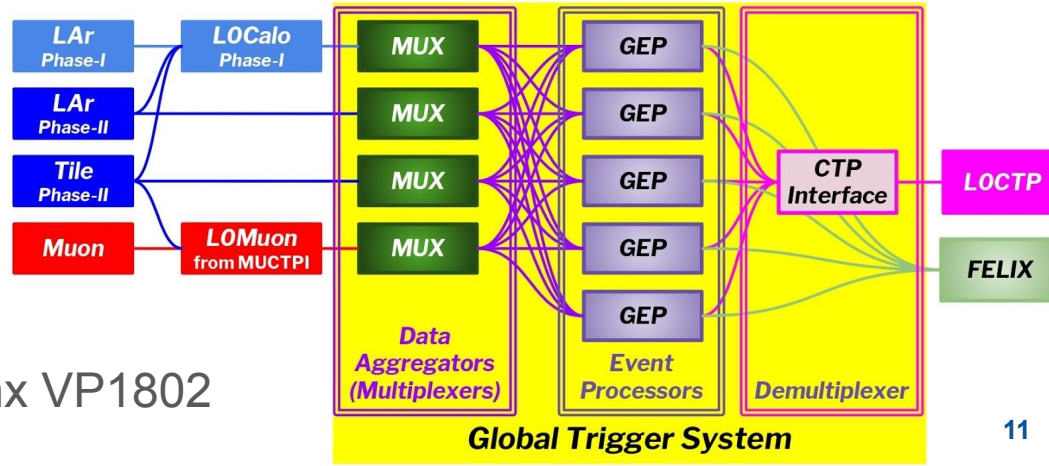




L0 Global Trigger

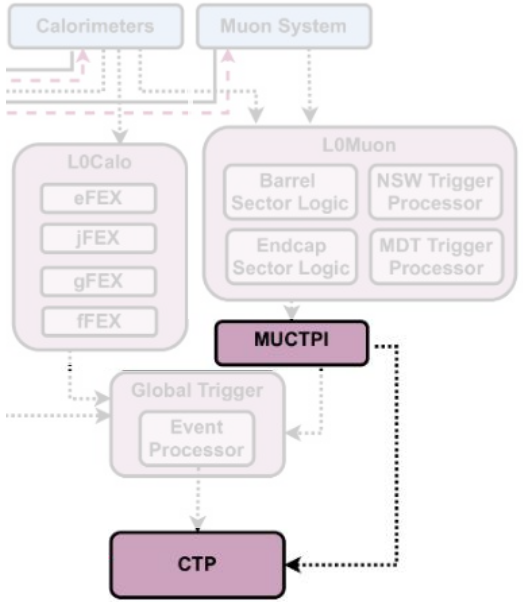
- All modules based on common hardware ATCA platform
  - different functions implemented in firmware
- Prototypes
  - v2b available & tested
    - Based on Xilinx Virtex UltraScale+ 13P
  - v3 schematic review under way
    - w/ Versal Premium Xilinx VP1802

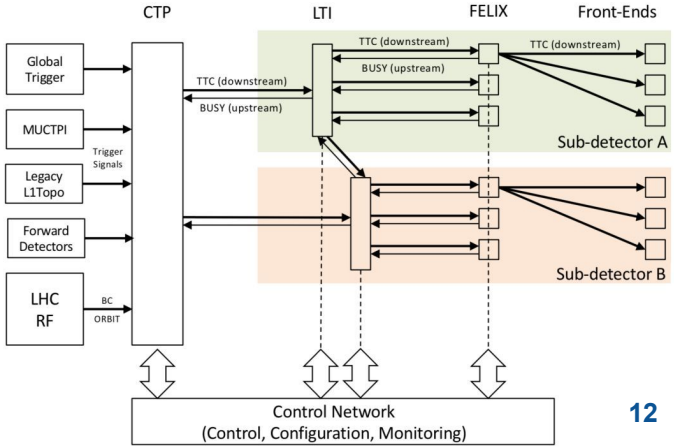




Central Trigger

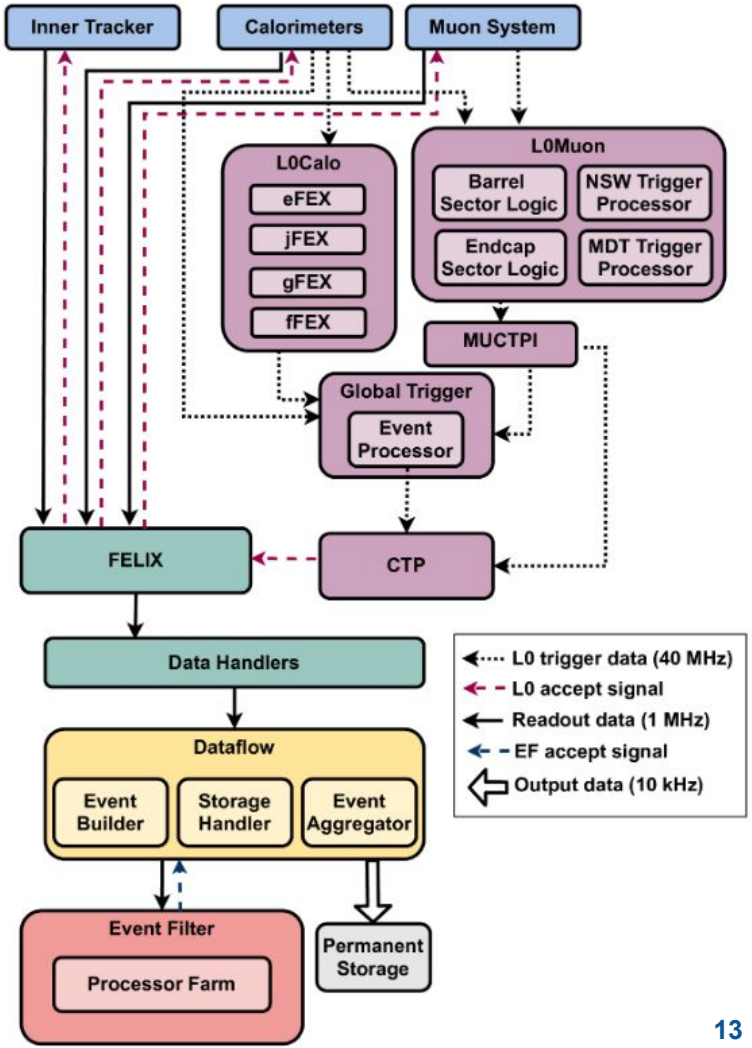
- Central Trigger Processor
  - Final decision, prescales, vetos
  - Number of L0 triggers: 512 → 1024
  - Passed specification review
- CTP drives the Trigger, Timing and Control (TTC) system network
  - TTC distributed via the Local Trigger Interface (LTI) modules
    - Test Setup available
- Muon-CTP Interface (MUCTPI)
  - Re-use Run 3 HW with new FW





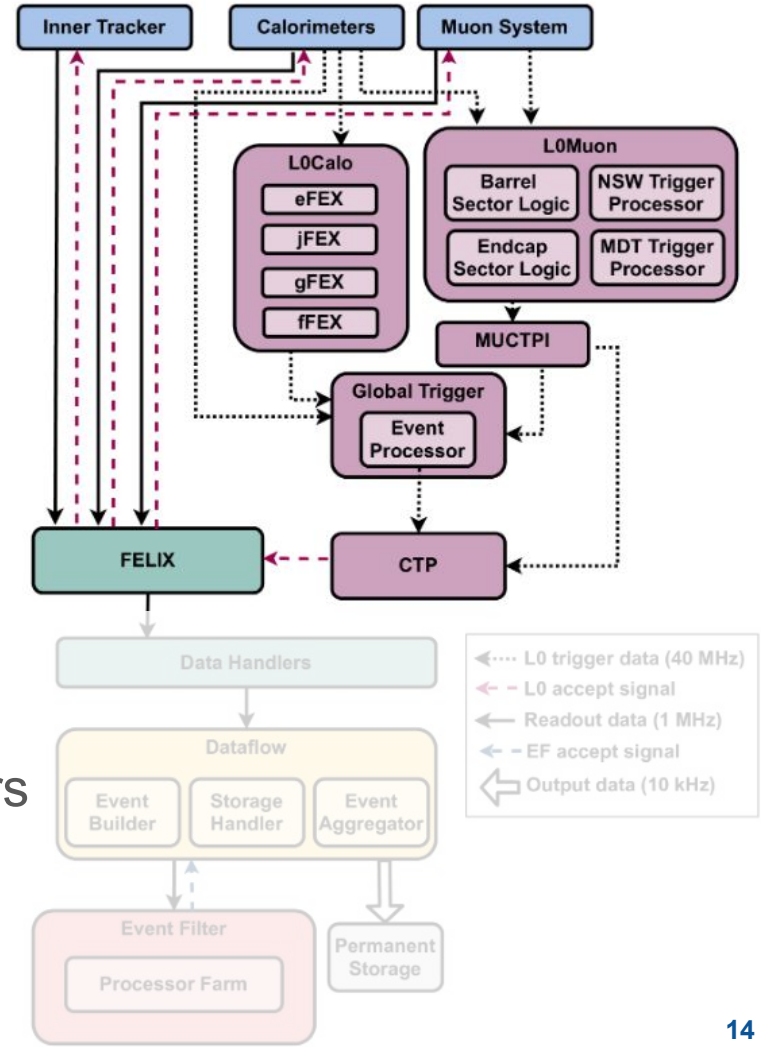
High Level Trigger

- Full event building at 1 MHz
  - 40 Tbps (5 TB/s)
- Heterogeneous commodity computing system
  - Offline-like algorithms
  - Under evaluation the possibility to use accelerators (GPUs or FPGAs)
- New DAQ infrastructure:
  - readout, dataflow, network, online software



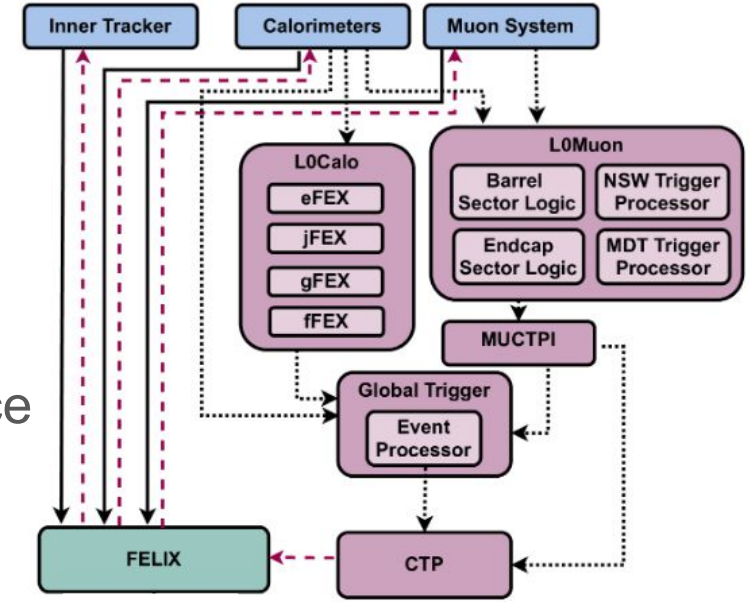
Readout

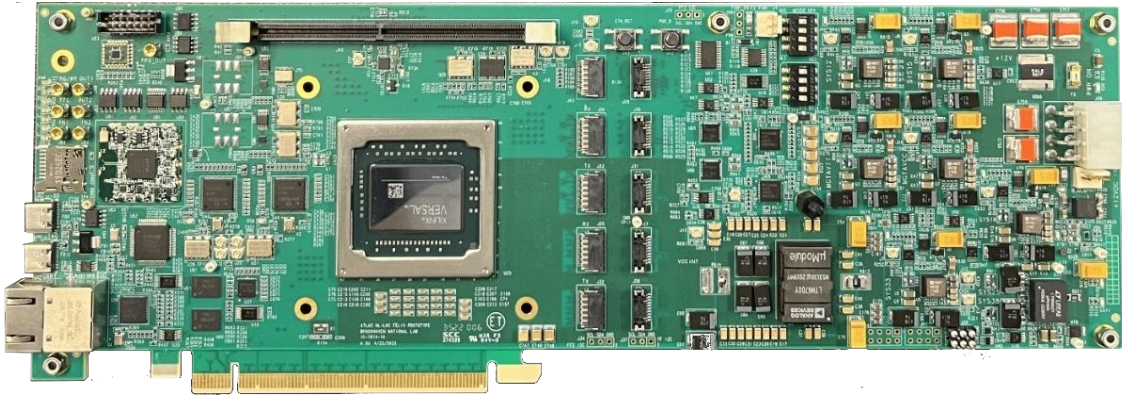
- **F**ront-**E**nd **LI**nk e**X**change
  - PC-based gateway
  - hosting FPGA-based PCIe I/O cards
- FELIX interfaces
  - custom optical links to/from front-end
  - to/from commodity switched network
- Partially deployed in Run 3
  - for new or already upgraded detectors
- To be upgraded for Run 4
  - FLX-182 prototype



Readout

- FLX-182 prototype (FPGA/SoC)[1]
  - Xilinx XCVM1802, PCIe gen4
  - 24 links up to 25 Gb/s + TTC interface
- Functionality tests successful
  - Hardware and firmware functions
  - Optical links and PCIe transmission
  - Integration w/ ATLAS Global Trigger

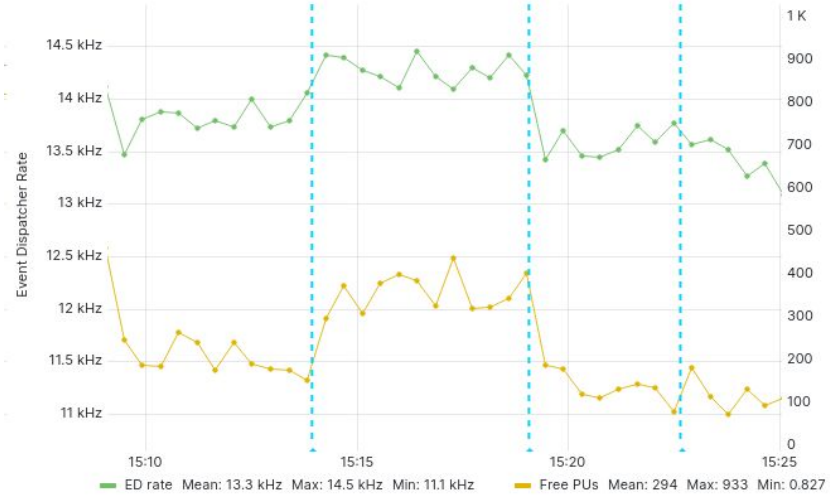


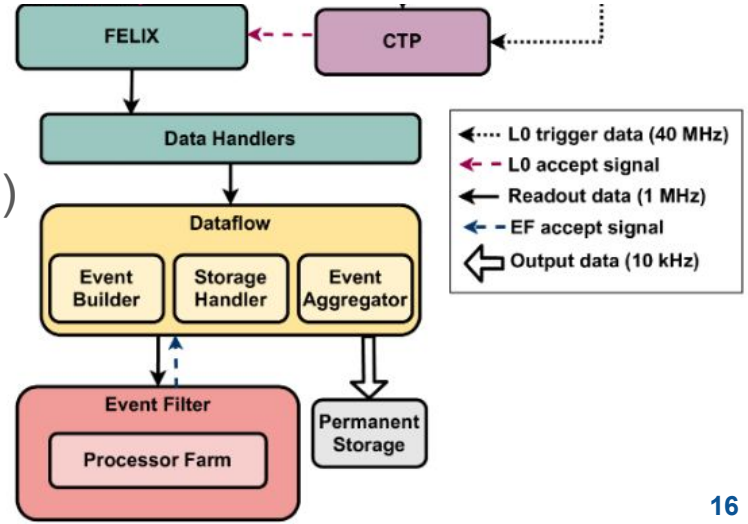


[1] More details in Joaquin Hoya presentation, Thursday 2:45 pm [link]

Dataflow and networking

- Dataflow provides full events (from readout) to EF and storage
- Completing a SW prototype
  - Based on Run 3 Dataflow
  - w/ new features and optimizations
  - Supporting expected rate: 12 kHz per rack (Assuming SW only architecture)
- Networking studies ongoing[1]
  - Investigating deep-buffer switches
  - Simulation Models

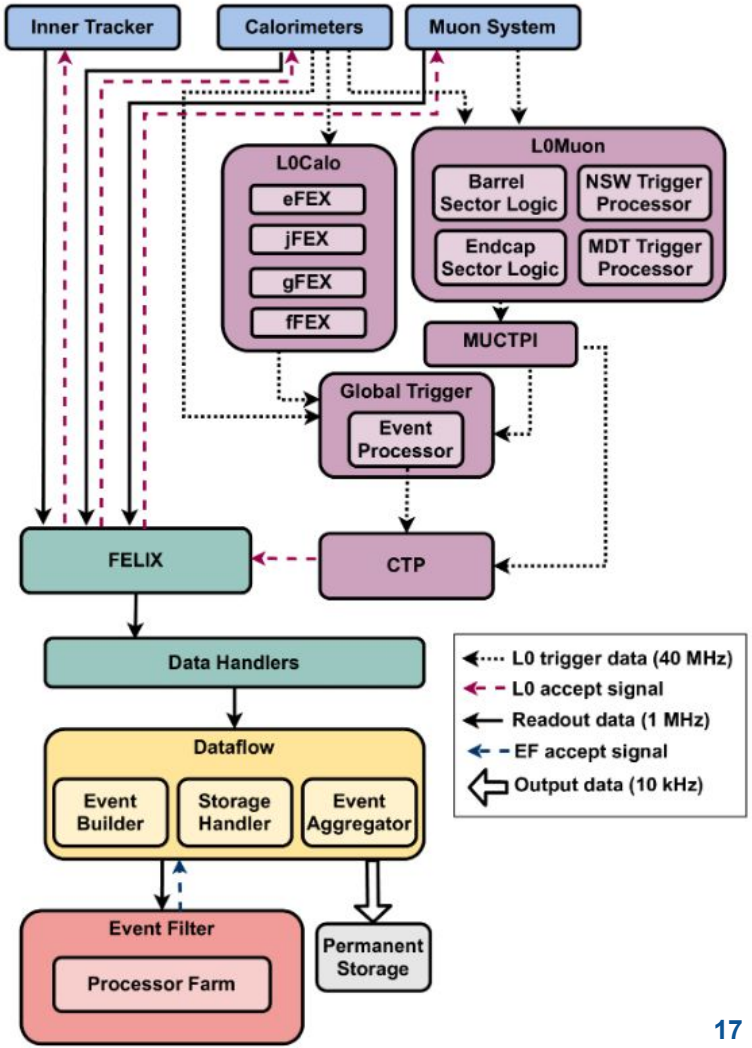




[1] More details in Eukeni Pozo Astigarraga presentation, Tuesday 4:45 pm [link]

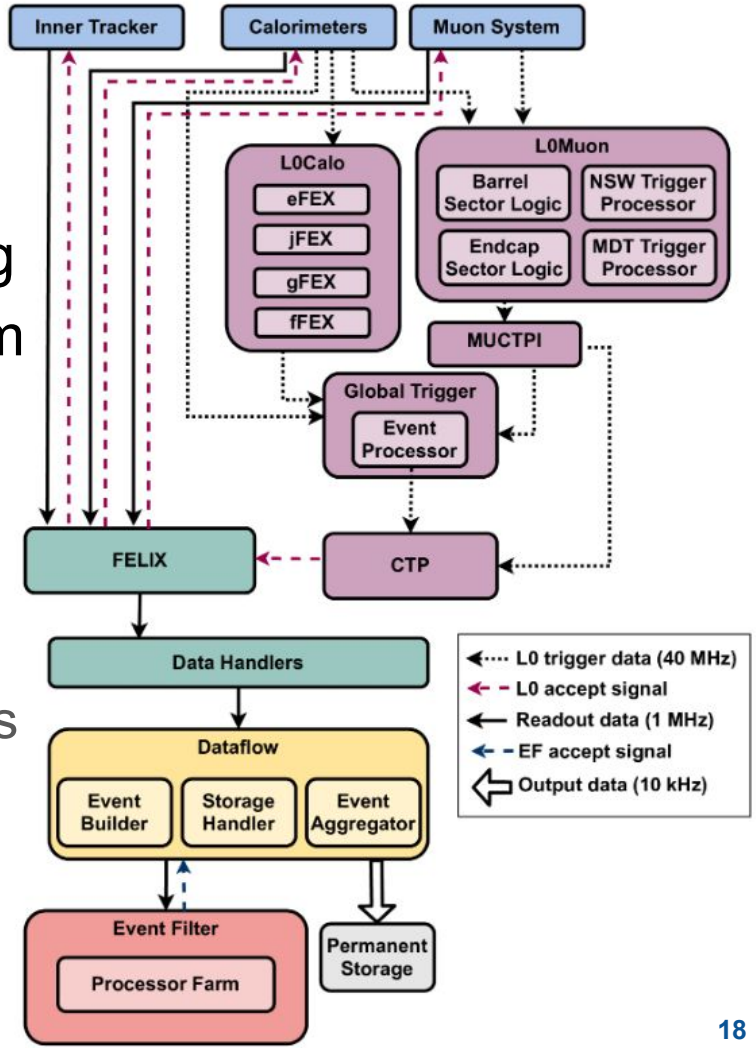
Dataflow and networking

- Persistent-storage buffer system
  - Complementary dataflow option w.r.t. Run 3 application-based design
  - Developed using DAOS
    - an open-source high-performance distributed storage system
  - Using Intel's high-end NVMes and persistent memories
- Prototype being tested
  - Viability depends on the evolution of storage technology



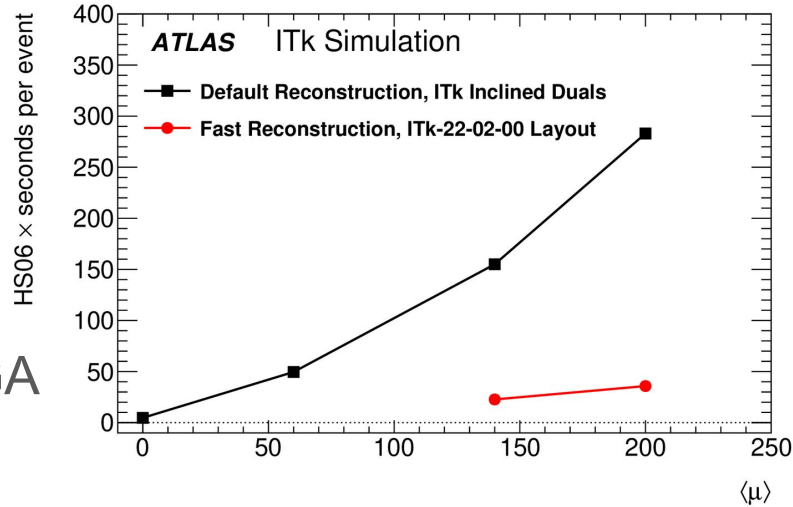
Online Software

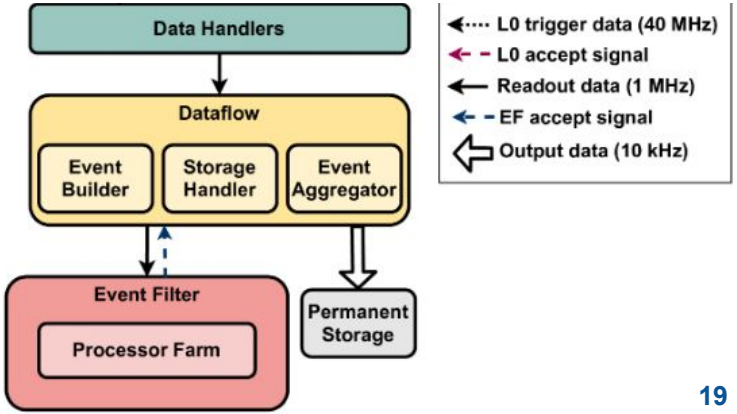
- Responsible of configuring, controlling and monitoring the whole DAQ system
- Prototype EF farm orchestrator based on Kubernetes
  - Open-source orchestrator platform that automates deploying, managing and scaling containerized applications
  - Tests performed on Run 3 farm
- Started integration into the Run Control Software framework



Event Filter

- Commodity hardware:
  - CPU (7.8/11.4 MHS06 for Run 4/5)
  - Possibly w/ accelerators: GPU, FPGA
- Preliminary feasibility studies*
  - CPU showed x8 speed-up
  - Use of GPU/FPGA looked promising
- First demonstrators started
  - tracking, muon, calorimeter
- Technology decision about the use of accelerators in 2025





* For Technical Design Report Amendment (2021)

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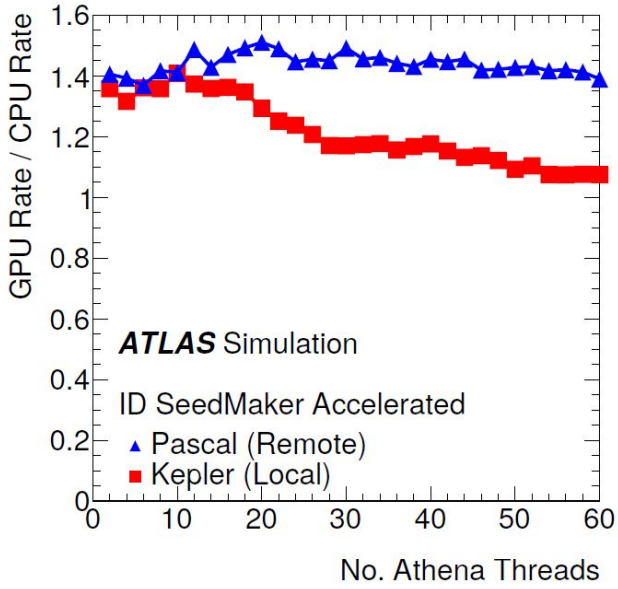
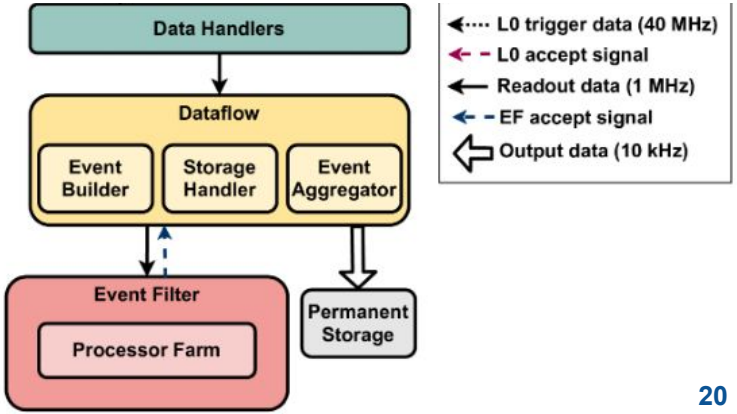
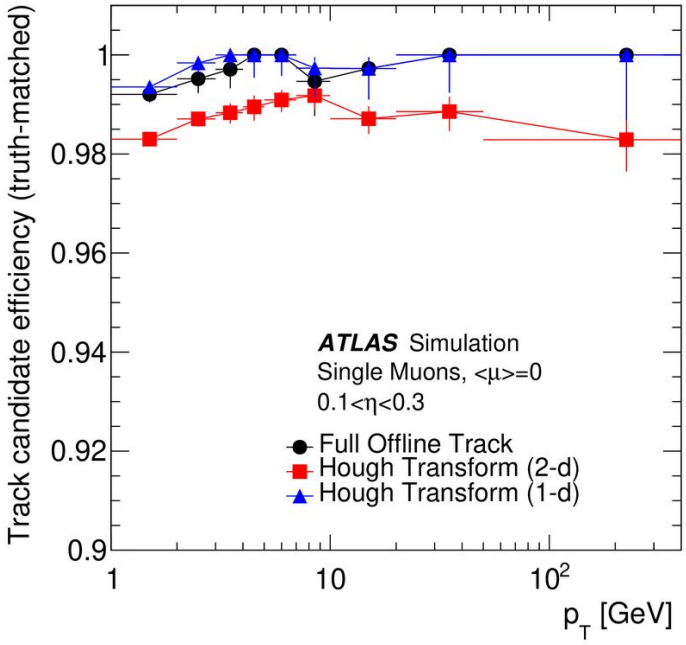




* For Technical Design Report Amendment (2021)

EF tracking

- Many ongoing FPGA & GPU studies
  - for track seeding, pattern recognition, track fitting, ambiguity removal
- Exploring use of High Level Synthesis
  - Hough transforms with FPGAs[1] and Graph Neural Network[2]

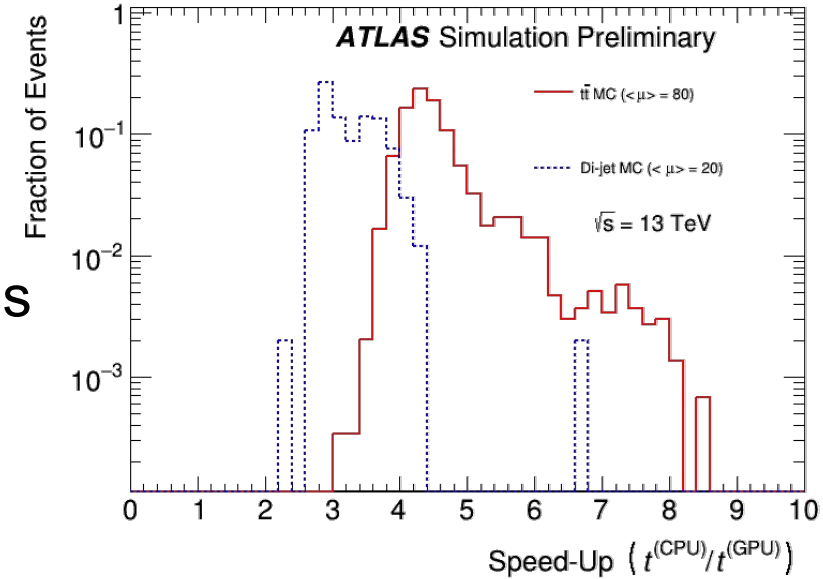


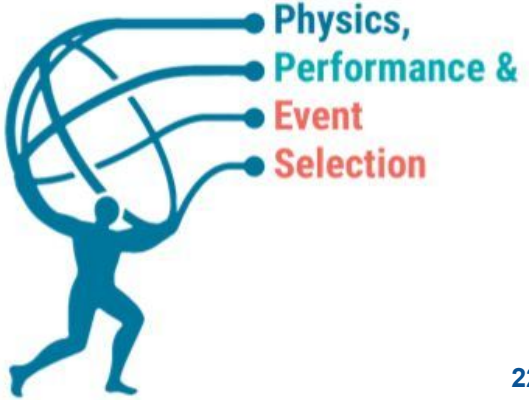
- Plan to use **A**cts **C**ommon **T**racking **S**oftware
  - Experiment independent toolkit for track reconstruction
  - Support for accelerators and heterogeneous options

[1] More details in Abraham Kahn poster [link]
[2] More details in Sebastian Dittmeier presentation, Tuesday 2:30 pm [link]

EF Calo and PPES

- EF Calo: demonstrated topological Cell Clustering w/ GPUs
  - speed-up w.r.t CPU (1st version)
    - ~3.5 for di-jets <μ> ~20
    - ~5.5 for tt at <μ> ~ 80
  - exploring FPGAs alternatives
- Physics, Performance & Event Selection group coordinates
  - simulation, performance and trigger menu development for Level-0 and EF algorithms





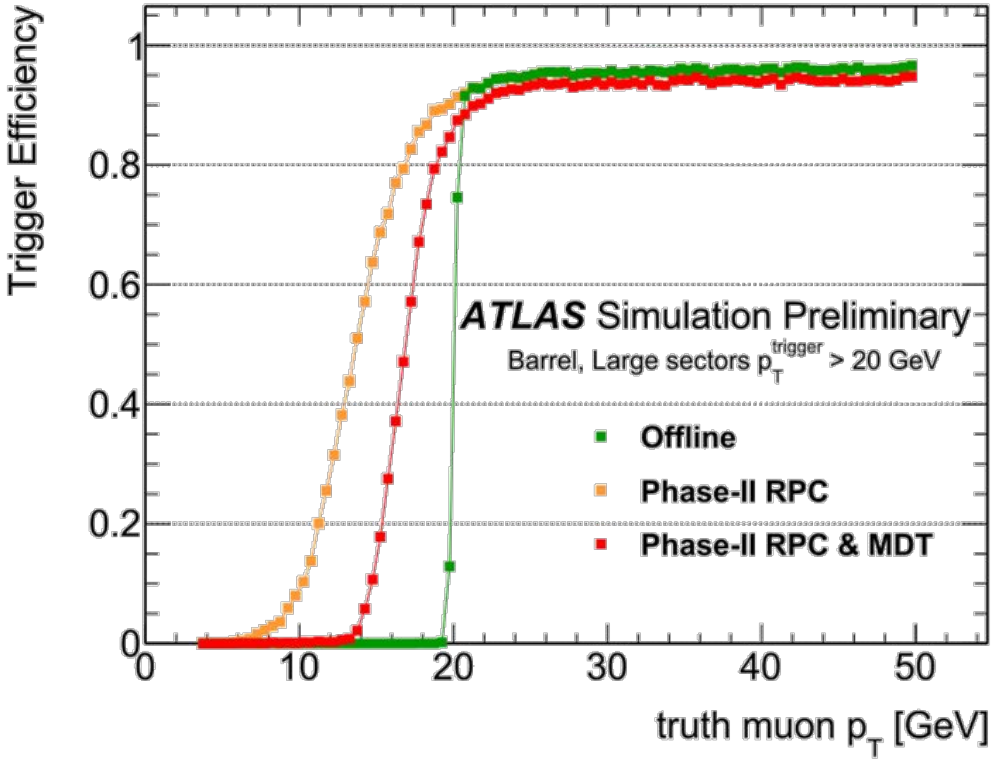
Conclusion

- Upgrades based on a mix of commodity and custom solutions
  - Most projects already passed many reviews
  - Prototypes available for many projects
- Level-0 trigger
  - focus on integration with the many interfaces
- Readout, Dataflow, Network, online SW
  - testing prototypes: 1st FELIX prototype, dataflow prototypes, container-based prototype farm orchestration
- Event Filter
  - investigating accelerator options, technology decision in 2025

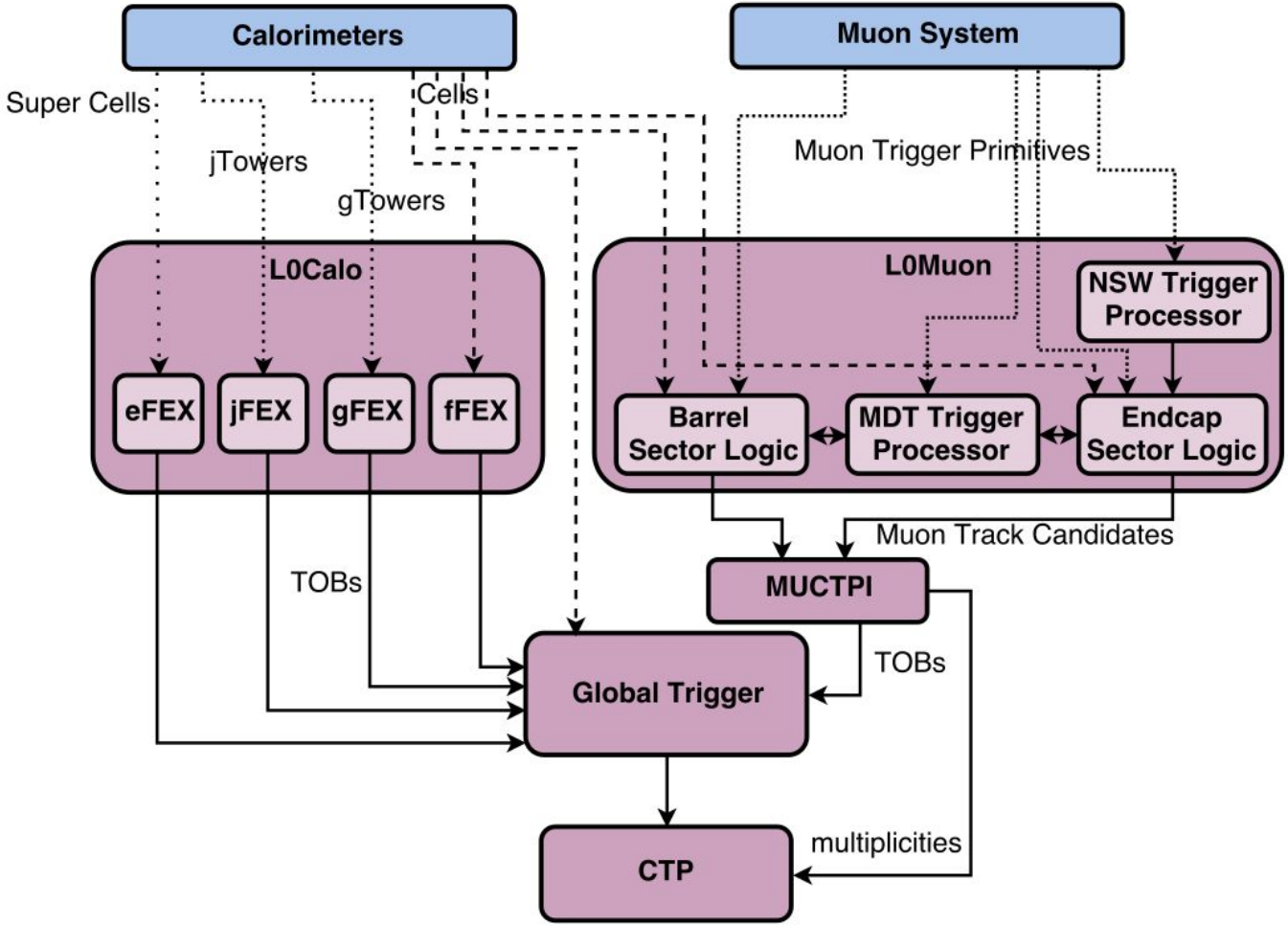
Backup

L0 Muon: MTD trigger processor

- Use MDT hits to improve the muon track candidate parameters, coming from the RPC and TGC Sector Logic (SL) boards.
  - Refined candidates are then sent back for the final trigger decision

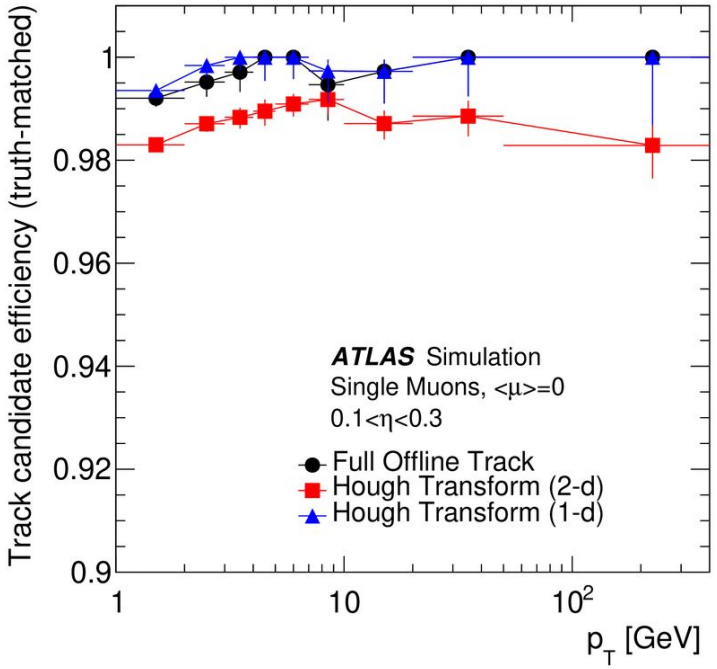


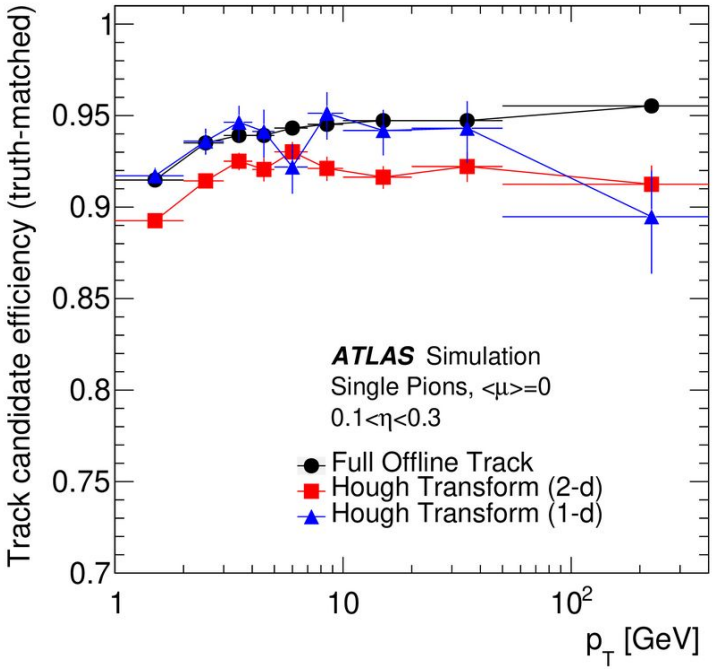
Level 0


Calorimeters
Muon System
Super Cells
Cells
jTowers
gTowers
Muon Trigger Primitives
L0Calo
L0Muon
NSW Trigger Processor
eFEX
jFEX
gFEX
fFEX
Barrel Sector Logic
MDT Trigger Processor
Endcap Sector Logic
Muon Track Candidates
TOBs
MUCTPI
TOBs
Global Trigger
multiplicities
CTP

EF: FPGA Hough transform efficiency

- Single particles (muons/pions), barrel region, no pile-up,





Event Filter

- Regional tracking in Regions of Interest identified at Level-0
  - to verify the presence of high-pT tracks in single lepton triggers
  - to associate objects to a common vertex
- Run full-scan tracking at reduced rate
  - after regional tracking for jets & E_T^{miss}
- Large radius tracking for exotics
  - focuses on tracks with high impact parameters like those resulting from the decays of Long Lived Particles