



# Orbit Builder for CMS Phase-2 at CERN

Presenter: Rafał Dominik Krawczyk, on behalf of the CERN CMS DAQ group Primary authors: Rafał Dominik Krawczyk-Rice University, Andrea Petrucci-UCSD Email: rafal.dominik.krawczyk@cern.ch

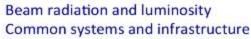
26th International Computing in High Energy & Nuclear Physics Conference 9 May 2023

# CMS in Phase-2

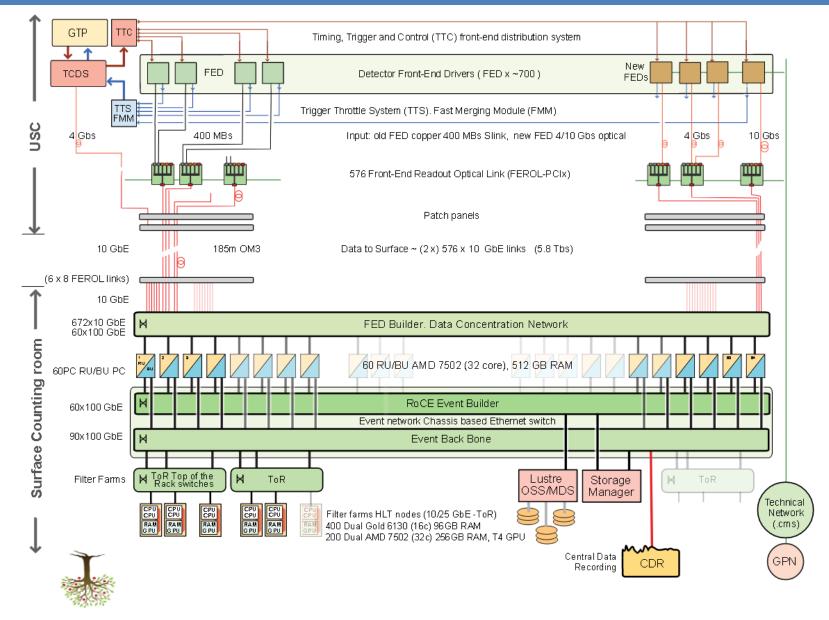
Barrel EM calorimeter Trigger/HLT/DAQ Muon systems **New Endcap Calorimeters** New Tracker

• One of four main LHC experiments

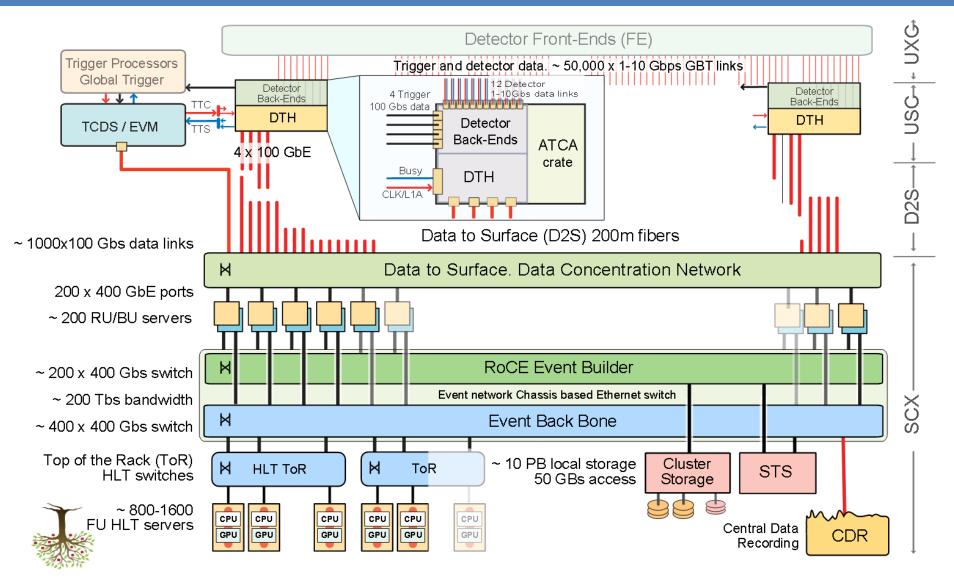
- Upgrade for HL-LHC luminosity increase
  - Run 3 (now)  $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
  - Run 4 (2029)  $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
  - Run 5 (2035)  $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
- Phase-2 DAQ:
  - Event size  $\rightarrow$  from 2 MB to 8.4 MB
  - L1 Trigger acceptance rate  $\rightarrow$  from 100 kHz to 750 kHz
  - HLT accept rate  $\rightarrow$  1 kHz to 7.5 kHz
  - Ready in 2025 for Run 4 commissioning



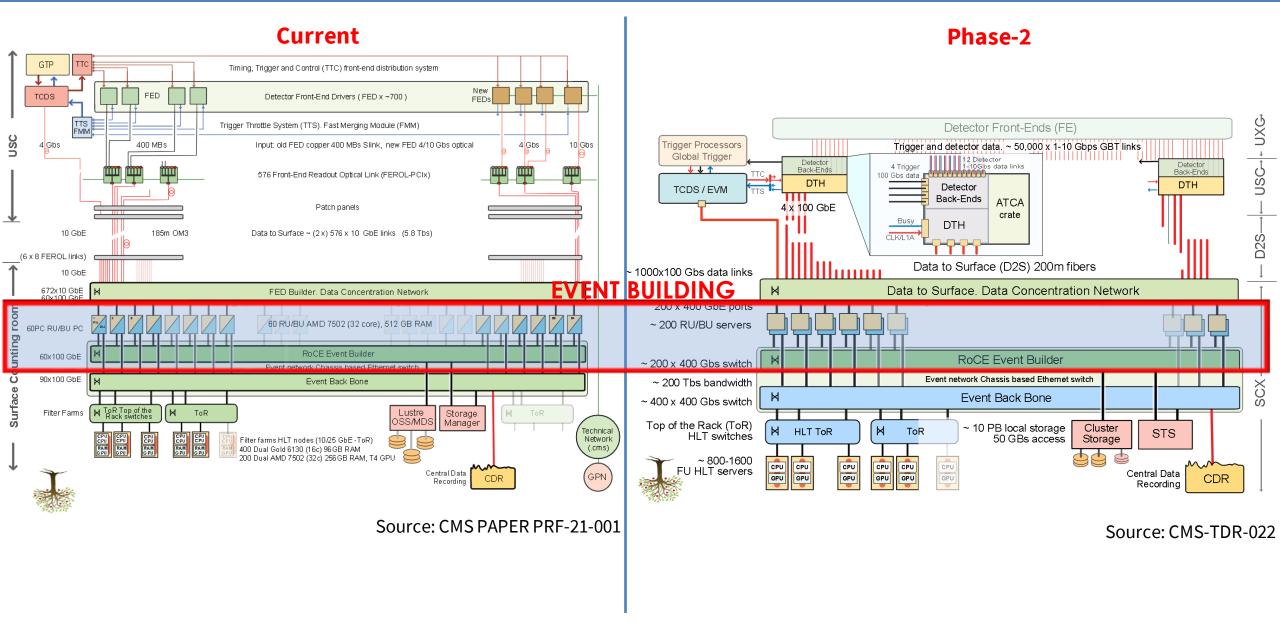
### Current DAQ architecture



### Phase-2 DAQ architecture

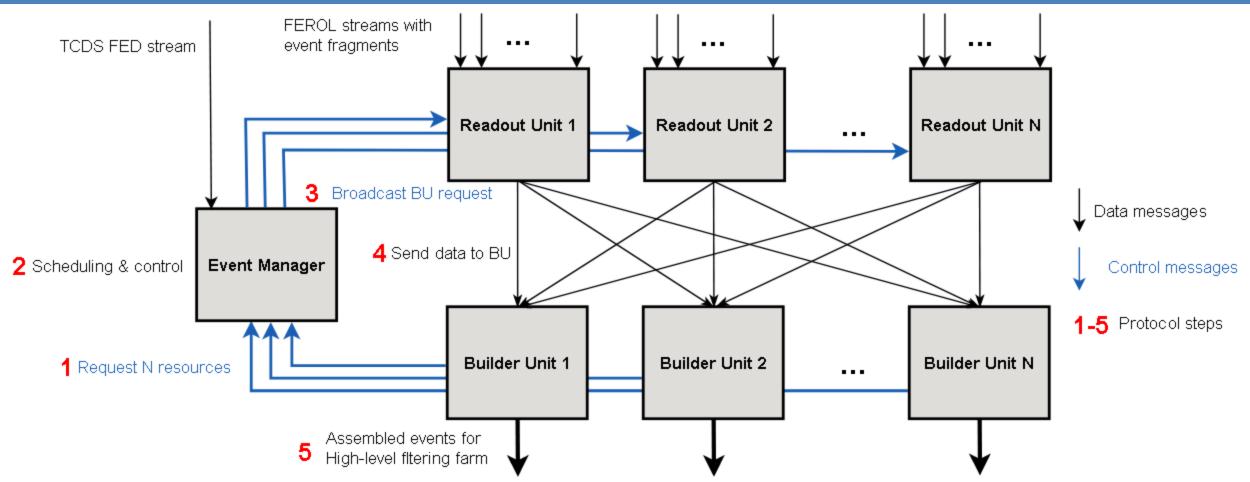


#### Current versus Phase-2 DAQ architecture



#### Orbit Builder for CMS Phase-2 at CERN

# CMS event building



#### Primary objective $\rightarrow$ assembling events from their scattered fragments

- Phase-2 DAQ:
- Event size  $\rightarrow$  from 2 MB to 8.4 MB
- L1 Trigger acceptance rate  $\rightarrow$  from 100 kHz to 750 kHz
- HLT accept rate  $\rightarrow$  1 kHz to 7.5 kHz

Orbit Builder for CMS Phase-2 at CERN

Challenge for Phase-2  $\rightarrow$  increased workloads:

- Total builder network traffic  $\rightarrow$  from 1.6 Tb/s to 51 Tb/s
- Total servers from ~60 to ~200 servers
- High-performance software, quasi-real-time lossless data taking

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CHEP 2023,9 May 2023

#### Phase-2 event versus orbit

#### Events in DAQ

- Corresponds to a **collision** selected by L1 trigger
- Full event size  $\rightarrow$  up to 8.4 MB
- Event rate  $\rightarrow$  up to 750 kHz

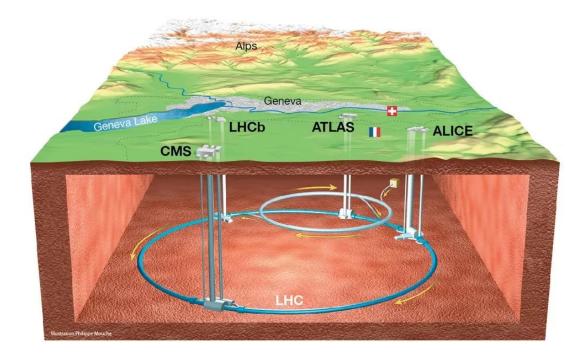
# CMS Experiment at the LHC, CERN Data recorded: 2018-Nov-12 08:36:52.866176 GMT Run / Zent / LS: 326586 / 2491137 / 6

#### CMS-PHO-EVENTS-2018-010-19

Orbit Builder for CMS Phase-2 at CERN

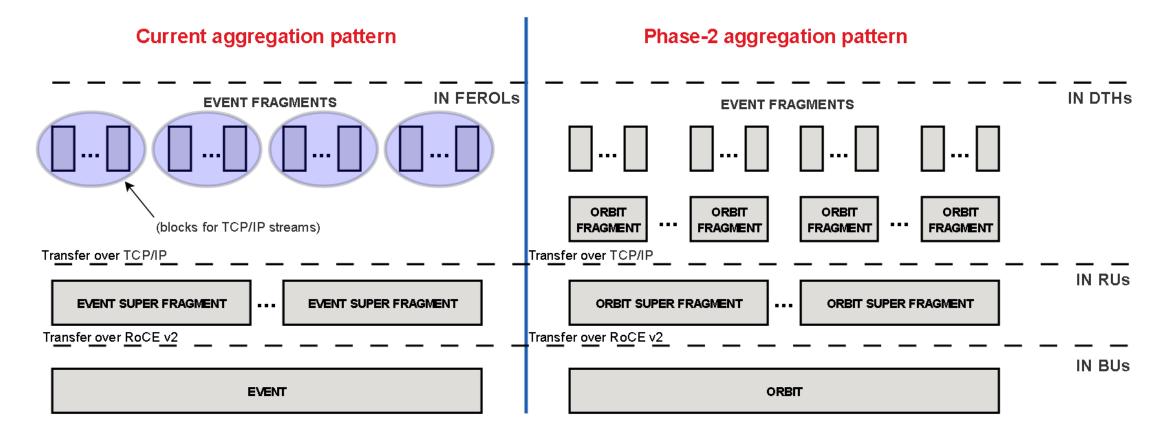
#### Orbits in DAQ

- A collection of events during one LHC orbit
- Orbit fragment size  $\rightarrow$  50-250 kB
- Orbit rate  $\rightarrow$  11.2 kHz
- 67 events per orbit on average



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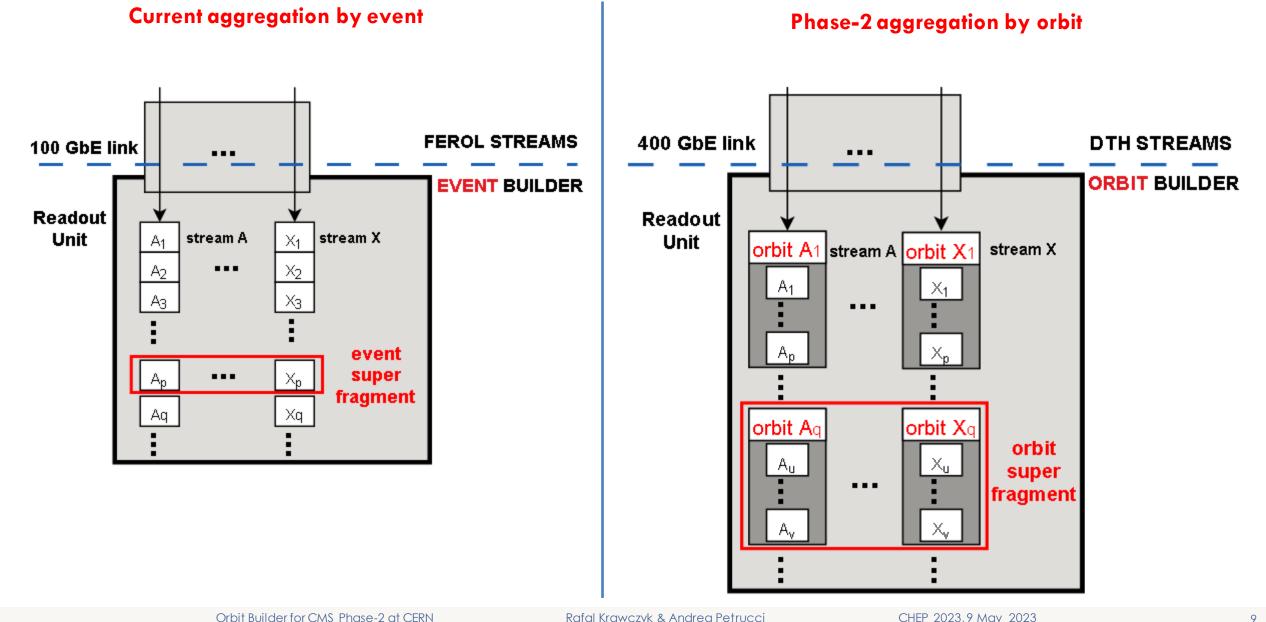
## Phase-2 orbit builder data aggregation



#### Why selected orbits for Phase-2:

- More data per transmission to RU
- More data per RU-BU transmissions
- Less control messages in the event builder

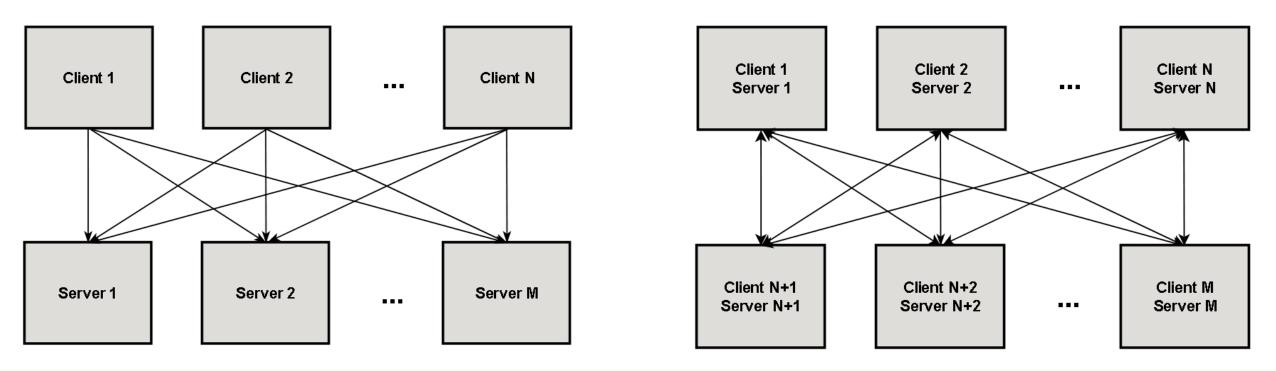
### Event builder versus orbit builder



### Orbit builder software study

Developed the **pipestream** C++benchmark based on the **XDAQ 2<sup>nd</sup> generation** online software

- Emulates Event Builder network traffic
- **REST** and **finite-state machine** for the runtime control
- High-performance library supporting RDMA over Converged Ethernet (RoCE)
- YAML for bootstrap configuration
- See the related CHEP talk  $\rightarrow$  "Towards a container-based architecture for CMS data acquisition" by Dainius Šimelevičius
- Runs standalone or in Kubernetes
- Scheduled data sending over network between different nodes from clients to servers
- Throughput of clients and servers periodically probed through REST

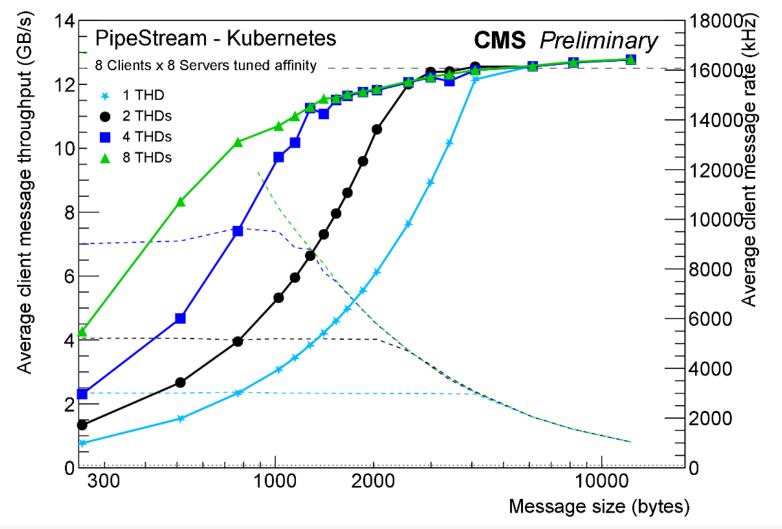


### Performance tests

- Tuned parameters:
  - maximal message size
  - buffer size per connection
  - burst size
  - threads number and affinity
  - memory affinity
- Used the existing DAQ Run 3 infrastructure with 100 Gigabit Ethernet
- Measured nodes performance for the all-to-all, CMS event building-like traffic
- One orchestrator and 14 test nodes

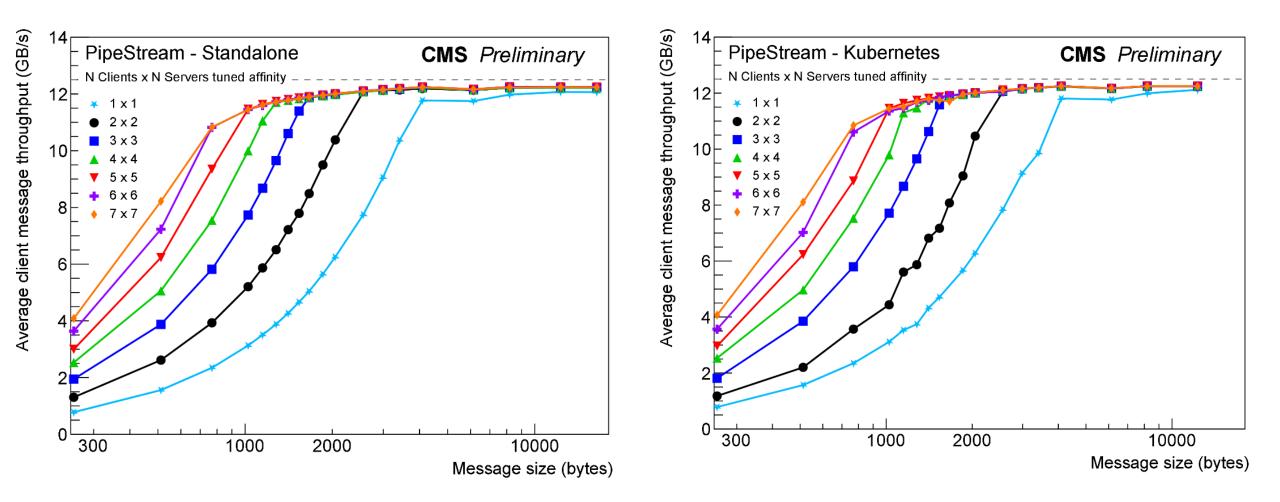
### Message rate and throughput over small system

- A **folded** configuration with client and servers sharing nodes
- Checked performance for small message sizes
- Measured message rates



### Standalone versus Kubernetes

- A configuration with client and servers on separate node
- Checked performance for CMS-like message sizes
- No performance penalty in K8s



- Proof of concept  $\rightarrow$  XDAQ 2<sup>nd</sup> generation framework for the CMS Phase-2 event building use-case
- Initial results good enough to proceed with the development
- Next step  $\rightarrow$  developing into a fully-functional event builder with the presented software platforms



#### Primary authors:

- Krawczyk, Rafał Dominik (RICE)
- Petrucci, Andrea (UCSD)

#### Co-Authors:

Amoiridis, Vassileios (CERN); Behrens, Ulf (RICE); Bocci, Andrea (CERN); Branson, James (UCSD); Brummer, Philipp (CERN); Cano, Eric (CERN); Cittolin, Sergio (UCSD); Da Silva Almeida Da Quintanilha, Joao (CERN); Darlea, Georgiana-Lavinia (MIT); Deldicque, Christian (CERN); Dobson, Marc (CERN); Gigi, Dominique (CERN); Glege, Frank (CERN); Gomez-Ceballos, Guillelmo (MIT); Gutic, Neven (CERN); Hegeman, Jeroen (CERN); Izquierdo Moreno, Guillermo (CERN); Kartalas, Miltiadis (CERN); (RICE); Li, Wei (RICE); Long, Kenneth (MIT); Meijers, Frans (CERN); Meschi, Emilio (CERN); Morovic, Srecko (UCSD); Orsini, Luciano (CERN); Paus, Christoph (MIT); Pieri, Marco (UCSD); Rabady, Dinyar Sebastian (CERN); Racz, Attila (CERN); Sakulin, Hannes (CERN); Schwick, Christoph (CERN); Simelevicius, Dainius (Vilnius University); Vazquez Velez, Cristina (CERN); Zejdl, Petr (CERN); Zhang, Yousen (RICE); Zogatova, Dominika (CERN)

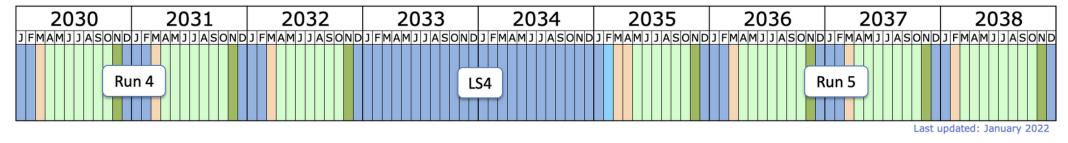
Supplementary slides

#### **Worker Nodes**

CPUs	2 x Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
RAM	256 Gib DDR4, 2666 MT/s
NICs	MellanoxConnect X-6 in Ethernet mode

Test Network			
ports	14 x 100 Gbps		
Switch	Juniper QFX10000-30C line card (100Gbps)		
Chassis	QFX10008		



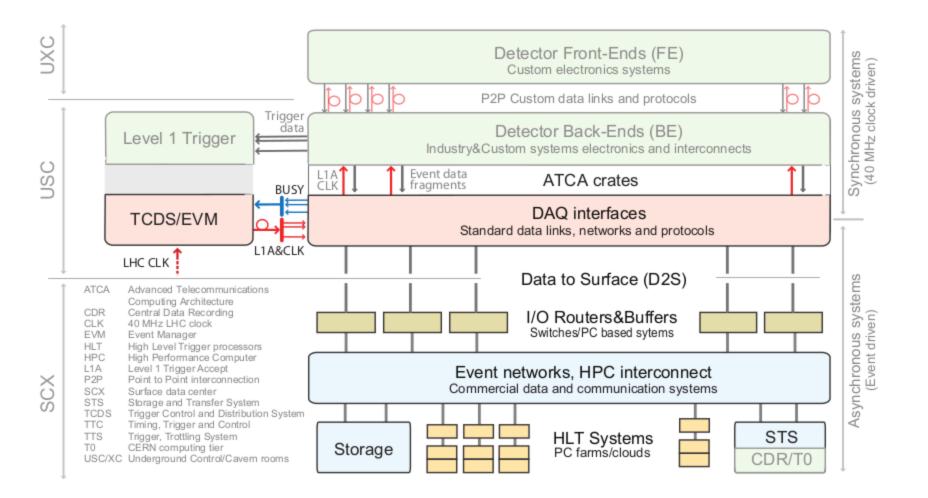




Shutdown/Technical stop Protons physics Ions Commissioning with beam Hardware commissioning/magnet training

Source CERN :Longer term LHC schedule

### Conceptual design of Phase-2 CMS DAQ



Source: CMS-TDR-022

	LHC	HL-LHC	
CMS detector	Phase-1	Phase-2	
Peak $\langle PU \rangle$	60	140	200
L1 accept rate (maximum)	100 kHz	500 kHz	750 kHz
Event Size at HLT input	2.0 MB <sup>a</sup>	6.1 MB	8.4 MB
Event Network throughput	1.6 Tb/s	24 Tb/s	51 Tb/s
Event Network buffer (60 s)	12 TB	182 TB	379 TB
HLT accept rate	1 kHz	5 kHz	7.5 kHz
HLT computing power <sup>b</sup>	0.7 MHS06	17 MHS06	37 MHS06
Event Size at HLT output <sup>c</sup>	1.4 MB	4.3 MB	5.9 MB
Storage throughput <sup>d</sup>	2 GB/s	24  GB/s	51 GB/s
Storage throughput (Heavy-Ion)	12 GB/s	51 GB/s	51 GB/s
Storage capacity needed (1 day <sup>e</sup> )	0.2 PB	1.6 PB	3.3 PB

<sup>a</sup>Design value.

<sup>b</sup>Does not include Data Quality Monitoring.

<sup>c</sup>Actual compression factor for Phase-1. For Phase-2 same factor is assumed, see Section 6.2.11.

<sup>*d*</sup>The storage throughput is defined as the effective throughput with concurrent recording and transfer. The throughput required is determined by the HLT output event size and the additional output streams, see Section 6.2.11.

<sup>e</sup>Assuming an LHC duty cycle, i.e. the fraction of time spent in stable colliding beams, of 75 %.

#### Source: CMS-TDR-022

Component	Technology	Estimated quantity
DTH-400 and DAQ-800 boards <sup>a</sup>	ATCA custom board	250 boards
TCDS2 custom boards	ATCA custom board	16 boards
DAQ D2S links	100-GBASE-CWDM4 <sup>b</sup>	900 links
Data Concentrator Network	Chassis-based <sup>c</sup> switch	1100 ports <sup>d</sup>
Event Builder Nodes <sup>e</sup>	Rack-mount 2U server	200 servers
Event Builder Network	Chassis-based	200 ports
	400 Gb/s switch	
Event Backbone Network	Chassis-based	400 ports
	400 Gb/s switch	
ToR switch	Rack-mount <sup>f</sup> switch	42 ToR switch
		(approx. 5×50 ports)
HLT servers <sup>g</sup>	Rack-mount 1U(2U)	1600(840) servers
	server with 2(6) GPU	
Storage System	Network-attached	102 GB/s bandwidth $^{h}$
	storage appliance	3.3 PB total storage

<sup>*a*</sup>DTH-400 boards with DAQ and TCDS functionality and DAQ-800 boards with DAQ functionality only. <sup>*b*</sup>Transceiver, optical module and single-mode optical fibers linking USC to SCX.

<sup>c</sup>Switch with 100 Gb/s and 400 Gb/s line cards.

<sup>d</sup>900 ports 100 Gb/s and 200 ports 400 Gb/s.

<sup>e</sup>A server capable of  $\approx 1 \text{ Tb/s}$  concurrent input and output is assumed (requires PCIe Gen5).

<sup>f</sup>400 Gb/s uplinks from Event Backbone and 100 Gb/s downlinks to HLT servers.

<sup>g</sup>The values in parentheses are for Run-5.

<sup>h</sup>providing 51 GB/s throughput (read+write).

#### Source: CMS-TDR-022

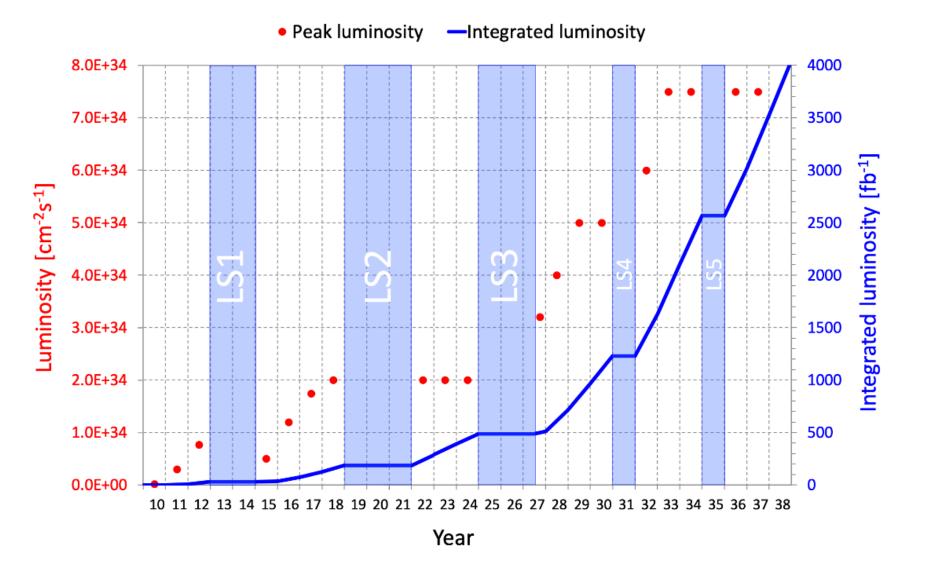
## Run 1-3 table

	Run 1	Run 2	Run 3
Event building rate <i>pp</i>	100 kHz	100 kHz	100 kHz
Event size <i>pp</i> <sup><i>a</i></sup>	1 MB	2 MB	2 MB
Read-out links S-LINK64 (copper) 400 MB/s <sup>d</sup>	636 <sup>b</sup>	$575^b 532^c$	$528^{b}$
Read-out links optical <sup><math>i</math></sup> 6 Gb/s <sup><math>d</math></sup>	-	55 <sup>c,e</sup>	$55^{b,e}$
Read-out links optical <sup>i</sup> 10 Gb/s	-	$60^b 167^c$	176 <sup>b</sup>
FED Builder network technology	Myrinet	Ethernet	Ethernet
FED Builder network speed	2 rails of 2.5 Gb/s	10 & 40 Gb/s	10 & 100 Gb/s
Event builder # of readout units	640	108 <sup>c</sup>	$50^{f}$
Event Builder network technology	Ethernet	Infiniband	Ethernet RoCE v2 <sup>j</sup>
Event Builder link speed	1-3 rails of 1 Gb/s	56 Gb/s	100 Gb/s
Event Builder parallel slices	8	1	1
Event Builder network throughput	1.0 Tb/s	1.6 Tb/s	1.6 Tb/s
Event Builder # of builder units	1260 <sup>g</sup>	73 <sup>c</sup>	$50^{f}$
BU RAM disk buffer	none	16 TB	15 TB
HLT # of filter unit motherboards	$720^{b,g} \dots 1260^{c,g}$	$900^b$ $1084^c$	$200^{k}$
HLT # cores	$5.8k^b 13k^c$	$16k^b 31k^c$	$26k^{h,k}$
HLT computing power (MHS06)	$0.05^b \dots 0.20^c$	$0.34^b 0.72^c$	$0.65^{h}$
HLT # of NVIDIA T4 GPUs	-	- /	$400^k$
Storage system technology	16 SAN <sup>1</sup> systems	1 cluster file system	1 cluster file system
Storage system bandwidth write + read	2GB/s	9GB/s	30 GB/s
Storage system capacity	300 TB	500 TB	1.2 PB
Transfer System to Tier-0 speed	2×10Gb/s	$4 \times 40 \mathrm{Gb/s}$	$4 imes 100{ m Gb/s}$

<sup>*a*</sup>design value, <sup>*b*</sup>at the beginning of the run, <sup>*c*</sup>at the end of the run, <sup>*d*</sup>main data-taking configuration - excluding links from partition managers used for partitioned running, <sup>*e*</sup>54 links from mezzanines with optical SlinkExpress, <sup>*f*</sup> readout and builder unit running on same server ("folded event builder"), <sup>*g*</sup>filter and builder units running on same server, <sup>*h*</sup>not including GPU compute power, <sup>*i*</sup>SlinkExpress, <sup>*j*</sup>Remote DMA over Converged Ethernet, <sup>*k*</sup>ordered at the time of writing, <sup>*l*</sup>Storage-area network

#### Source: CMS PAPER PRF-21-001

### Runs luminosity timeline



Source: CMS-TDR-022