CLAS12 DAQ upgrade at high luminosity

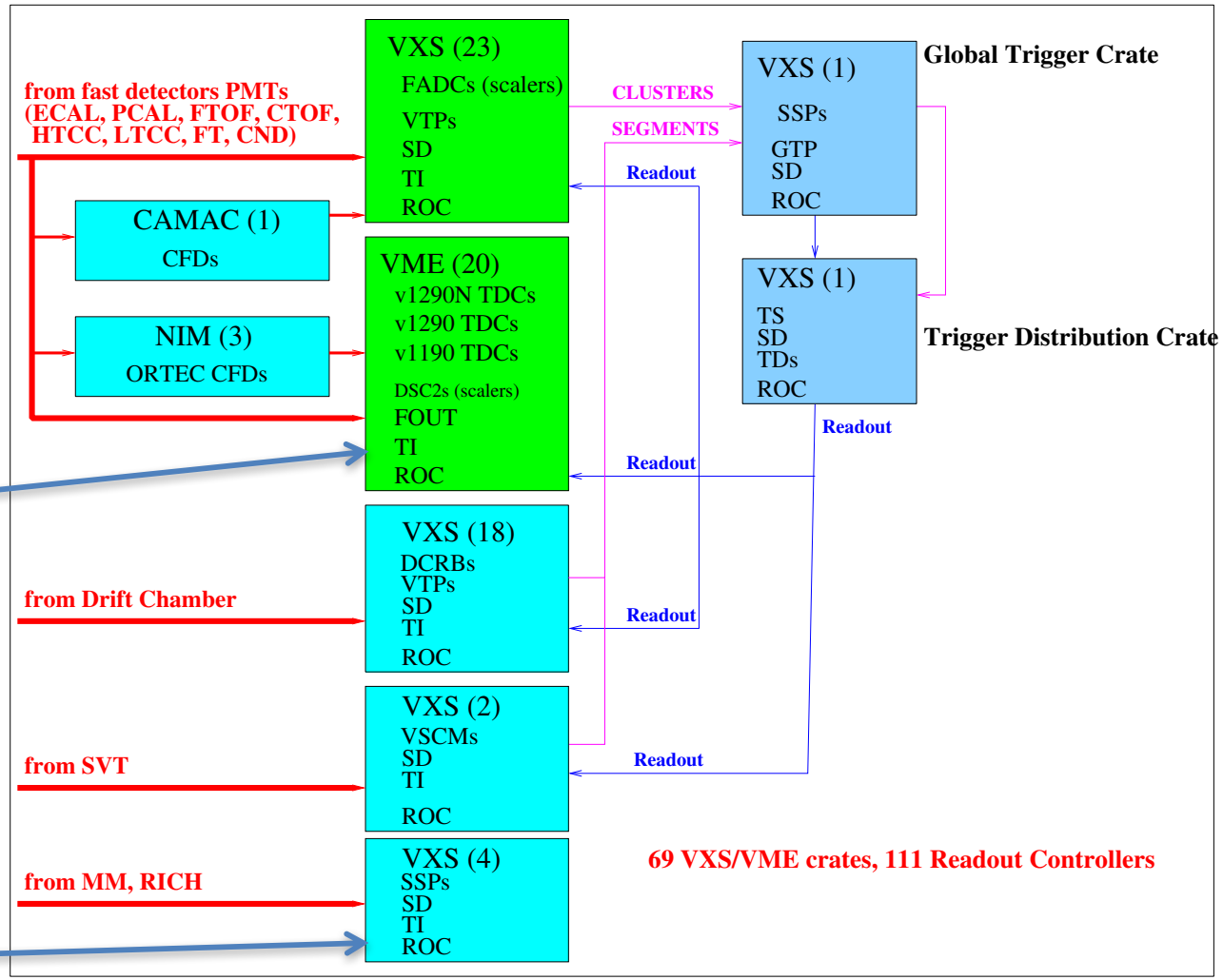
Sergey Boyarinov

CLAS Collaboration Meeting

June 2, 2021

1. Front End Electronics Upgrade
2. Trigger System Evolution

CLAS12 front-end upgrade for 100kHz (current event rate 30kHz)



Upgrade VME to VXS crates with VETROC TDCs

MM readout based on VMM3/Sampa ASIC

VME to VTP readout (in progress for SOLID)

VETROC TDC board

Channel counts:
- 64 channels on VETROC base; plus
- 64 channels on Mezz. Cards; plus
- 64 channels via VME P2/backplane IO card.
  --Any-level differential (converted to LVTTL on board)

Power supply:
- VME: +5V, +12V -12V

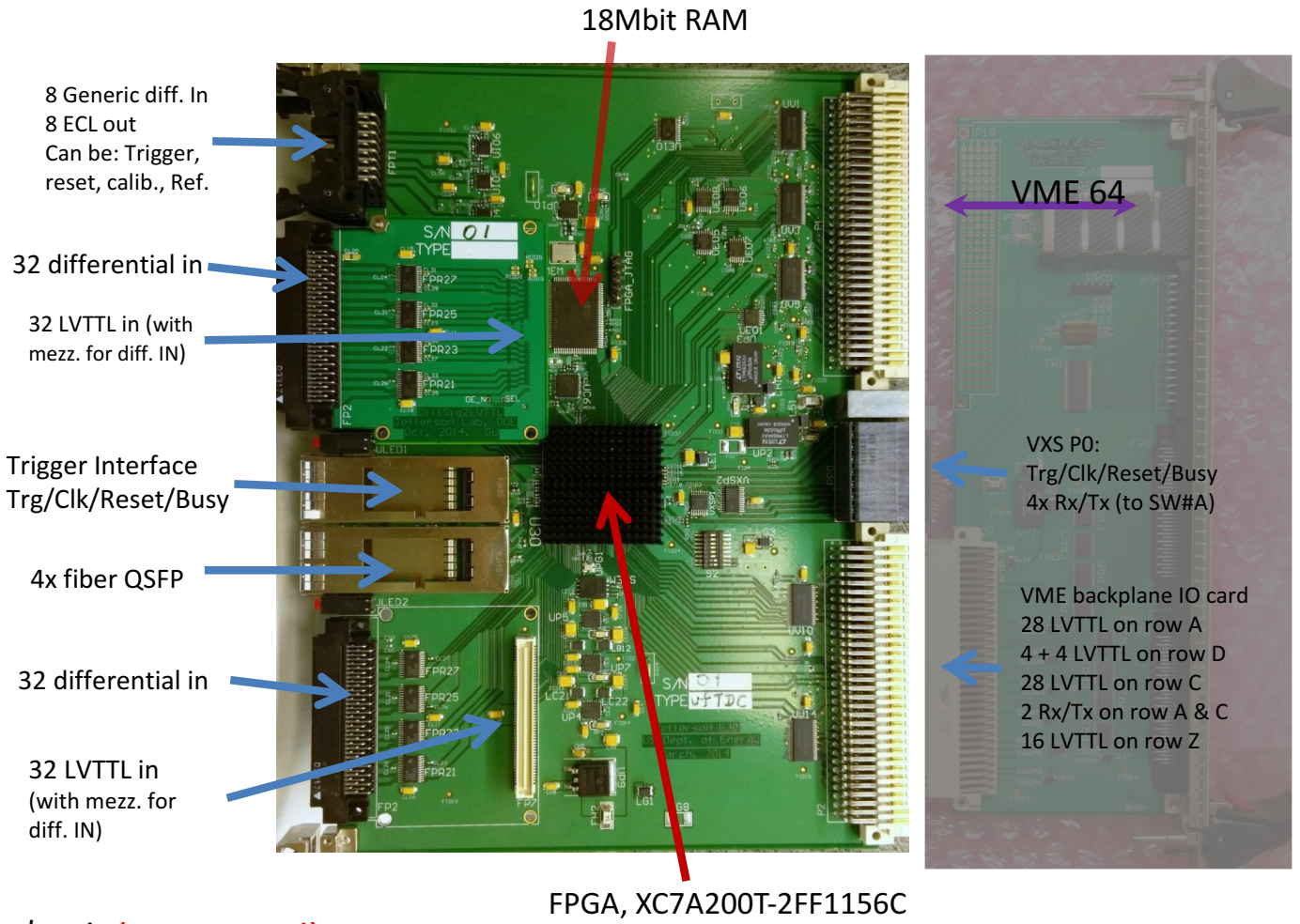
Data Readout:
- VME 64
- VXS P0
- QSFP front panel

Slow Controls(FPGA loading, setting etc.):
- VME for slow control

Fast Controls inputs (trigger etc.):
- VXS P0 (VXS payload slot);
- QSFP front panel (like a TI);
- Generic input (8-pair) front panel connector.

Measurement precision:
- ~ 35 ps, limited by the 'LVTTL' conversion

Status:
- Triggered readout: ready (both the FPGA firmware and the VME software)
- Streaming readout: FPGA firmware is available, but needs be tested



Budget: 40 VETROCs x $2k = $80k (8 received)

Crates VME64X->VXS backplane upgrades – 8 x $6.5k = $52k (6 installed)

1 new VXS crate (CTOF-HTCC separation) with CPU, SD, TI = $20k

Connectors, cables - $10k

Total: $162k

MM readout based on VMM3 ASIC

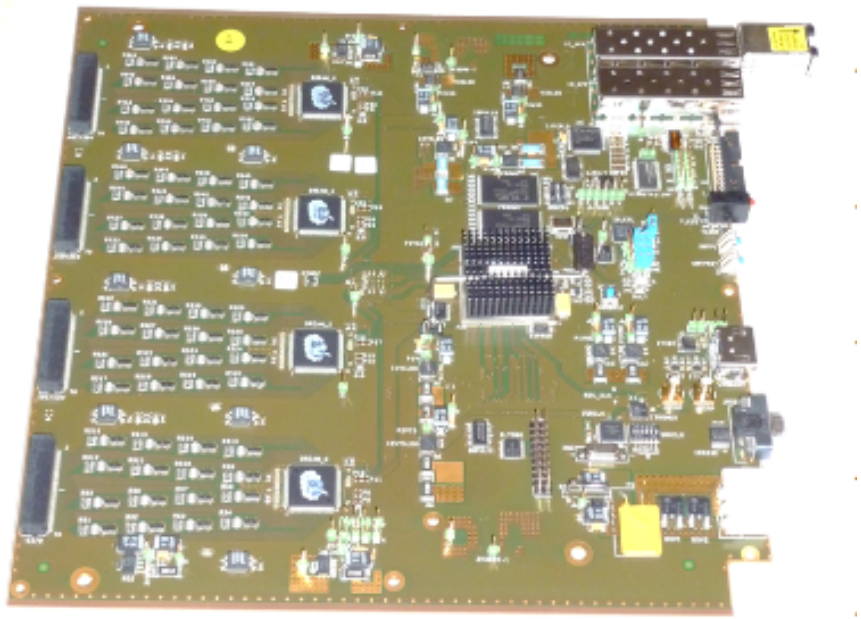


Figure 11: Photograph of the 512-channel Front-End Unit.

Notes:

1) **Trigger support would allow future expansion to support integration into trigger system. Requires a significant number of additional FPGA I/O, hence the increased FPGA costs for that configuration.**
2) **VMM3 noise & dynamic range still need to be confirmed suitable for use in CLAS12 MM use case**
3) **Backend may need a V**

FEU Replacement (DREAM -> VMM3A) Cost Estimate

- 512 channels per board (8x DREAM -> 8x VMM3A)
- 12 FEU (FMT) + 36 (BMT) => 48 FEU boards needed
  (need to double check this is exactly right)
- 48 * 8 = 384 VMM3 ASICs
- Plan to use same detector connector and readout fiber (so this upgrade will only replace these boards). VTP will be required to bypass VME readout to achieve high performance: 10GbE readout with VTP would support full MM readout @ 100kHz with ~15% occupancy (assuming 32bit per hit)

- Components
  - FPGA (if 6bit trigger path implemented): $1,000
  - FPGA (if only readout path implemented): $350
  - Connectors: $50
  - Fiber transceiver: $80
  - PCB: $300
  - Assembly: $500
  - ASIC (???): $800 (this assumes $100 per chip, online I've read $25 – probably depends on if we can piggy-back an order)
  - Misc (power, memory, etc): $200

- Unit cost (w trigger*, w/o trigger): $2930, $2280

- **Total (w trigger*, w/o trigger): $150k, $110k**

- Expecting VMM3-based card(s) in jlab for evaluation by the end of 2021
- Jlab investment into wafers production is under discussion

MM readout based on SAMPA ASIC

JLAB group (Ed Jastrzembski with colleagues) tested SAMPA V4 – based boards, conclusion: "We have successfully streamed and analyzed data from the SAMPA chip using both test pulse and GEM detector stimuli. We have made fundamental measurements on the SAMPA chip that complement those performed by the ALICE collaboration. We believe that the SAMPA chip and the elegant data transport mechanism employed in this system form an excellent basis for future streamed and triggered data acquisition systems at Jefferson Lab."

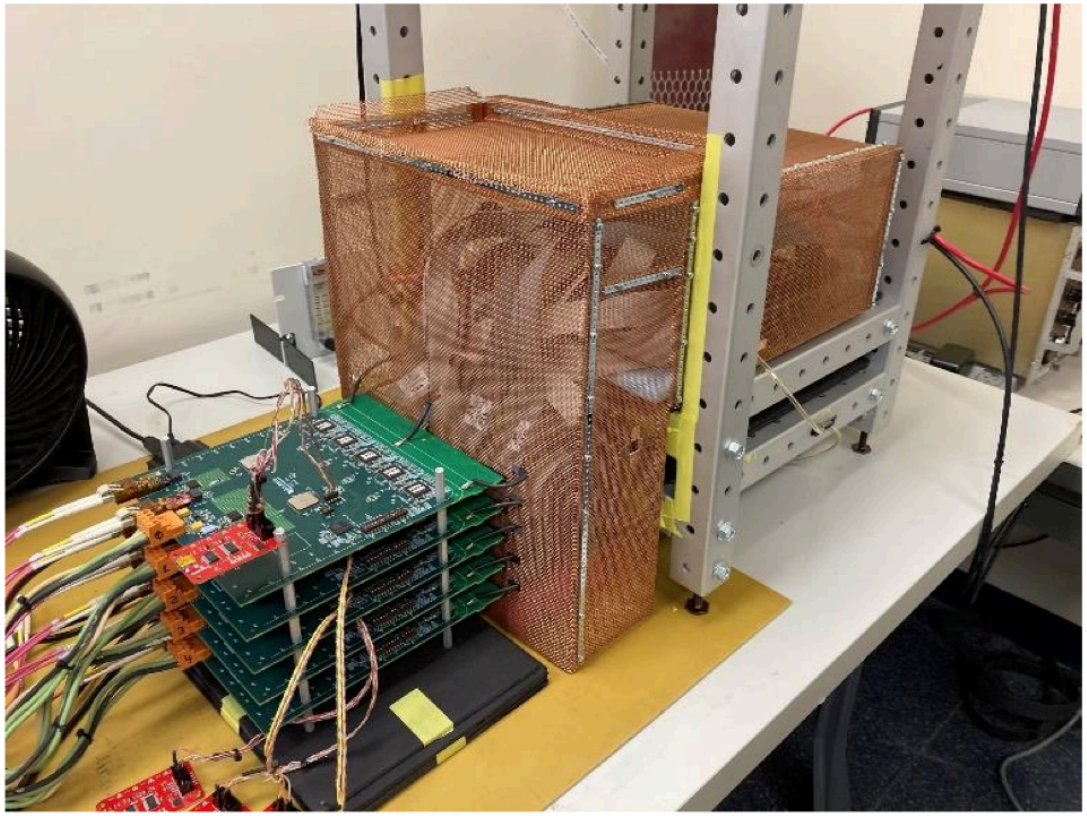
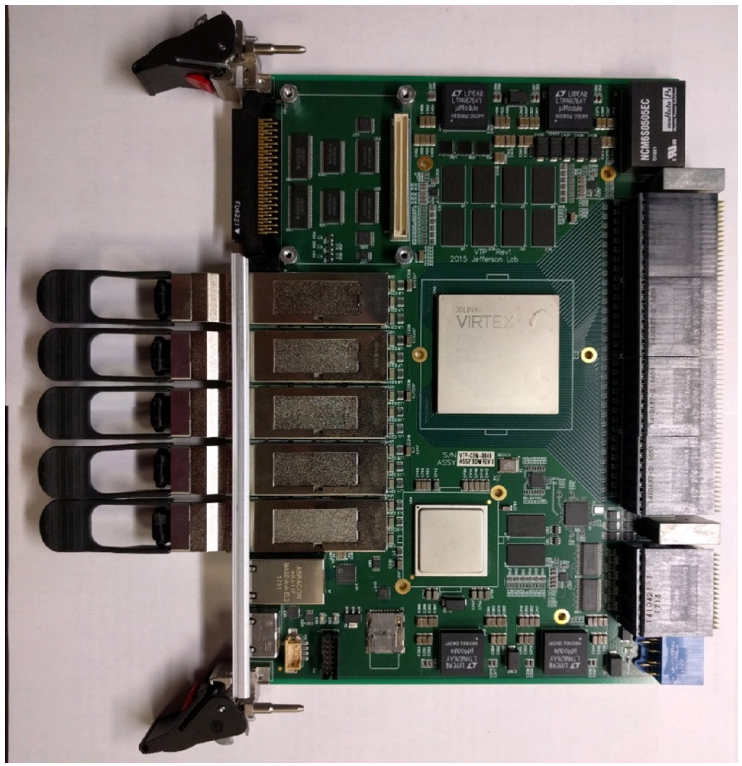
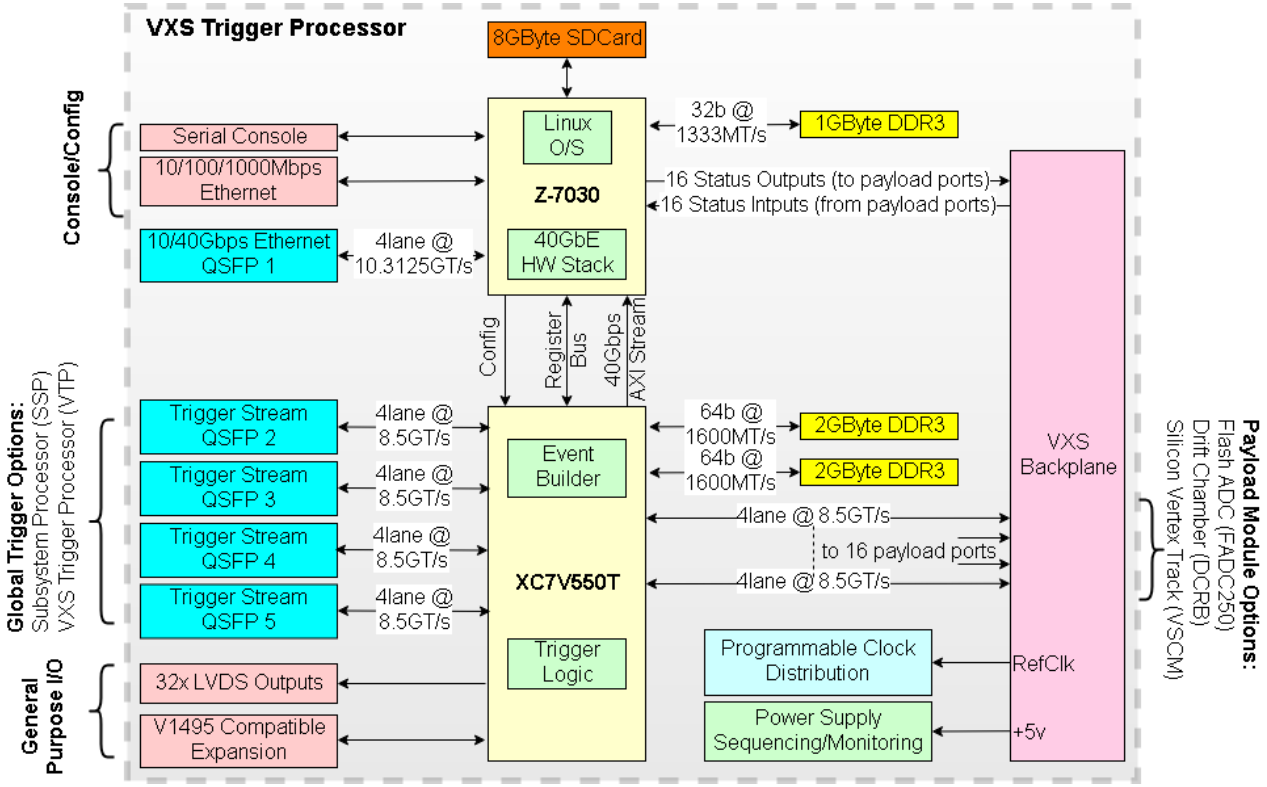


Figure 10. SAMPA front end cards connected to GEM detector. Detector and cables are enclosed in a Faraday cage.

- Better than VMM3 in handling common mode noise in SVT+MM setup
- CLAS12 committed funds into wafers production, enough chips to equip entire MM
- SAMPA V5 - based board(s) will be in JLAB in July
- MM–to-SAMPA adapter board will be designed, working with Fast Electronics Group
- Test on real MM is planned in the end of 2021

Upgrading VTP board for data readout





- VME bus bandwidth is about 200MB/s for JLAB electronics
- In existing trigger-based mode, VTP sends trigger information from QSFP2 to the following trigger system stage, and will be able to act as readout board in the same time if needed (2.5->3.125 for serial on back plane, 10Gbit/s out from 16 slots); more VTPs may be needed if used for readout
- In streaming mode, there is no trigger information, VTP sends stream of data from QSFP1 to Linux server with expected bandwidth up to 4 x 10Gbit/s link
- FPGA based TCP/IP protocol is used between VTP and Linux server
- **Needs about 100K to read all VXS crates through VTPs instead of VME bus**

DAQ upgrade up to 100kHz event rate

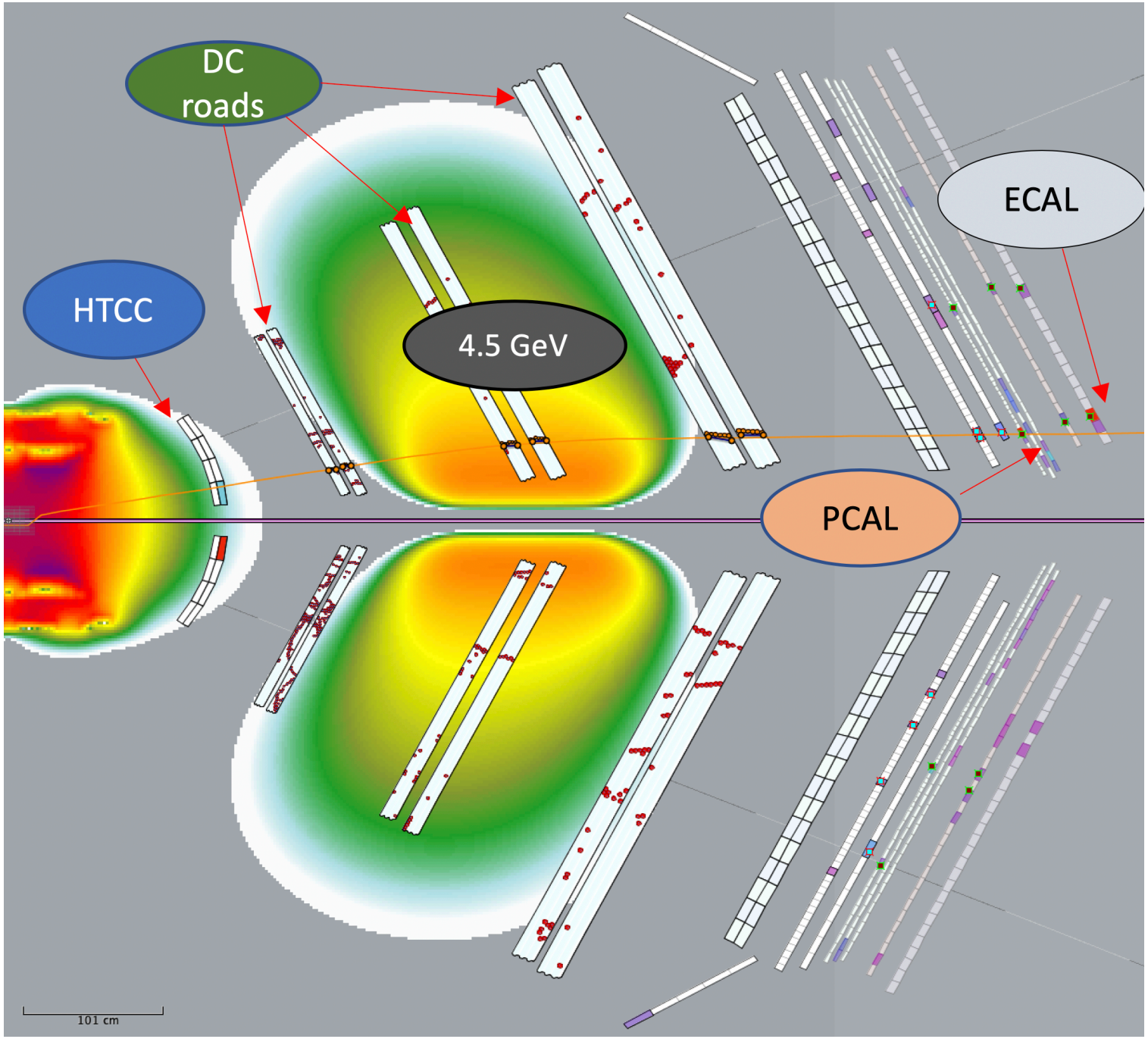
- Trigger-based mode is used
- FADC250, DCRB, VSCM, SSP boards will stay
- CAEN TDCs have to be replaced with VETROCs, VME crates to be converted to VXS
- MM readout to be decided, proposed solution is new SAMPA/VMM3 ASIC based board, work in progress with MM team
- SVT ASIC performance have to be validated for high luminosity running
- Some VTPs have to be used as both trigger and readout modules, firmware under development
- Some boards firmware and CODA software have to be validated and may need to be modified/fixed
- CODA software (EB in particular, also ET and ER) have to be able to process higher rate, may need improvements
- Time scale 2 years

DAQ upgrade to streaming (above 100kHz)

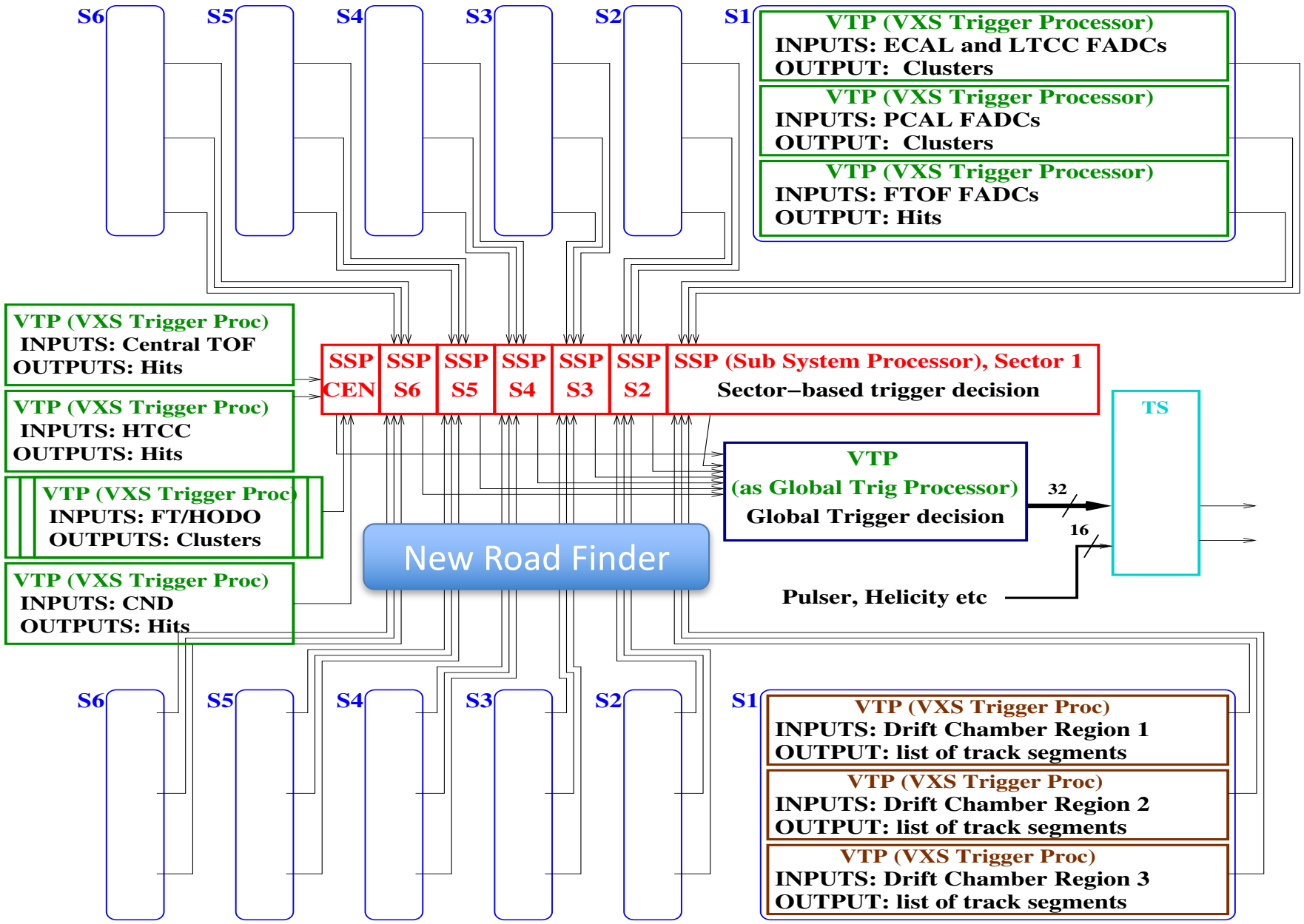
- VTP, FADC250, DCRB, VSCM, SSP, VETROC boards can be reused, or/and new non-vxs based electronics can be used
- All new electronics development (ASICs etc) have to be compatible with streaming mode (for example new tracker readout)
- New streaming version of CODA is needed – not available at current time, switching to streaming DAQ can be considered only when back-end is available or close to become available
- Time scale 3-5 years depending on demand

Front-end electronics upgrade is underway, no serious problems anticipated

CLAS12 Electron Trigger Event Example



CLAS12 Trigger System (level1)



CLAS12 Trigger System Status

- Fully operational, efficiency close to 100%
- Portion of ‘good’ events depends on trigger type (electron, photon, meson), about 50% in average
- The achieved performance of the CLAS12 Trigger System allows use without significant changes for the entire CLAS12 physics program, although portion of ‘good’ events can decline with luminosity increased

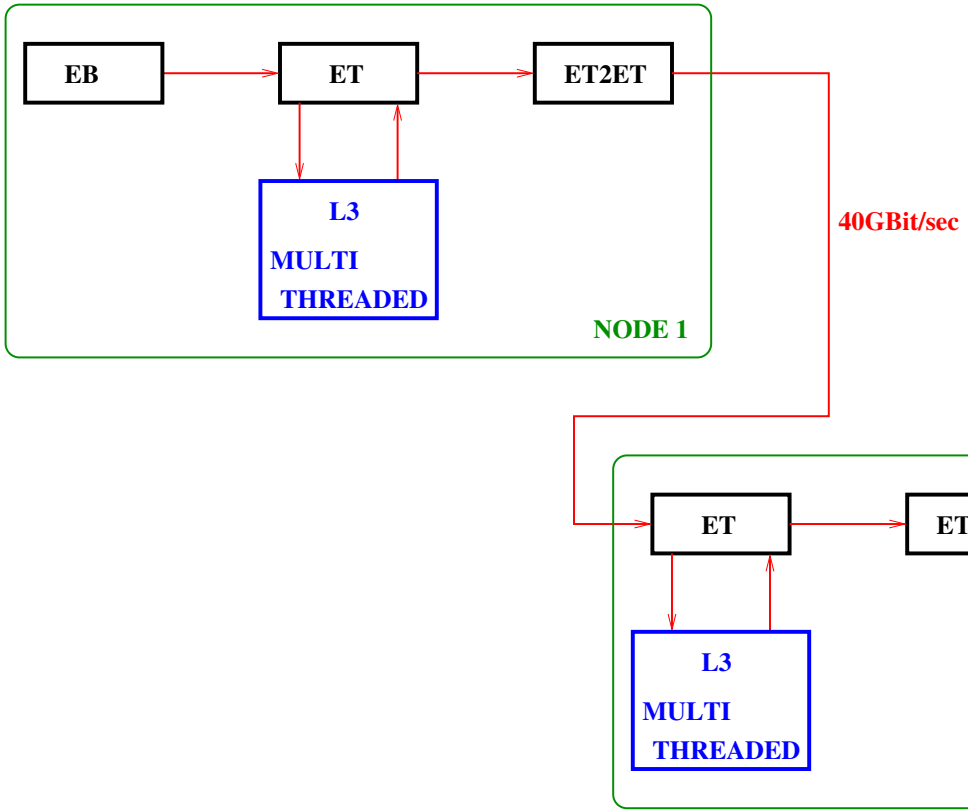
CLAS12 Trigger possible improvements

- ECAL/PCAL trigger can to be improved in following ways: (1) in addition to electron shower clustering, search for MIP-like clusters have to be added to improve muon class triggers; (2) use individual strip real attenuation length instead of average one; (3) allow individual strip timing delays and improve cluster timing reporting
- DC trigger can be improved (needed in particular for Q**2 cuts) in following ways: (1) segments selectivity and space resolution improvement; (2) roads space resolution improvement; (3) drift time usage to improve two previous items feather
- Additional geometry matching between detectors, for example DC vs PCAL clusters
- Allow multi-particle trigger in one sector
- Improve timing coincidence by narrowing signals from different trigger components

CLAS12 Trigger Upgrade

- Current trigger system is solely based on FPGA, there is no Level3 component
- We decided do not touch existing Level1 trigger (for now), and implement all additional elements in new level3 (software) trigger
- Dummy Level3 component was added, and all trigger improvements will be developed as Level3 elements; it will allow not only improve current trigger, but also develop solutions for future streaming DAQ data processing; fpga-based solutions still can be considered
- Initial tasks for level3 will be drift chamber new segment finder, and AI-based track finder; after that other detectors will be incorporated

CLAS12 Level3 (software) trigger



Level 3 is DAQ component, running between Event Builder and Event Recorder, currently used to correct delayed helicity reporting

C/C++/JAVA supported

Level 3 provides additional event and data rate reduction for the current physics program, and will be a test bed for streaming era data processing algorithms

4 servers are available, new server with 2 GPU cards is coming

Drift Chamber – based trigger component

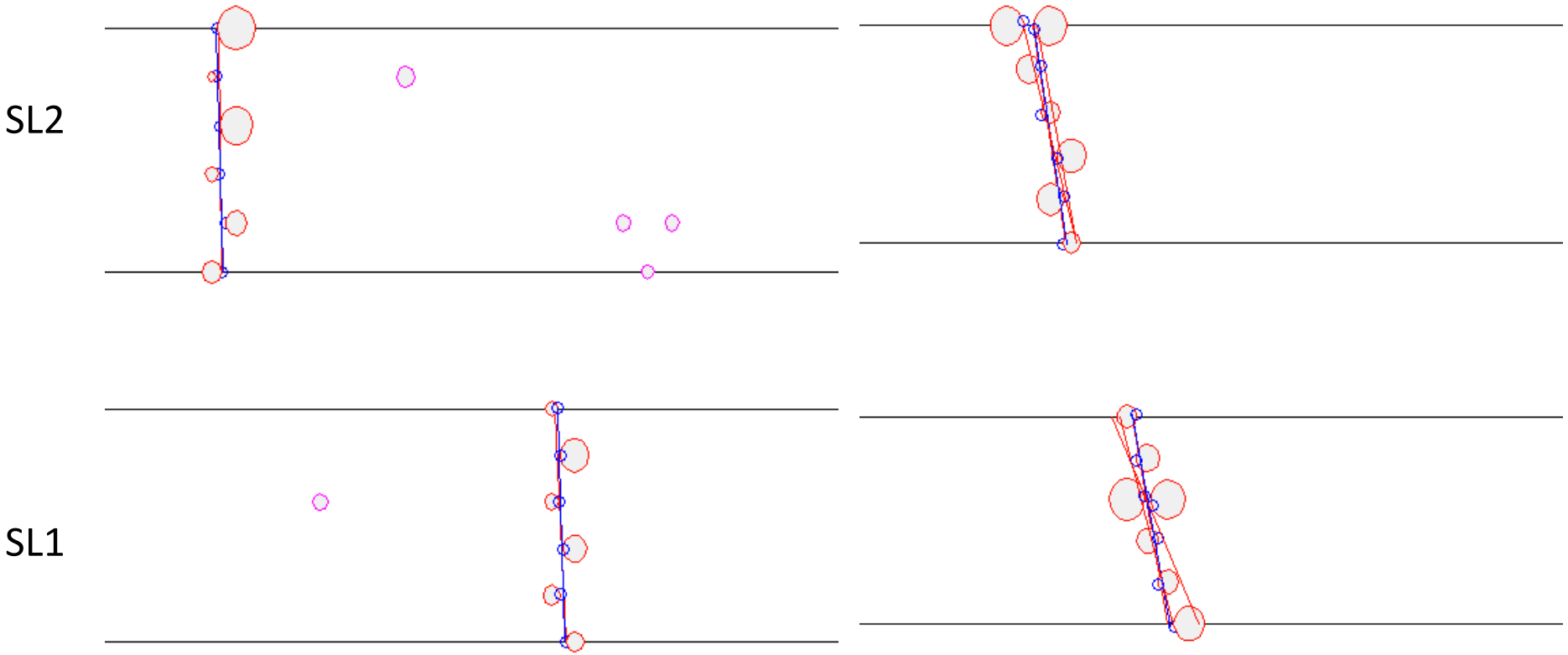
- Existing fpga-based segment finder: hit-based, does not need timing calibration, compares data with segment dictionary
- Proposed segment finder: time-based, requires reasonable timing calibration, fits data by straight line – suppose to improve segment position and angle resolution
- Three basic operations: (1) shift-and-sums, (2) peak search in 2-dim array, and (3) linear fit; will explore fpga-, gpu- and cpu-based solutions

- Existing fpga-based road finder: hit-based, does not need timing calibration, compares data with road dictionary, uses 2- and 3-cell width roads
- Proposed road finder: AI-based (developed by Gagik and co), use segments from previous stage

Drift Chamber readout upgrade

- To study DC signals FADC-based test setup was build, set of cosmic runs were taken and data was analyzed; time-over-threshold readout was found useful and desired
- New firmware for DCRB boards was developed by Ben Raydo, changes in readout lists under way, will be ready for testing soon
- In addition to time-over-threshold reporting, new firmware allows DCRB to report multiple hits (currently they are single-hit TDCs)
- One of the problems we hope to solve is ‘wrong’ timing reporting for the drift chamber hits (for example when ‘wrong’ early hit kills good hit)

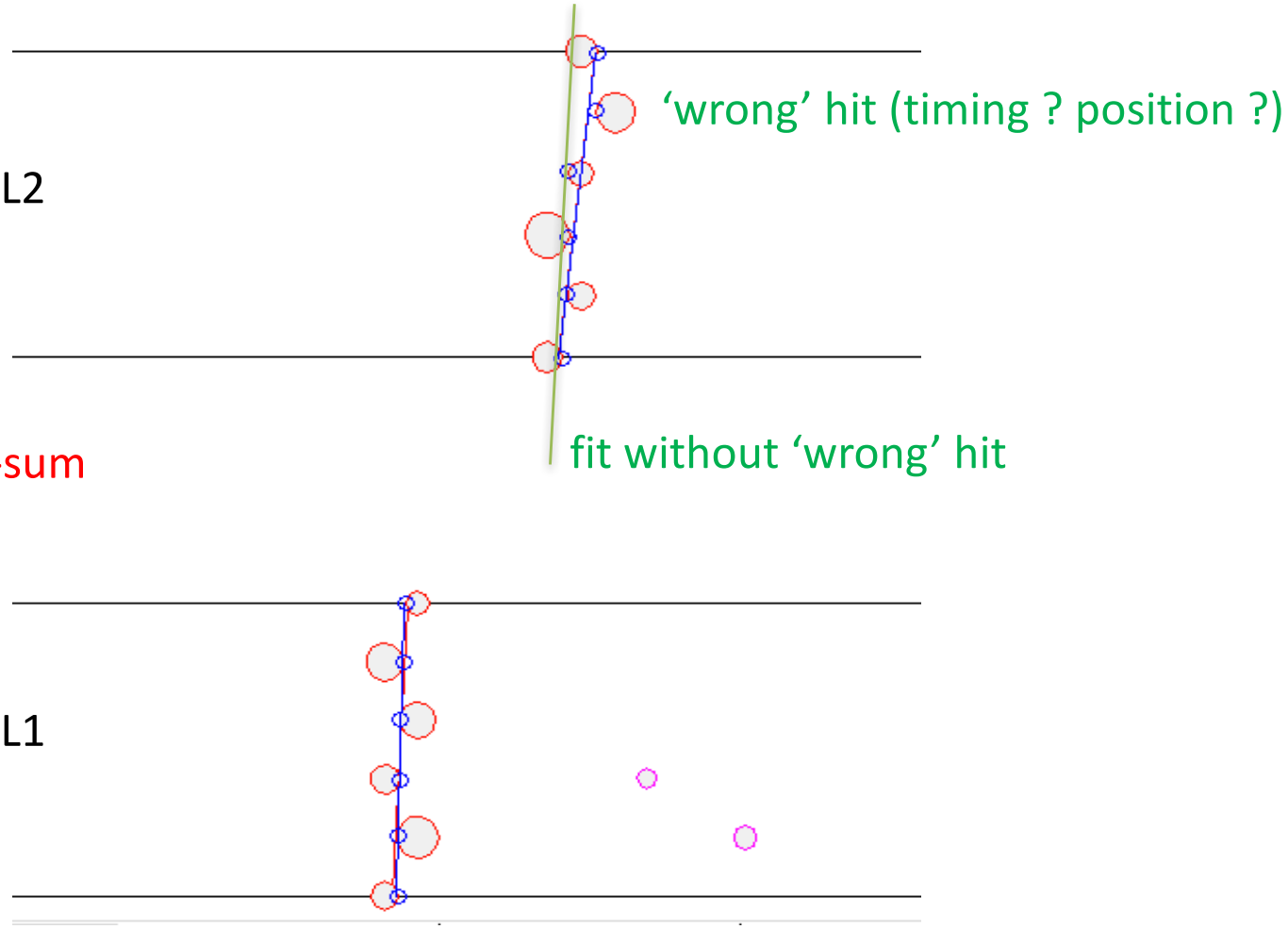
Drift Chamber Time-based Segment Finder
(works on 112x6 wire superlayers)



Red lines: shift-and-sum (fast processing on FPGA, GPU to be tested)

Blue line: linear fit

Drift Chamber Time-based Segment Finder (inefficiency/wrong timing)



Red lines: shift-and-sum

Blue line: linear fit

Example shows one of the observed limitations for the possible dc trigger improvement: request to have 'parallel' segments in that region will lead to inefficiency

Drift Chamber – based trigger component development status

- For the high luminosity experiments, drift chamber trigger component was identified as needed primary attention
- Three problems in drift chamber trigger implementation can be named: noise (extra hits), inefficiency (missing hits) and wrong time reporting
- The combination of those problems creates significant difficulties when trying to improve existing DC-based trigger
- Several possible upgrades are being explored: new TDC firmware (time-over-threshold and multihit), drift time usage in segment finder, AI usage in road finder
- All those upgrades are implemented and ready for testing in CLAS12, expect results by the end of 2021

Online data processing / trigger improvement necessity:
with computing technology development and expected data rate on the level of few GB/s for high luminosity running, we can probably use existing trigger system and let data rate increase by factor several; nevertheless we will continue to develop improved trigger algorithms because, if successful, it will increase data quality and speedup offline data processing; our strategy can be reconsidered in future

CLAS12 and Streaming Readout

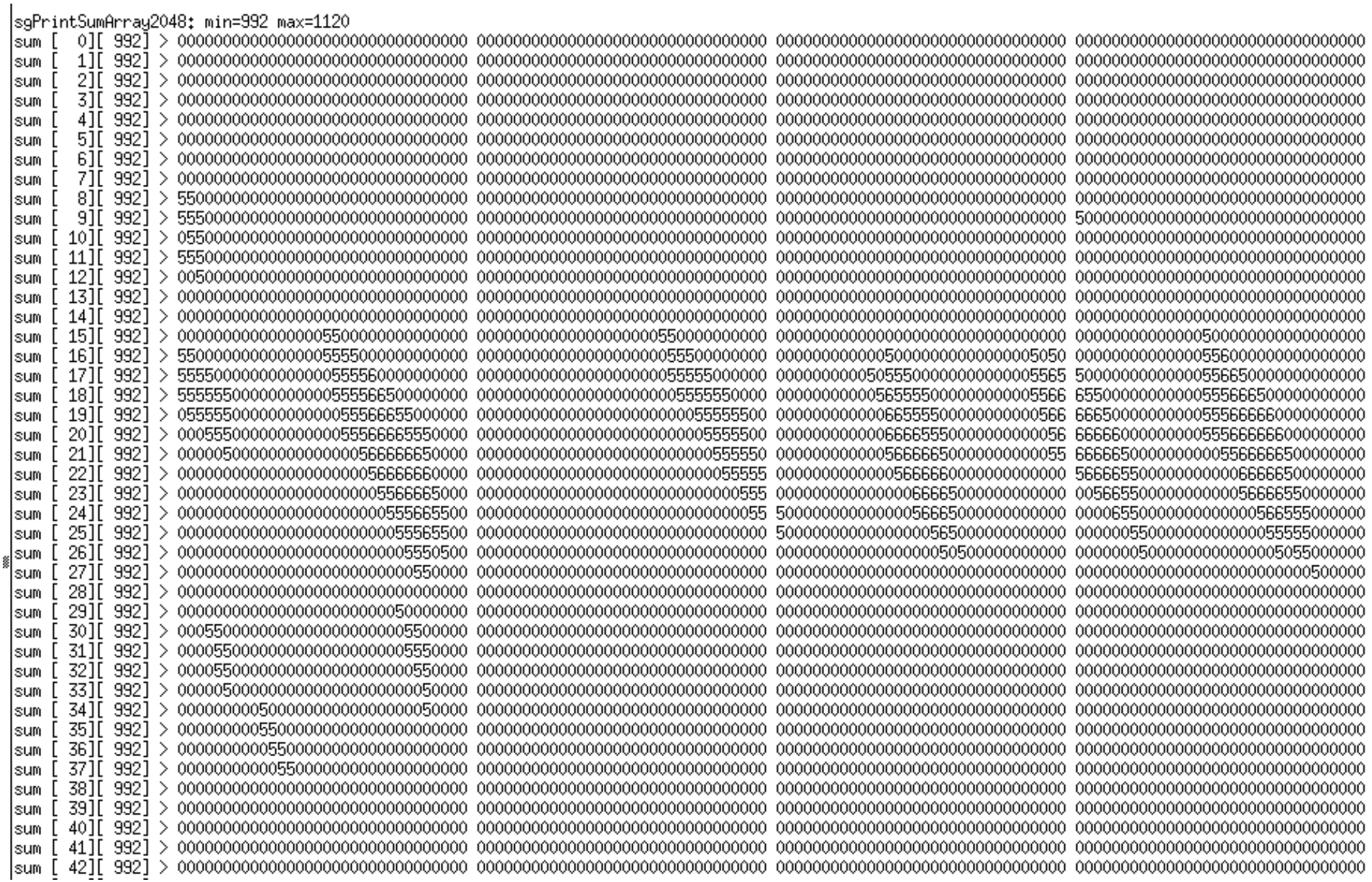
- It will be needed to use streaming mode if required event rate will exceed 100kHz (may not happens because of detector limitations and/or L1 trigger system improvements)
- Because of currently conducted upgrades, CLAS12 front-end electronics should be ready for the streaming DAQ operation in a few years; back-end suppose to be developed by other groups
- We are not planning to use hybrid system, will switch from triggered to streaming daq completely when it will be needed
- CLAS12 is able to provide test beds for the streaming DAQ development, from relatively small setups (few VXS crates) up to 40-crate system where full scale streaming DAQ can be tested, with the data rate on the level of 50GByte/sec, it should help back-end development conducted by others
- It is unclear how much data processing will be needed (same situation as for triggered daq for high luminosity) – everything possible from none to full reconstruction

Conclusion

- CLAS12 front-end upgrade plan is in progress, with the purpose to increase event rate up to 100kHz with existing triggered mode, and to make system compatible with streaming mode operation in future
- New data processing solutions being developed and tested in frame of the new level3 trigger project, with the purpose to improve trigger system
- We are working closely with jlab and outside groups assisting them with streaming DAQ back-end development, providing testing facility; it can be needed by CLAS12 if event rate exceeds 100kHz

Supporting slides

Time-based segment finder: 2-dim peaks after shift-and-sum process



Segment angle

Segment position