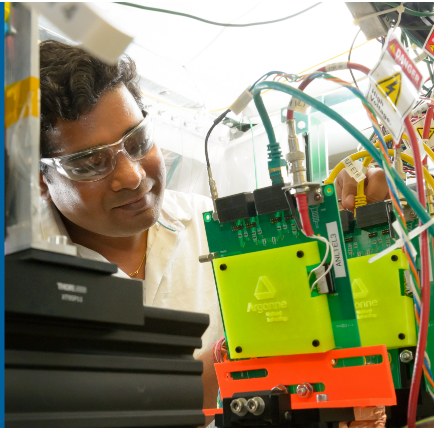
EIC UG Meeting Early Career Workshop

Time measurements using ultra fast silicon detectors with a 120 GeV Proton Beam for the TOPSiDE Detector Concept at The Electron-Ion Collider



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U.S. DEPARTMENT OF ENERGY
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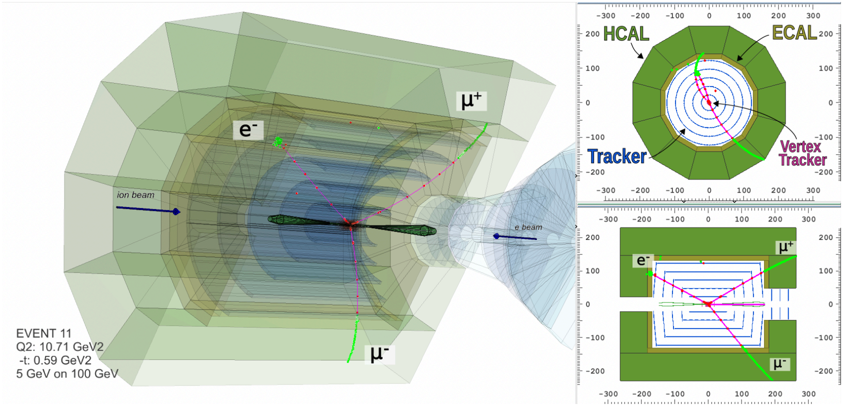
July 29, 2021

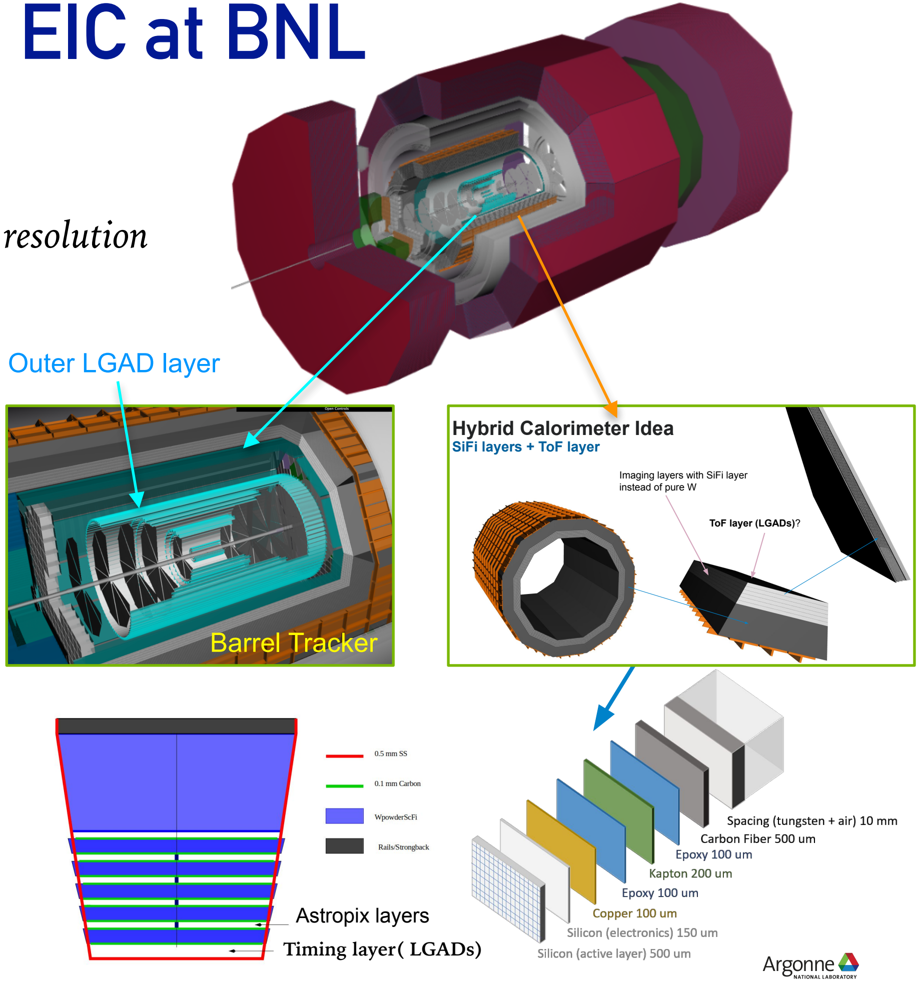
Outline

- Experimental Involvement
- UFSDs for EIC
- Low Gain Avalanche Detectors (LGADs)
- LGAD to AC-LGAD
- Summary

Experimental Involvement - EIC at BNL

- **The TOPSiDE detector concept at the EIC**
  - UFSDs for Particle Identification using ToF
  - π - K - p separation up to 7 GeV/*c* - *10 ps time resolution*
- **ATHENA experiment**
- **Barrel Silicon Tracker** - LGAD under study
- **Barrel ECAL**
  - Barrel SiW imaging calorimeter
  - Barrel hybrid SiW + WSciFi calorimeter





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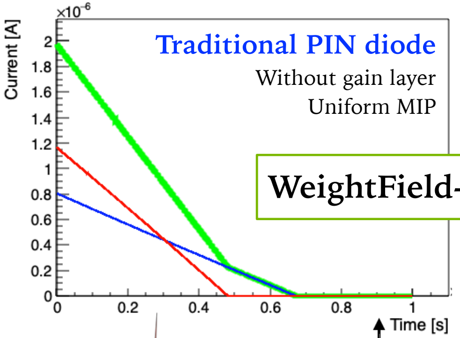
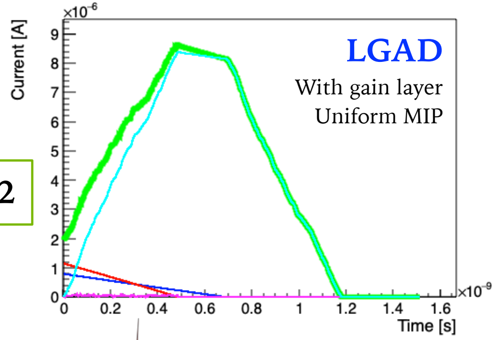
Introduction to UFSDs

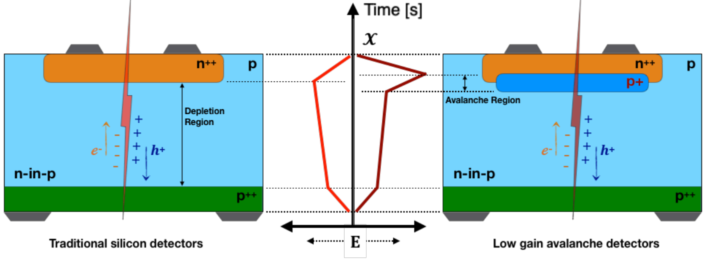
- **Low-Gain Avalanche Diode (LGAD)**
  - Gain layer (n^{++}- p^{+} - p - p^{++})
- **High E-field in gain region**
  - Multiplication process
  - Internal gain of 10-70
  - High signal-to-noise (SNR) ratio
- One bunch crossing with ~50 overlapping events recorded by the CMS experiment in 2012
- At HL-LHC it will be at the order of 150–200 events per bunch crossing
- The time-dimension improves reconstruction process by considering only time-compatible hits in the pattern recognition phase
- Particle Identification using Time-Of-Flight method

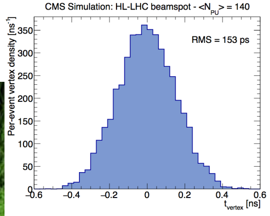
LGADs are considered potential candidate at the EIC

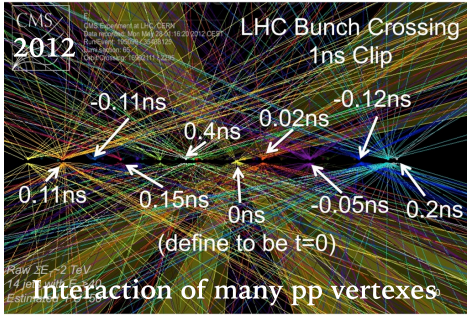


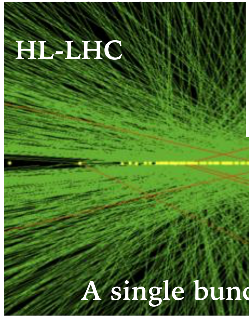
WeightField-2





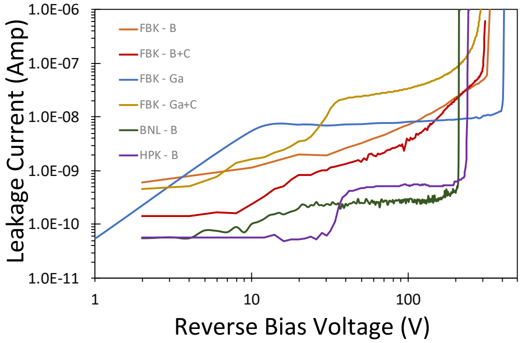


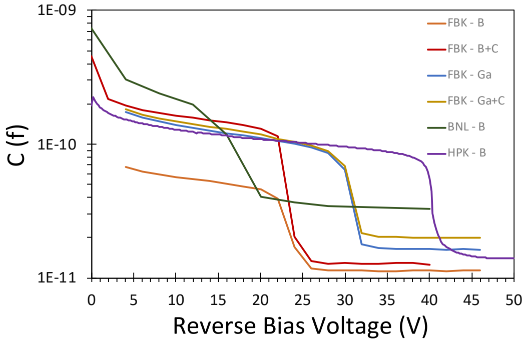


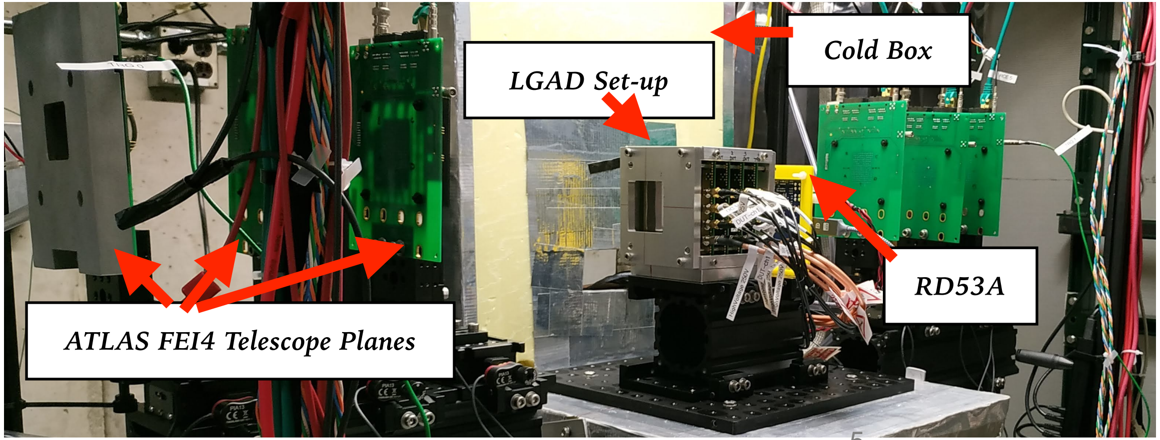


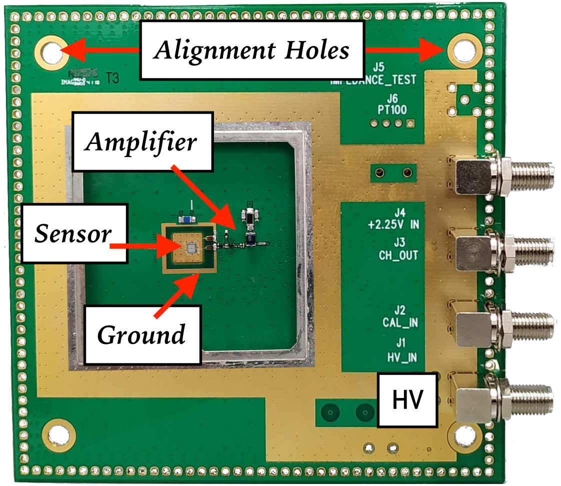
LGAD Measurement Setup

- **Single channel readout board**
  - Wide bandwidth 2 GHz and gain 10
  - Total trans-impedance of 4700Ω
  - followed by commercial amplifier
- **120 GeV Proton Beam at Fermilab**
  - Data were collected in spills of 4 sec
  - Trigger rate between 1 and 5 Hz





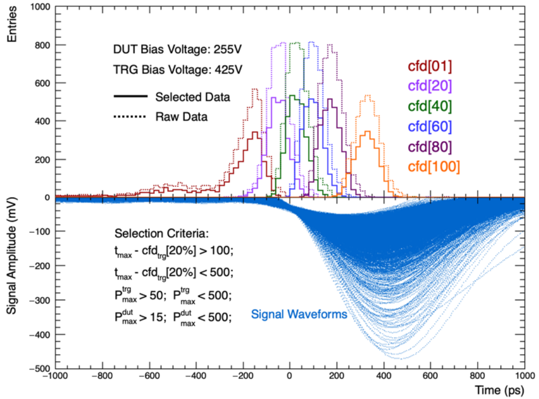




Analysis methods

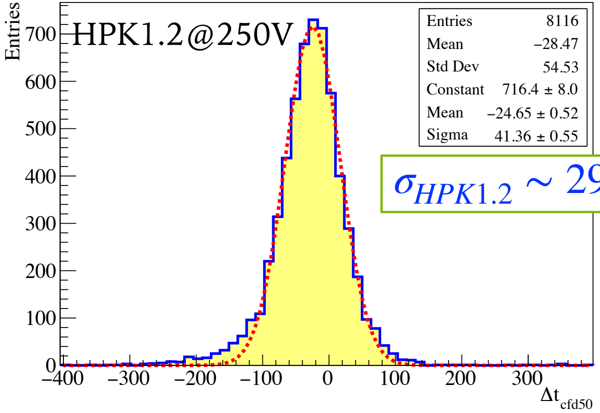
Analysis to mimic timing readout system

- Constant Fraction Discriminator (CFD) method
- Signal amplitude should be above 5 times of noise level and not be saturated by scope or readout chain
- The RMS of time difference between DUT and TRG

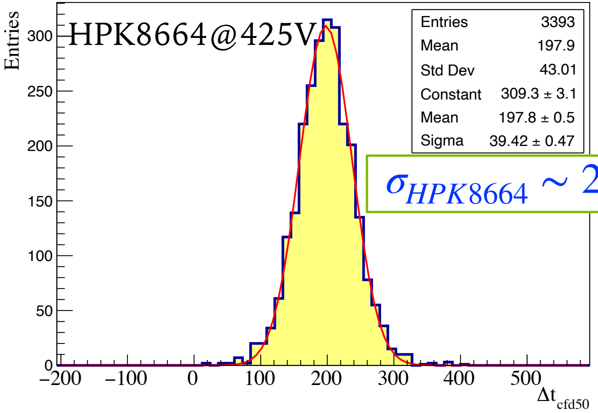


$$\sigma_t^2 = \sigma_{TimeWalk}^2 + \sigma_{Jitter}^2 + \sigma_{LandauNoise}^2 + \sigma_{Distortion}^2 + \sigma_{TDC}^2$$

$$\sigma_{DUT}^2 + \sigma_{TRG}^2 = \sigma_{(TRG-DUT)}^2$$



$\sigma_{HPK1.2} \sim 29.25\ ps$



$\sigma_{HPK8664} \sim 26.43\ ps$

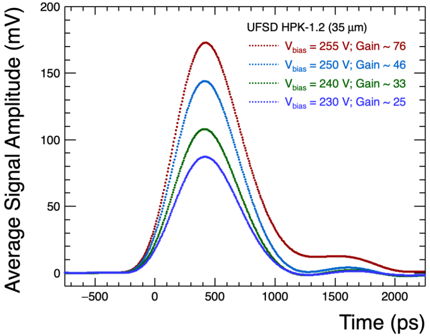
Results and Summary - LGADs

Test beam results for HPK 1.2 (35μm), 3.1(50μm)

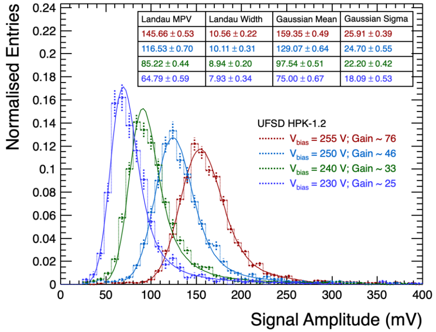
- Constant Fraction Discriminator (CFD) method
- The RMS of time difference between DUT and TRG gives time resolution
- Charge Multiplication increases with bias voltage increasing the Gain

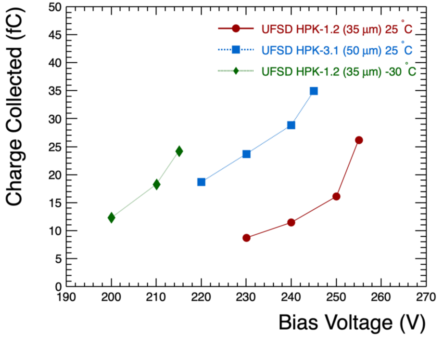
$$\sigma_t^2 = \sigma_{TimeWalk}^2 + \sigma_{Jitter}^2 + \sigma_{LandauNoise}^2 + \sigma_{Distortion}^2 + \sigma_{TDC}^2$$

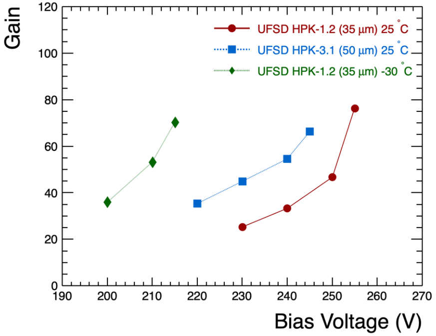
Average Signal Shape

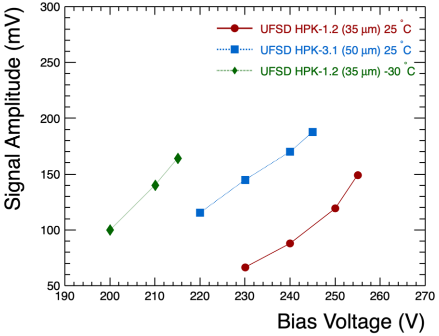


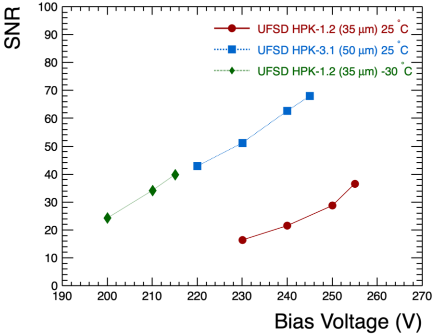
Normalized Signal Amplitude





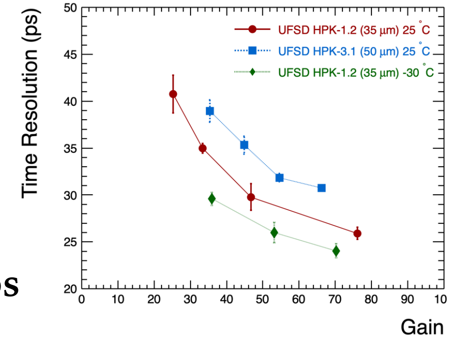


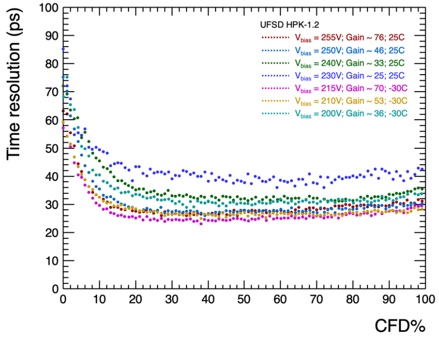


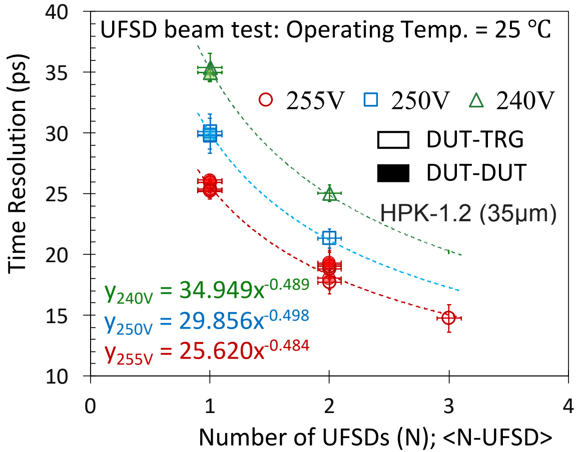


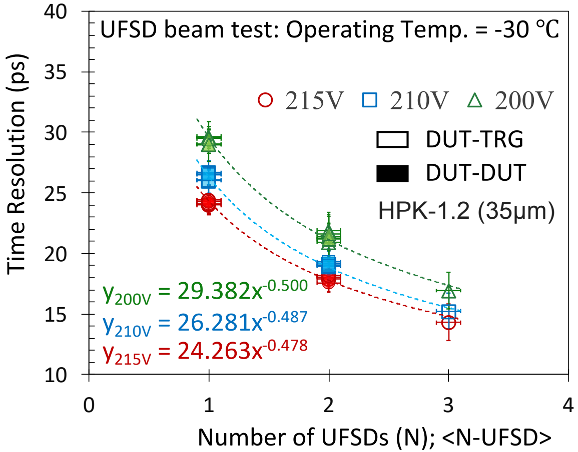
Results and Summary - LGADs

- Timing resolution for 3 layers of LGADs
- Timing resolution improves at low temperature but restricted by the lower breakdown voltage
- Very short rise time of ~350-400 ps were obtained
- M. Jadhav et al 2021 JINST 16 P06008, arXiv:2010.02499
  - Achieved **timing resolution of 14.31 ± 1.52 ps**
  - Fastest test beam measurements to date





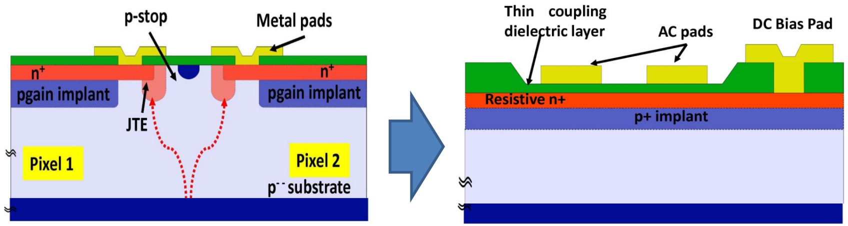




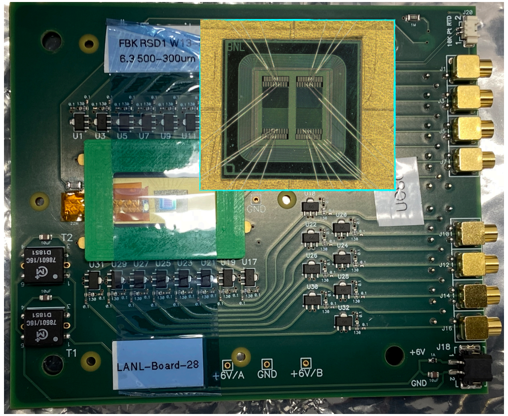
AC-LGAD Testing

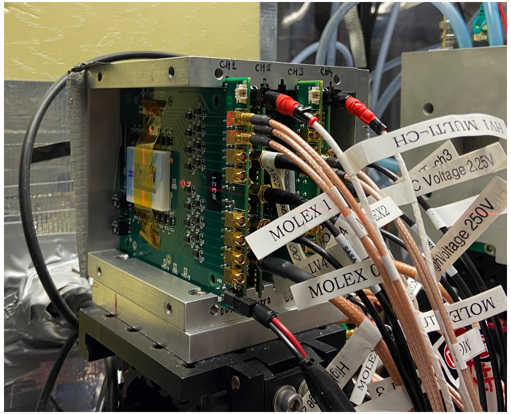
Test beam campaign for AC-LGADs

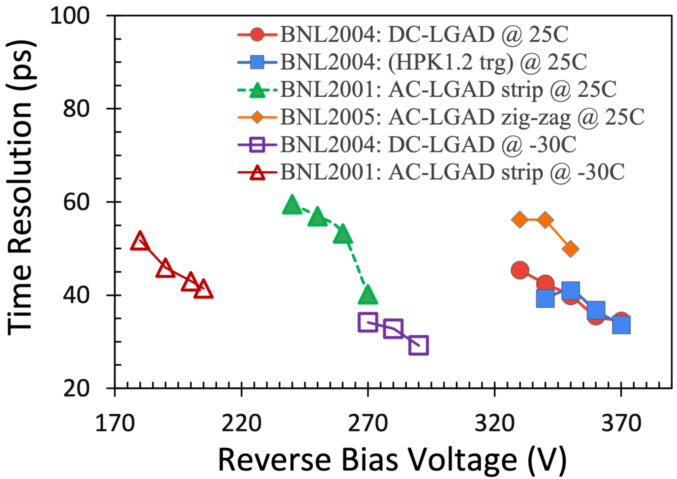
- **Dielectric layer for isolation and AC-coupling**
  - Results in 100% fill factor
- **AC-LGADs and Multi-Channel Boards**
  - Testing at the 120 GeV proton test-beam in collaboration with UCSC and BNL as a part of the EIC LGAD consortium
  - The LGADs with strip and pixel array geometry are mounted on multi-channel readout boards
- **Upgrading DAQ from software based CFD to multi-channel digitizer**



DC-LGAD AC-LGAD

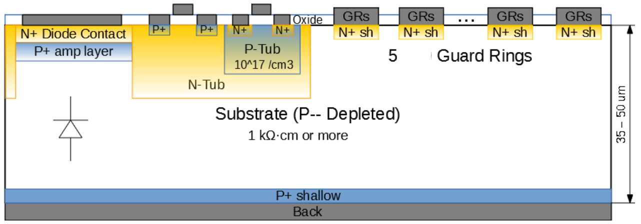


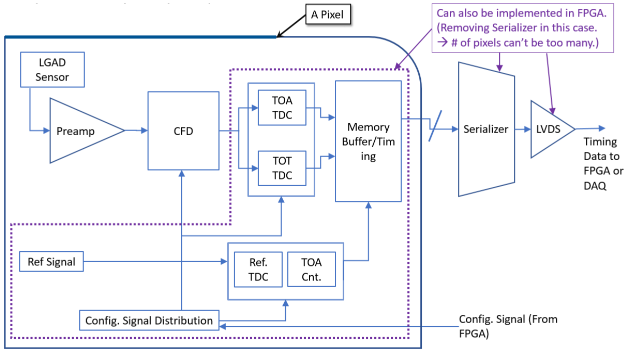


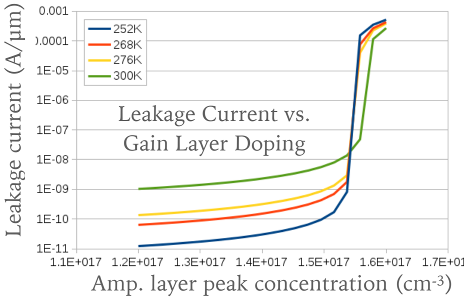


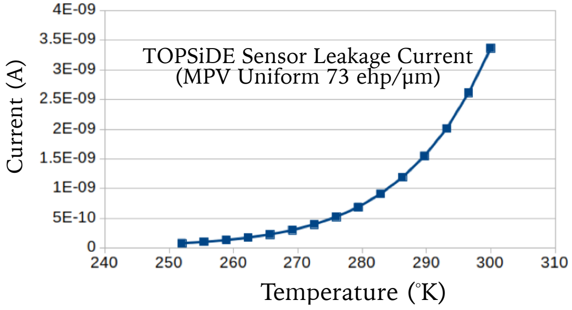
LGAD Development at Argonne

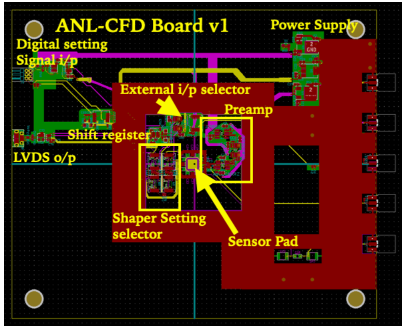
- **TCAD simulation - ATLAS Silvaco**
  - Sensor with pad size of 1 × 1 mm^2 and thickness 50 μm
- **The goal is to integrate readout electronics using HV-CMOS (PicoPix)**
- **The first stage includes preamplifiers, shaper, constant fraction discriminator**
  - Being prototyped on PCB board (w/o TDC) before implementation on to pixel
  - Time-of-Arrival, Time-over-Threshold
  - FPGA Ultra96 - programmable for up to 4 channels











Summary

- **Characterized and tested LGAD (DC & AC) in the lab as well as test beam**
  - Developed DAQ framework based on PyVISA and Python
  - Achieved **timing resolution of 14.31 ± 1.52 ps** ➔ Fastest test beam measurements to date
  - M. Jadhav et al 2021 JINST 16 P06008, arXiv:2010.02499
  - Testing of AC-LGADs with zig-zag strip structure (targeted for publication)
- **Ongoing tasks**
  - Upgrading DAQ from software based CFD to multichannel digitizer
  - Providing trigger from LGAD sensor to ATLAS telescope
  - Testing CFD read-out boards and development of Monolithic LGADs

Thank You!

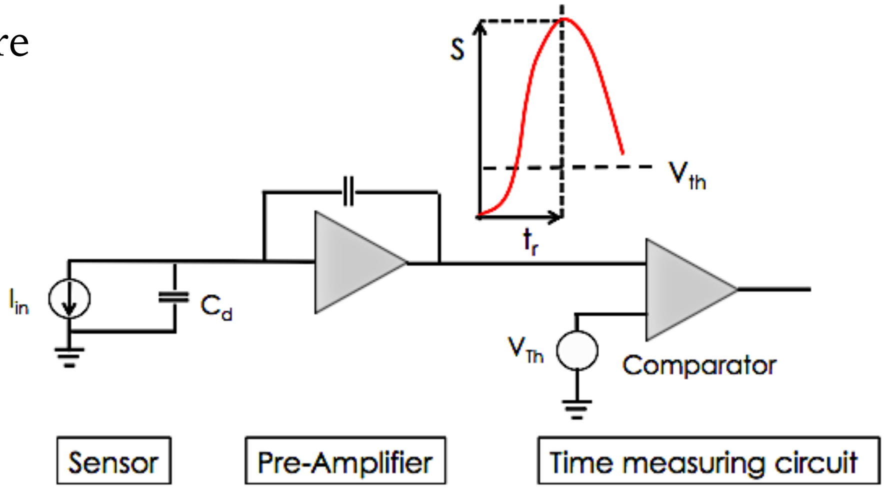
Back-up Slides

Timing Measurements

Time resolution of the Silicon detector can be expressed as contribution of,

$$\sigma_t^2 = \sigma_{TimeWalk}^2 + \sigma_{Jitter}^2 + \sigma_{LandauNoise}^2 + \sigma_{Distortion}^2 + \sigma_{TDC}^2$$

- **Timing capabilities of the silicon detector** are characterized by signal at preamplifier output and TDC binning
- **Time of arrival** is set when signal crosses the comparator threshold
- **Timing resolution** is measured as RMS of the timing difference (or TOF of a MIP) between the device-under-test (DUT) and the trigger.



A simple time-tagging detector

Timing Measurements

- **Time Walk:** the voltage value V_{th} is reached at different times by signals of different amplitude

$$\sigma_{TimeWalk} = \left[\frac{V_{th}}{dv/dt}\right]_{RMS}$$

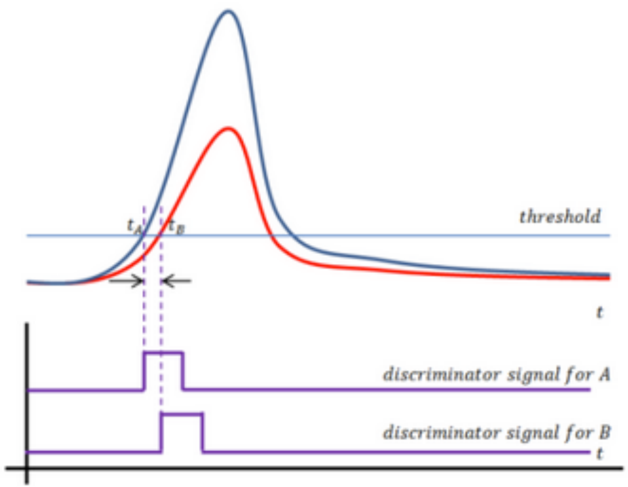
Constant fraction discriminator (CFD) with TOA defined at % of signal amplitude reduces time-walk contribution

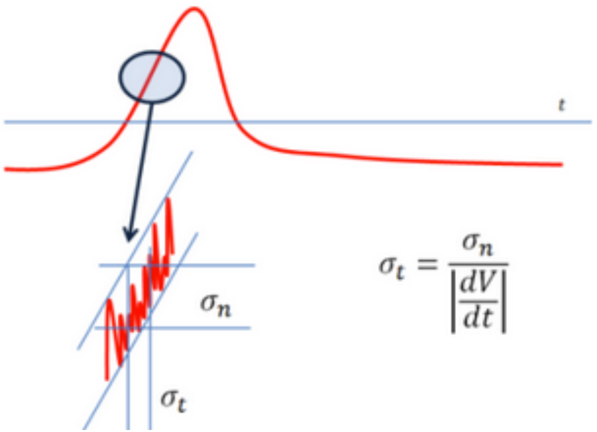
- **Jitter:** variation in time caused by the noise in the system

$$\sigma_{Jitter} = \frac{Noise}{dV/dt}$$

The noise is summed to the signal, causing amplitude variations

The predominant contribution to the timing resolution





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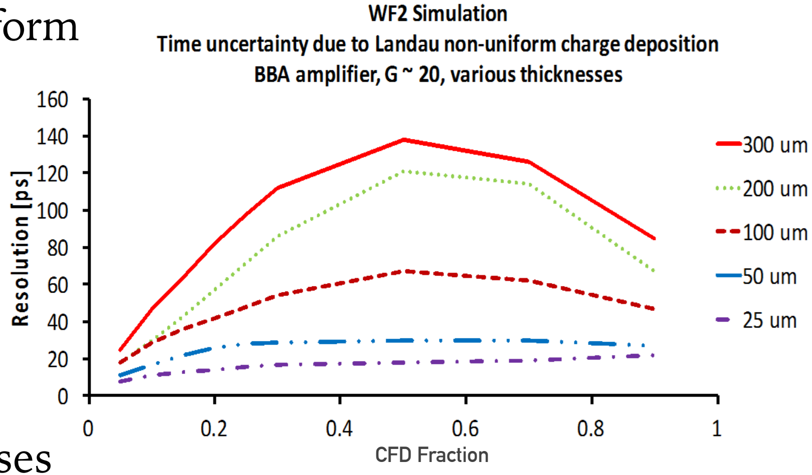
Timing Measurements

- **Landau Noise:** introduced by a particle's non-uniform charge deposition along its passage
  Decreases with thickness of the sensor
  Jitter and Landau noise contribute almost equally
- **Distortion:** The signal distortion is negligible in silicon for the saturated drift velocity and uniform weighting field.
- **TDC:** The TDC effect is minimal in most of the cases

$$\sigma_{TDC} = \frac{TDC_{bin}}{\sqrt{12}}$$



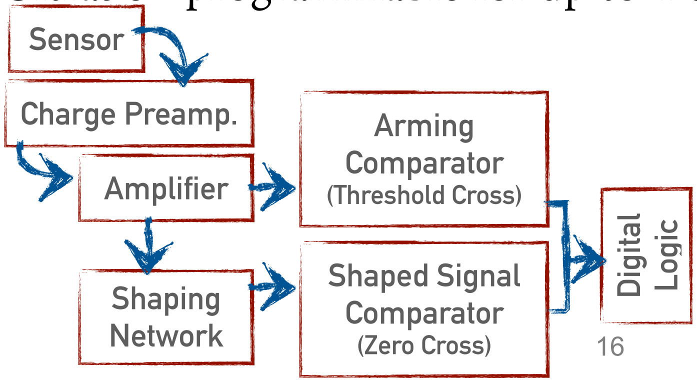
Thinner Sensor => faster rise time => larger slew rate

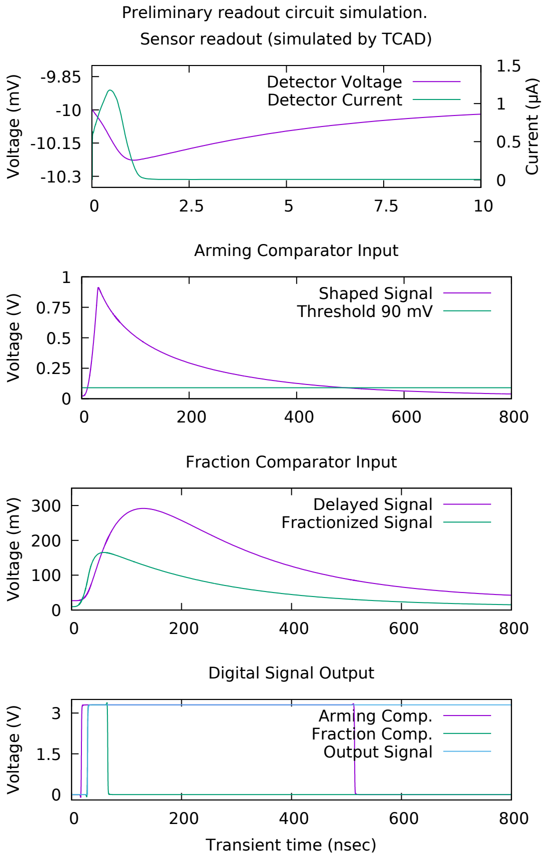
The time resolution is minimized by maximizing the slew rate dV/dt of the signal and minimizing the noise

We need large and short signals!

Readout Development

- **Front-end readout components**
  - Shaper, amplifier, discriminators, digitizers (TDC)
  - Time-of-Arrival, Time-over-Threshold
- **The first stage includes preamplifiers, shaper, constant fraction discriminator**
  - Being prototyped on PCB board (w/o TDC) before implementation on to pixel
  - FPGA Ultra96 - programmable for up to 4 channels





LTSpice Simulation