
HPS DAQ updates

Sergey Boyarinov
JLAB
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HPS DAQ & Trigger Requirements

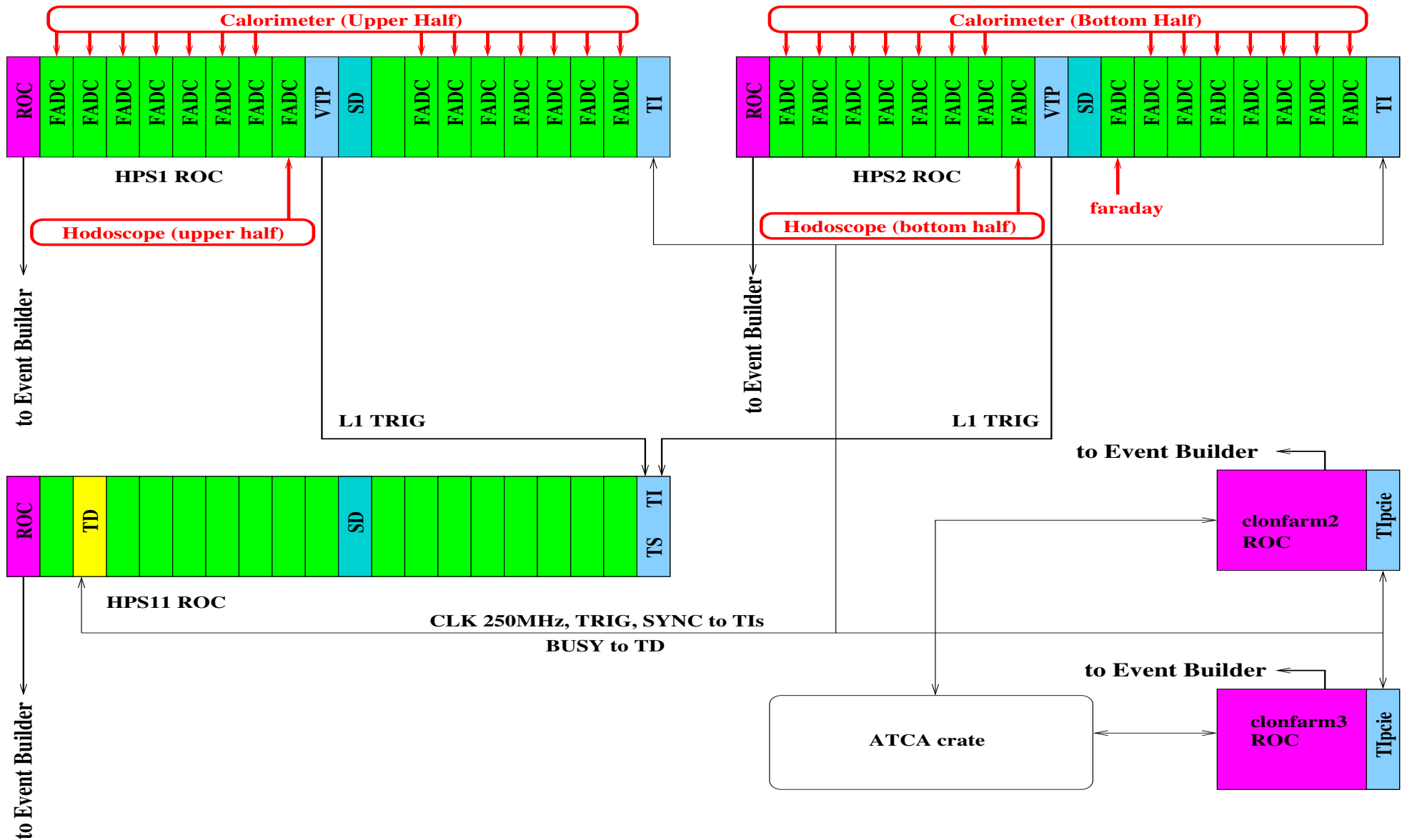
20kHz event rate

100MB/s data rate

>95% livetime

Achieved event rate 27kHz

HPS DAQ/Trigger Front-End Electronics



3 VXS crates, 2 servers, 1 ATCA crate, 7 Readout Controllers

HPS DAQ Status

- **Calorimeter Readout: 442 channels of 12bit 250MHz Flash ADCs**
- **Hodoscope Readout: 32 channels of 12bit 250MHz Flash ADCs**
- **CPU/VTP/TS/SD/TD trigger and signal distribution boards**
- **3 VXS crates**
- **2 servers with Tlpcie cards for SVT readout**
- **SVT readout (front-end and ATCA blades)**

Back-end computing and software is CLAS12 facility: network, computing, DAQ software, data monitoring, messaging system, realtime database

Main development for future run

Two new Tlpci boards were received from production and currently under testing

Tlpci was tested in servers where old version failed, and it works now, servers recognize it as standard PCI device

Library being developed

More boards will be produced, then we will be able to send one to SLAC

SVT readout have to be adjusted using new Tlpci boards

New Tlpcie module

Better PCIe compatibility:

- Xilinx UltraScale+ FPGA: xcku3p
- PCIeexpress from gen1x1 (low power) to gen3x8 (high bandwidth)

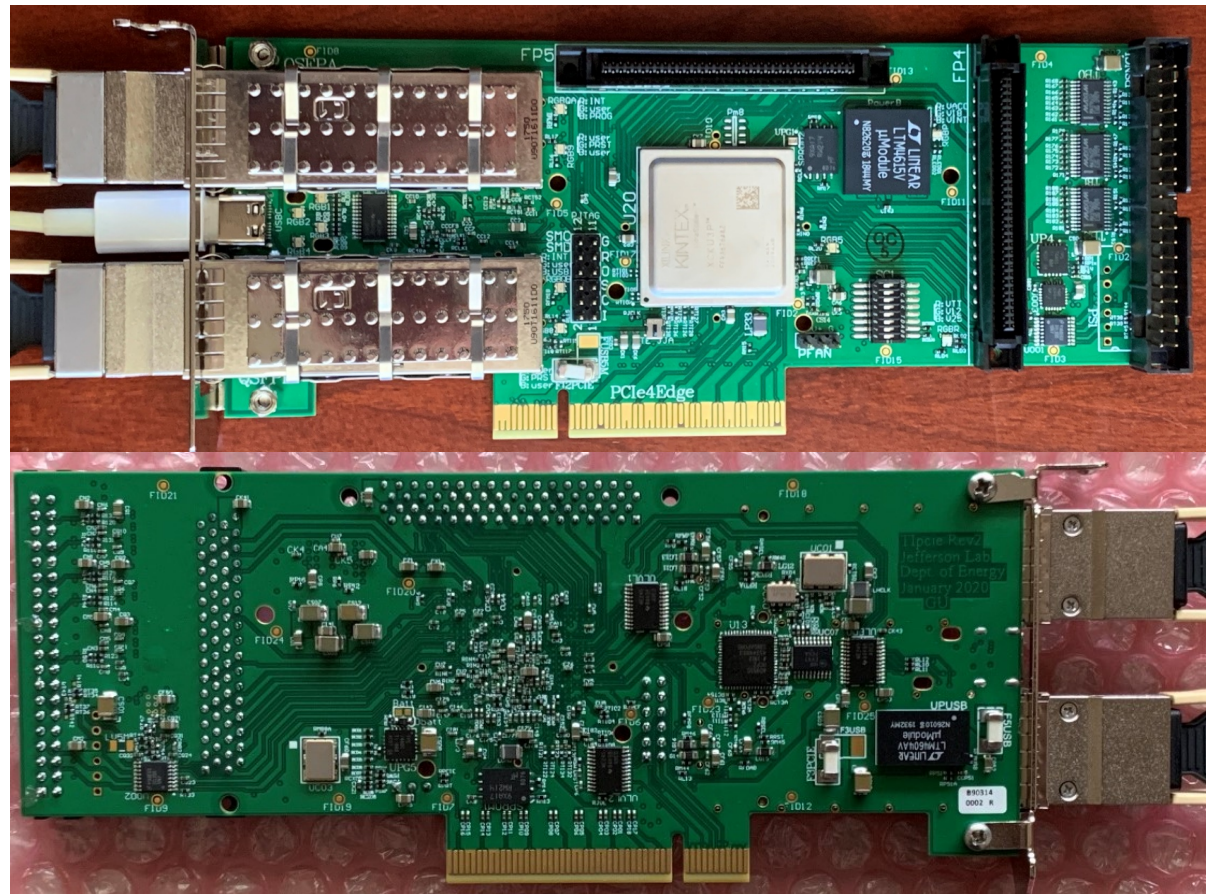
More like a VME TI:

- TI fiber#1, fiber#5
- 40-pin IO to the second front panel
8 outputs + 1 clock output;
(LVDS, 3 optional ECL)
10 inputs + 1 clock input; (any diff. level)

More potentials:

- Another 64 LVDS connection to the FPGA:
64-channel FPGA based TDC
- USB-C connector on the front panel
+5V in for standalone operation

Two prototypes under testing, more boards are ordered



DAQ Status

All hardware and software on JLAB side is ready to run any time, except new Tlpci boards

SVT part is removed

Integration with SVT DAQ has to be repeated again because of new Tlpcie module, it has to be discussed and planned (test setup at SLAC)

If SVT readout performance improved we can increase overall DAQ performance (without SVT, DAQ can run >30kHz)