4π Silicon Hybrid Detector with Charged Particle Identification and Highest Position Resolution for an Experiment at EIC

Rachid Nouicer, for the 4PISHDEIC Group
Brookhaven National Laboratory

SILICON PIXEL-BASED PARTICLE VERTEX AND TRACKING DETECTORS TOWARDS THE US ELECTRON ION COLLIDER WORKSHOP, September 02-04, 2020

Project Member: International Collaboration

Project members have extensive record on the construction of silicon detectors:

- **Silicon strip detector**
- **Silicon pixel detector**
- **Silicon hybrid pixel**
- **SOIMPXD**
- **UFSD: LGAD, AC-LAGD**
- **Silicon readout electronic**
- **Silicon assembly**
- **Cooling system**
- **Integration**
- **Commissioning**
- **And more**

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UNIVERSITY OF CALIFORNIA SANTA CRUZ

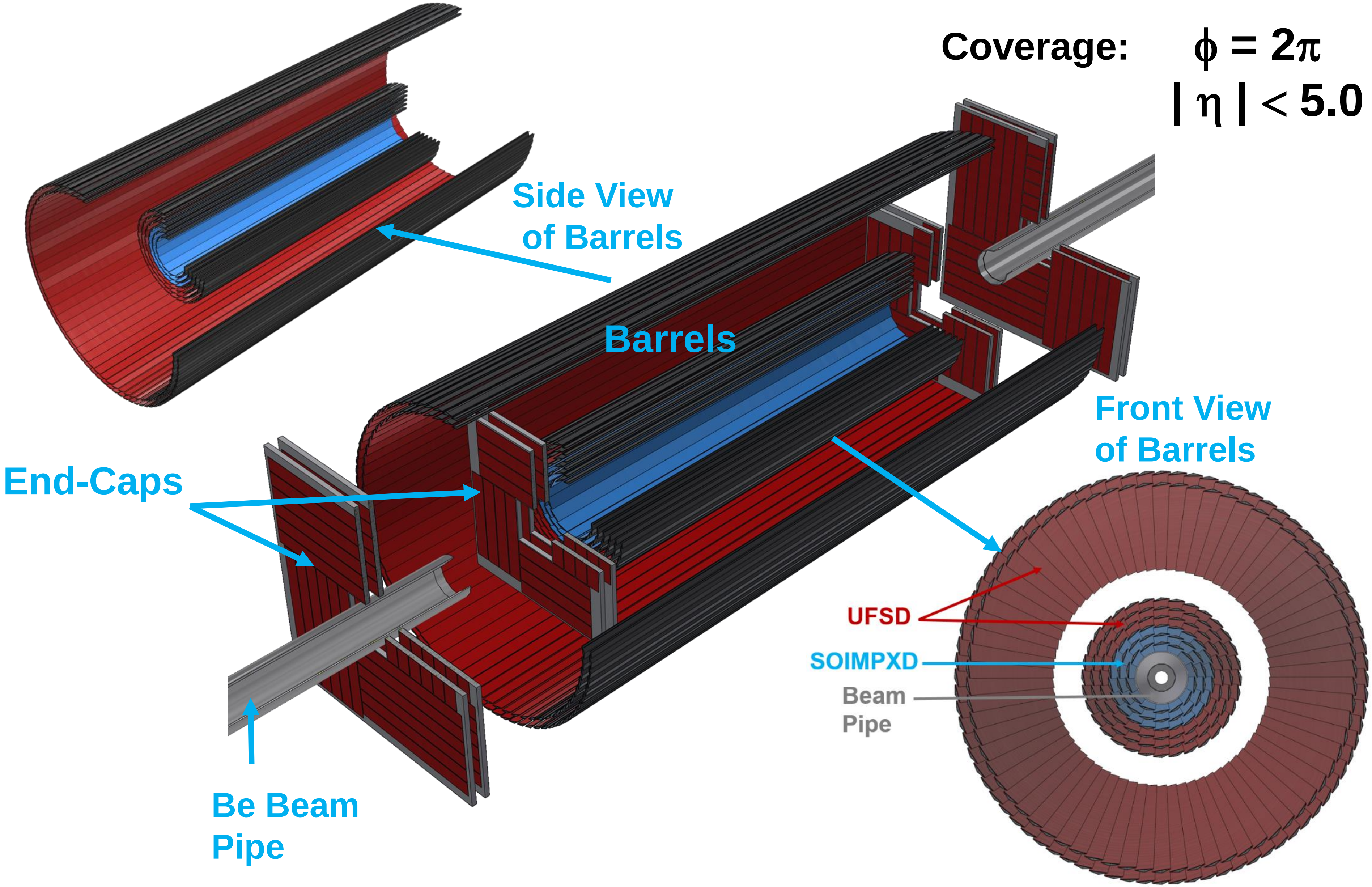
筑波大学 University of Tsukuba

We welcome people/institutions to join the project

4π Silicon Hybrid Detector = SOIMPXD + UFSD

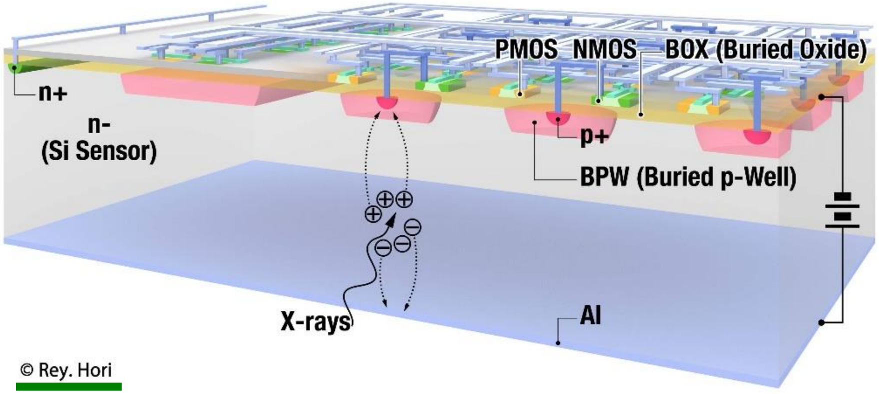
Coverage: $\phi = 2\pi$

$|\eta| < 5.0$



Why Silicon-On-Insulator Monolithic PiXel Detector (SOIMPXD) ?

- Monolithic device. No mechanical bonding.
- Fabricated with semiconductor process only → High reliability and Low Cost.
- High Resistive fully depleted sensor (50 um~700 um thick) with Low sense node capacitance → Large S/N.
- On Pixel processing with CMOS circuits.
- No Latch up and very low Single Event cross section.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology



Why Silicon-On-Insulator Monolithic PiXel Detector (SOIMPXD) ?

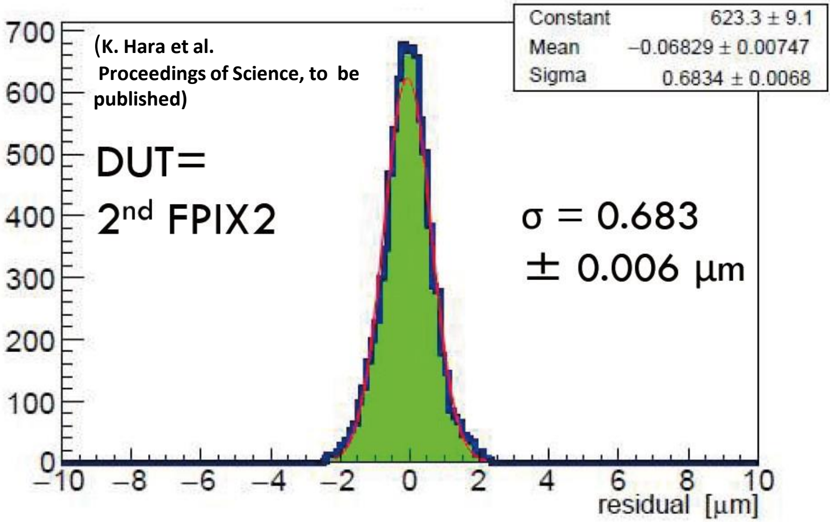
- **SOIMPXD has the best tracking position resolution in the world 0.68 μm, high radiation tolerance more than 10 Mrad (Si), time resolution ~ 1μs, and low material budget.**

Courtesy of Prof. Yuso Arai

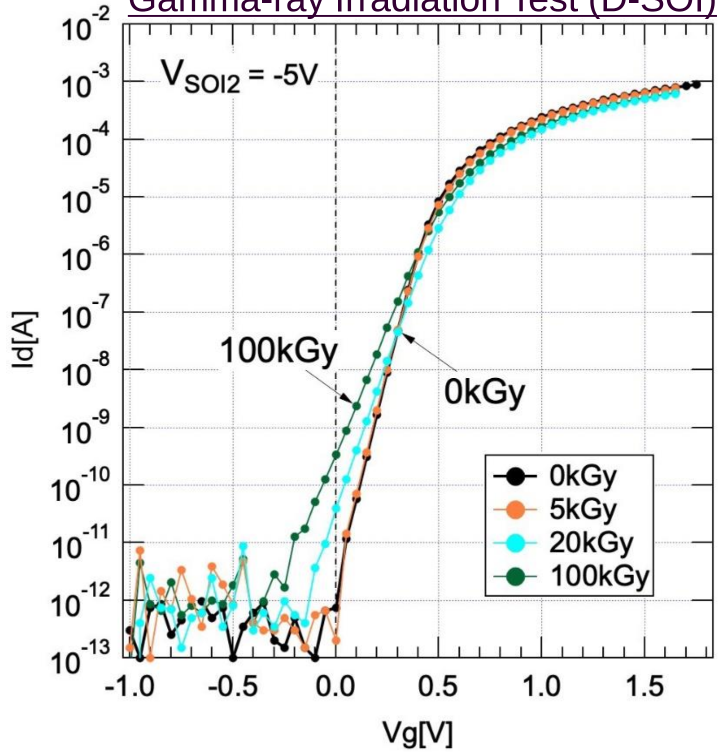
Tracking Resolution:

Proton beam 120 GeV @ FTBF 2018

D. Sekigawa et al. TIPP2018 →



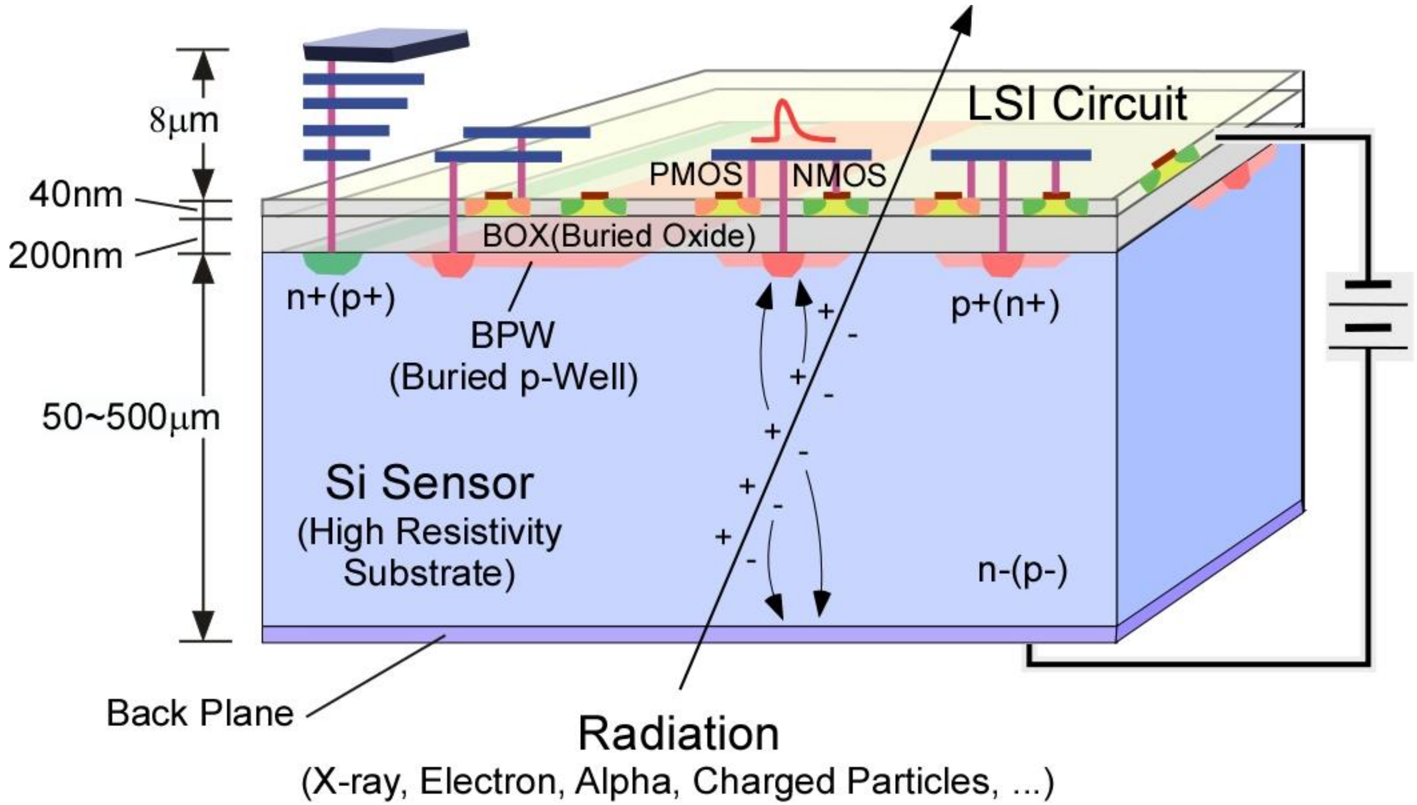
Gamma-ray Irradiation Test (D-SOI)



Detector	Pixel size	Resolution
ATLAS Pix	13.75 μm	1.1 μm
DEPFET	24 μm	1.4 μm
SOFIST	20 μm	**1.2 μm**
FPIX	8 μm	**0.68 μm**

Silicon-ON-Insulator Monolithic PiXel Detector (SOIMPXD)

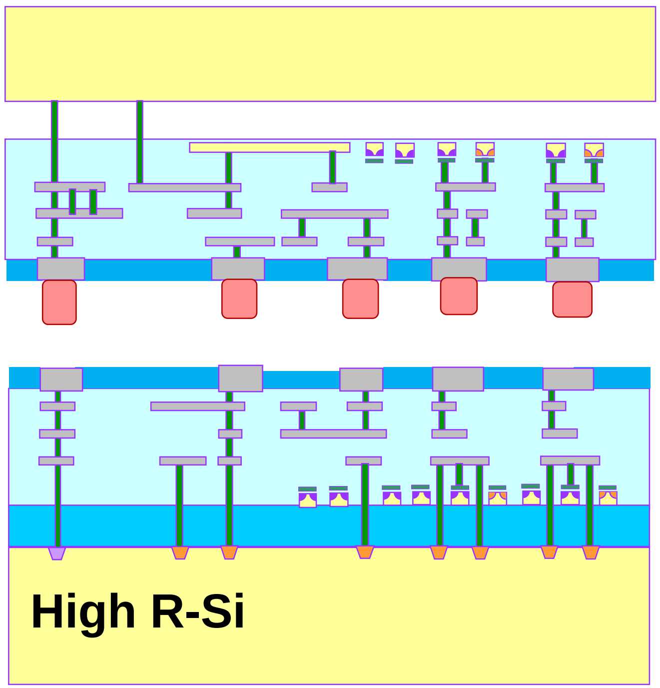
Courtesy of Prof. Yuso Arai



Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.

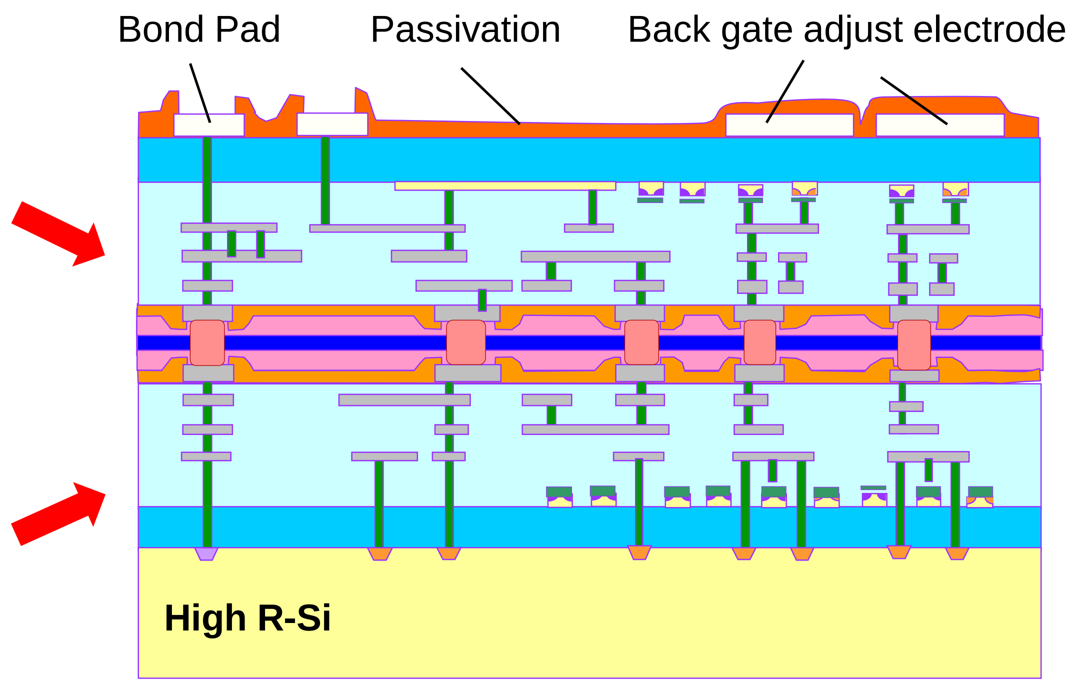
3D Vertical Integration

Upper Tier



Lower Tier

SOFIST Ver. 4

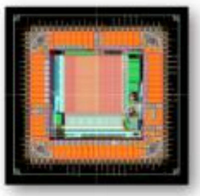
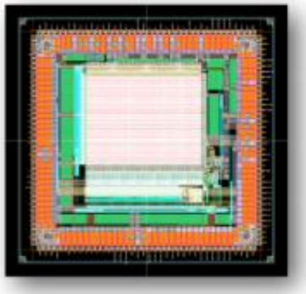
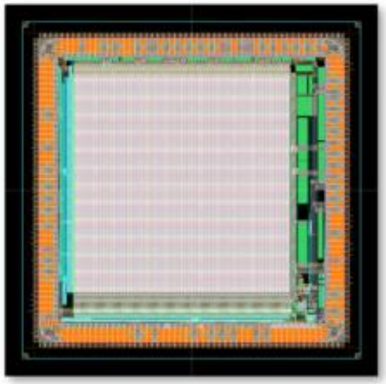
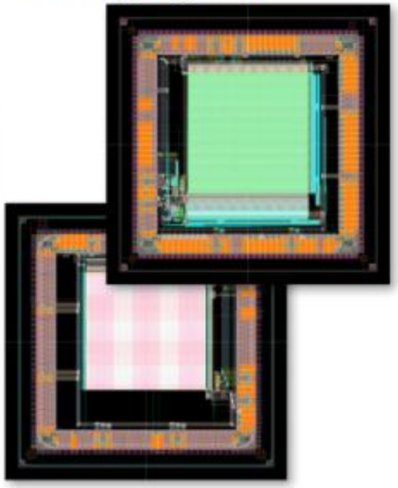


Upper and Lower Tier chips are produced in a same wafer and bonded chip to chip.

Extensive Program Achieved on SOIMPXD using Beam Test at FNAL

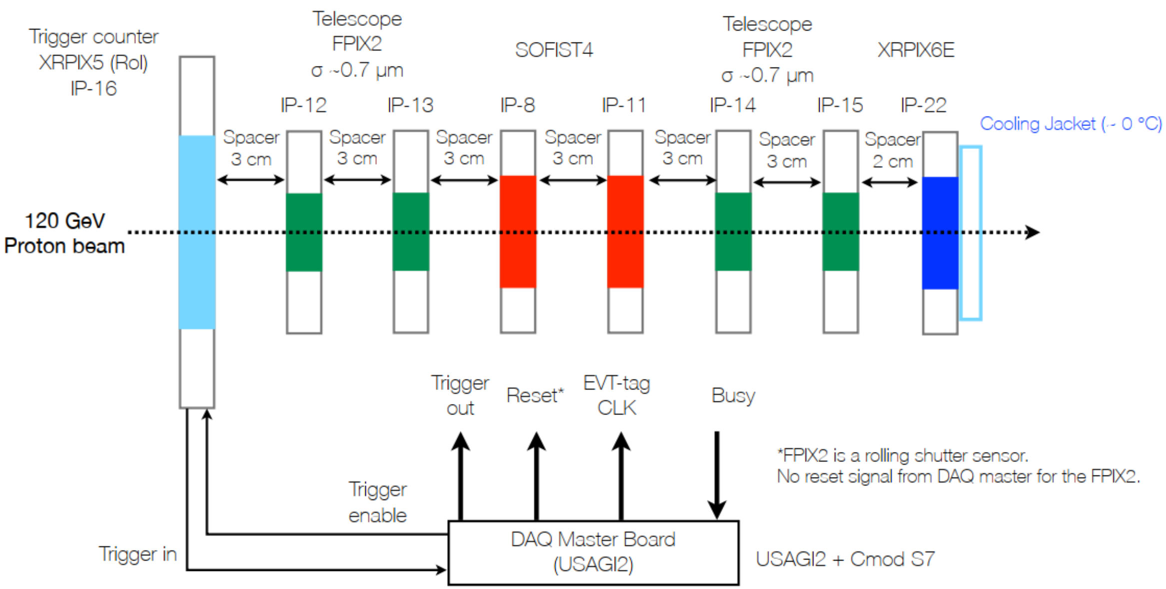
	SOFIST1	SOFIST2	SOFIST3	SOFIST4 (3D)
	Beam test at FNAL in Jan. 2017 Analog signal	Beam test at FNAL in Feb. 2018 Analog signal or Timestamp	Beam test at FNAL in Feb. 2019 Analog signal and Timestamp	Beam test at FNAL in Feb. 2020 Analog signal

Courtesy of Miho Yamada

	SOFIST1	SOFIST2	SOFIST3	SOFIST4 (3D)
Chip Size (mm^2)	2.9 × 2.9	4.45 × 4.45	6 × 6	4.45 × 4.45
Pixel Size (μm^2)	20 × 20	25 × 25	30 × 30	20 × 20
Pixel Array	50 × 50 (Analog Signal)	64 × 64 (Time Stamp) 16 × 64 (Analog Signal)	128 × 128 (Analog signal and Time stamp)	104 × 104 (Analog signal and Time stamp)
Functions (Pixel)	Pre. Amplifier (CSA) Analog signal memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 2) Analog signal memory (2 hits) or Time stamp memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n*-type (Single SOI)	Cz *p*-type (Double SOI)	FZ *p*-type (Double SOI)	FZ *p*-type (Double SOI)
Wafer Resistivity (kΩ·cm)	2 ≤	1 ≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Position resolution ~1.4 μm	Delivered (Jan. 2017) Time resolution ~1.55 μs	Delivered (May. 2018) Under evaluation	Delivered (Jan. 2019 ~)

SOIMPXD @ FBTF Feb. 26th - Mar 8th, 2020: 120 GeV Proton Beam



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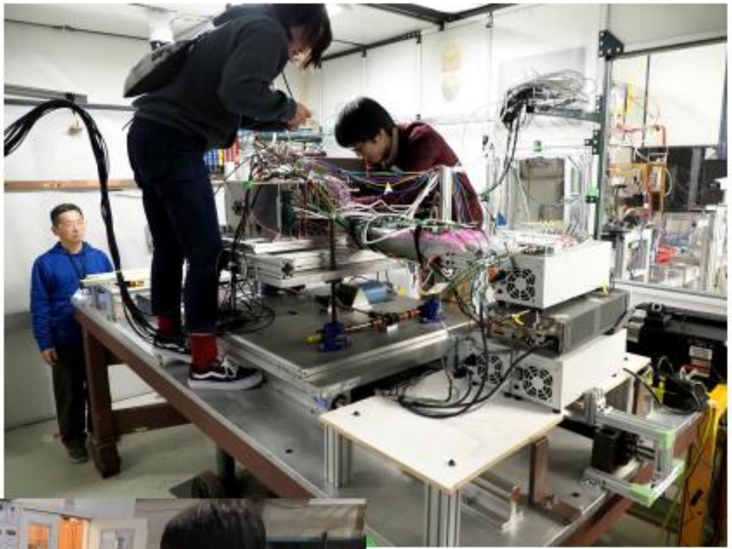
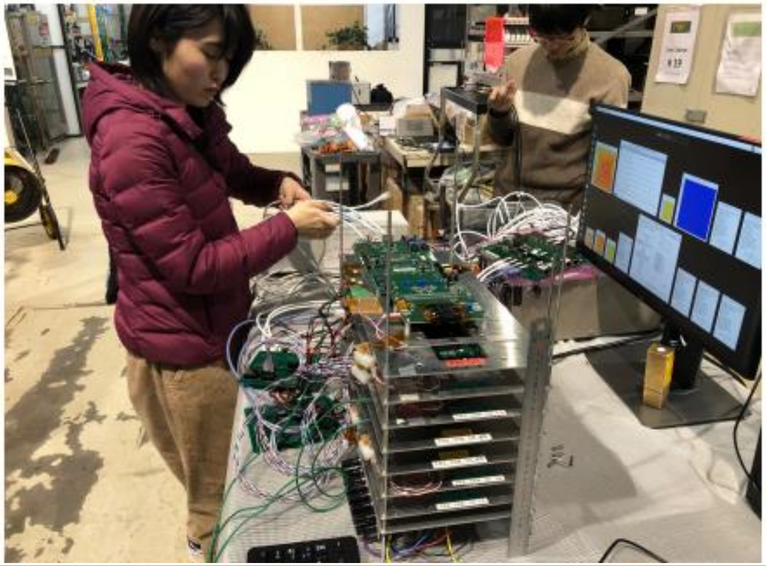
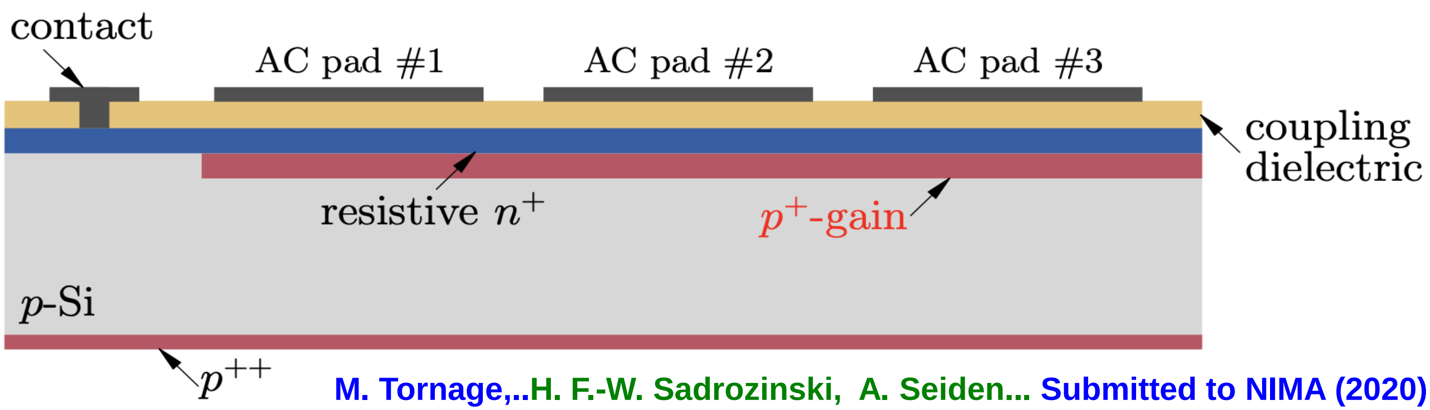




Why Ultra Fast Silicon Detector (UFSD) ?

- **Ultra Fast Silicon Detector (UFSD)** are thin pixelated silicon sensors - based on the Low Gain Avalanche Detector (LGAD) design which uses one extra implant during the sensor fabrication to achieve an intense electric field in a few micron region near the detector junction. The large electric field is able to start an avalanche multiplication for the collected electrons. The resulting large and fast signal allows the measurement of the particle hit time determination to be improved **from nanoseconds to picoseconds.** Developed by CNM Barcelona (Spain) first, HPK Hamamatsu (Japan), FBK Trento (Italy), and BNL (US).
- Can deliver the timing accuracy needed for ToF/PID and physics at the EIC
- Can be arranged in an array covering large areas as conventional silicon detectors for tracking
- The AC-LGADs are actually fairly simple compared to for example strip detectors (no large number of individual strips with polysilicon resistors) and not exceptionally difficult to fabricate, BNL was able to make them. Should result in reduced cost.

AC-LGAD: less complex sensor, no isolation structure needed for pads, continuous n and p implants for gain layer.



M. Tornage,..H. F.-W. Sadrozinski, A. Seiden... Submitted to NIMA (2020)

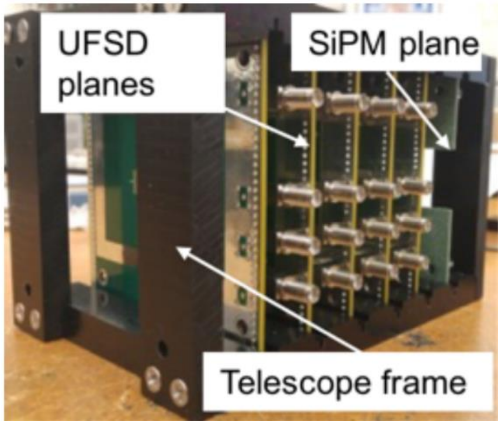
UFSD: Beam Test at CERN

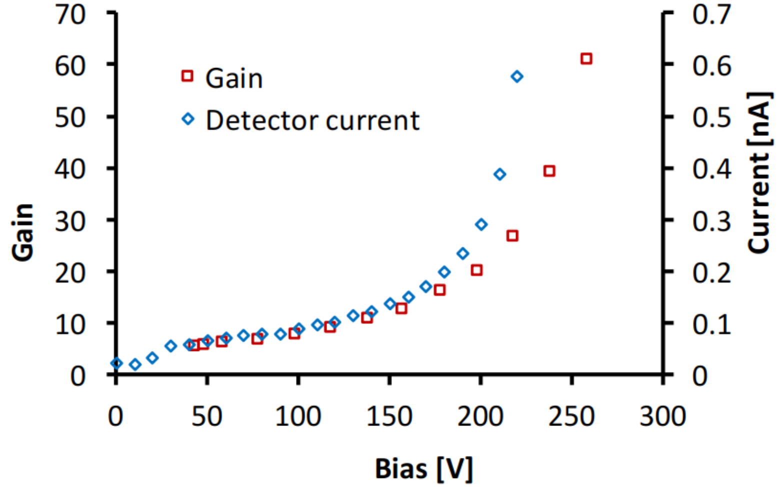
Results: Beam test with pions of 180 GeV/c momentum at CERN

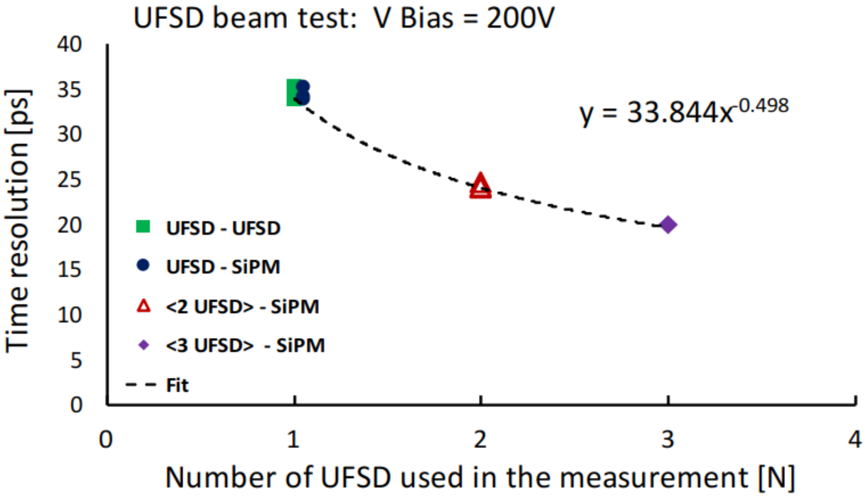
for the first production of 45 µm thick Ultra-Fast Silicon Detectors (LGAD).

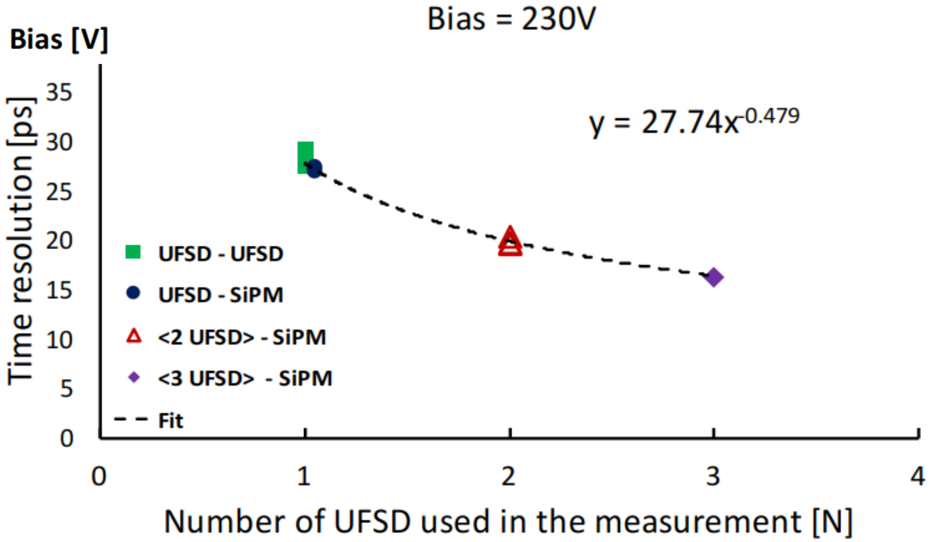
16 ps time resolution with three layers UFSD achieved, best in the world.

N. Cartigali,...,
H. F.-W. Sadrozinski,
A. Seiden...
NIM 850 (2017) 83.







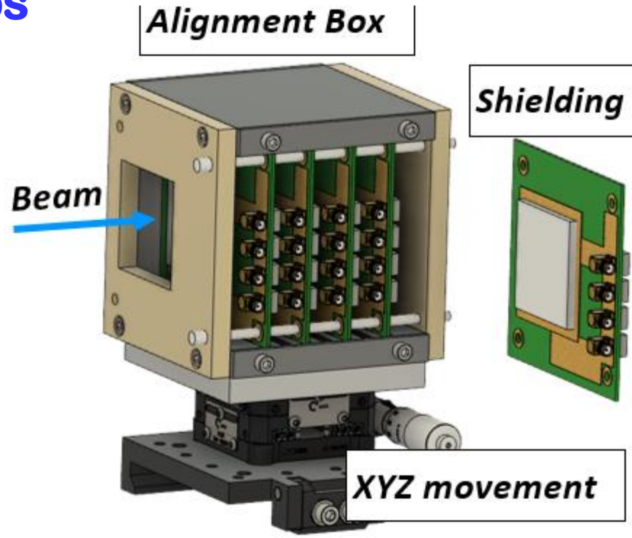


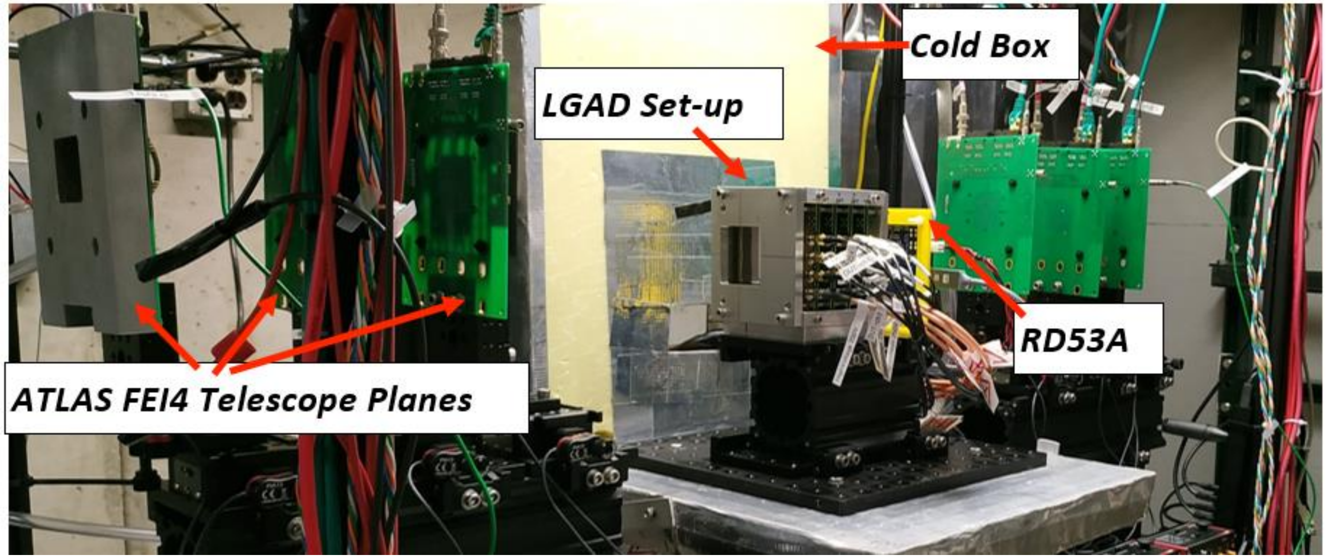
UFSD: Beam Test at Fermi Lab 2019

Achieved by ANL (Argonne) and UC (Santa Cruz) groups

Courtesy of Manoj Jadhav

- Proton Beam with momentum 120 GeV
- Objective of evaluation of time resolution for minimum ionising particles and effect of more than one sensor plane
- Four LGAD sensors placed in alignment box mounted on XYZ stage
- Sensors HPK 1.2 (35μm), 3.1(50μm) were tested
- Cold temperature measurements at -30 ℃ is achieved using FP89-ME Julabo Chiller
- Data were collected in spills of 4 sec duration and instantaneous trigger rate between 1 and 5 Hz were achieved





UFSD: Beam Test at Fermi Lab 2019

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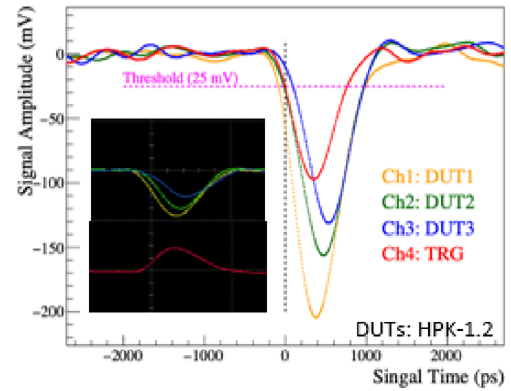
Courtesy of Manoj Jadhav

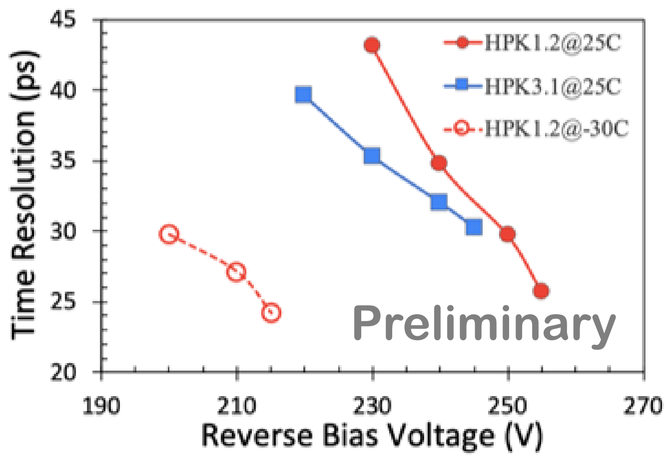
Timing Resolution

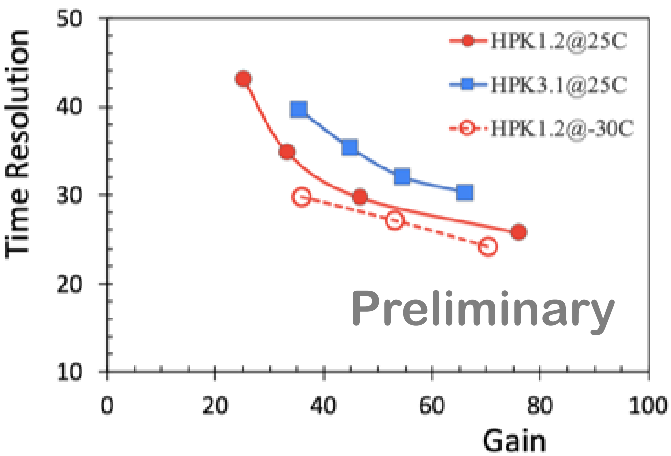
- Sensor leakage current were stable ~10-20 nA
- Very short rise time of ~350-400 ps were obtained
- Time resolution improvement at low temperature
- Figure below shows timing resolution as a function of bias voltage and the gain



Description of tested LGAD

Sensors HPK	Type	Thickness (μm)	Pad Area (mm²)	Capacitance (pF)	Rise Tiime (10-90%) (ps)	Breakdown Voltage (V)
1.2	n-on-p	35	1.3 × 1.3	5.35	375	270
3.1	n-on-p	50	1.3 × 1.3	3.9	470	245





UFSD: Beam Test at Fermi Lab 2019

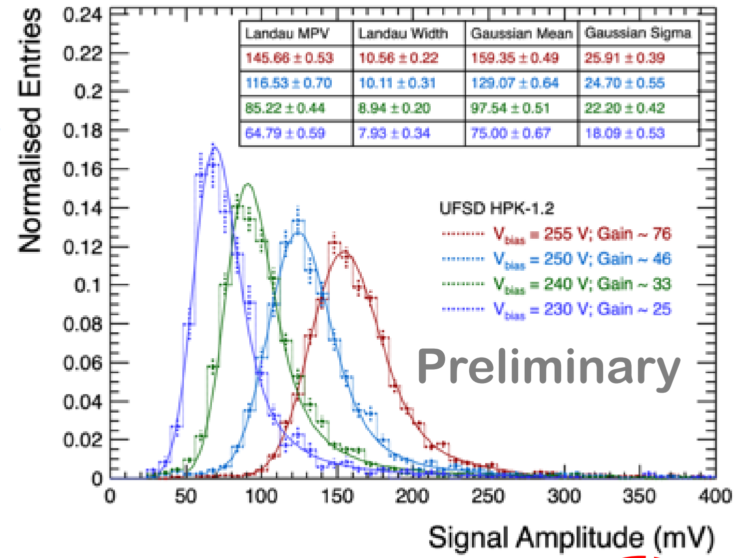
Achieved by ANL (Argonne) and UC (Santa Cruz) groups

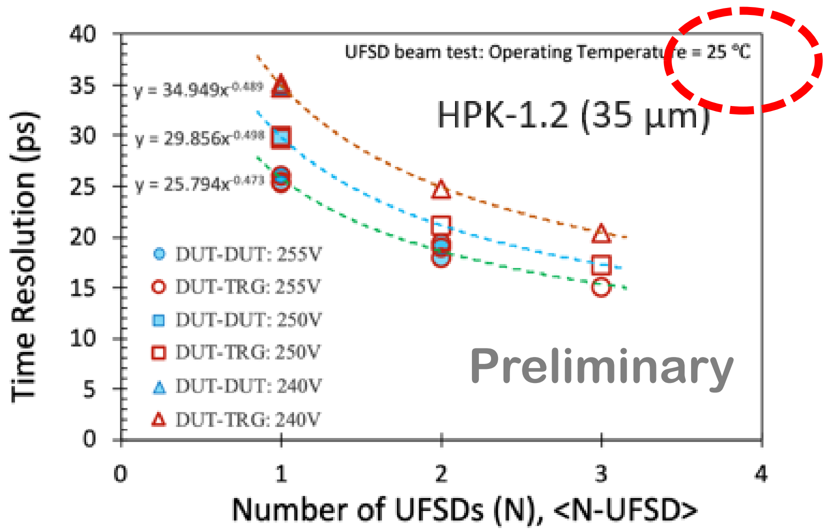
Courtesy of Manoj Jadhav

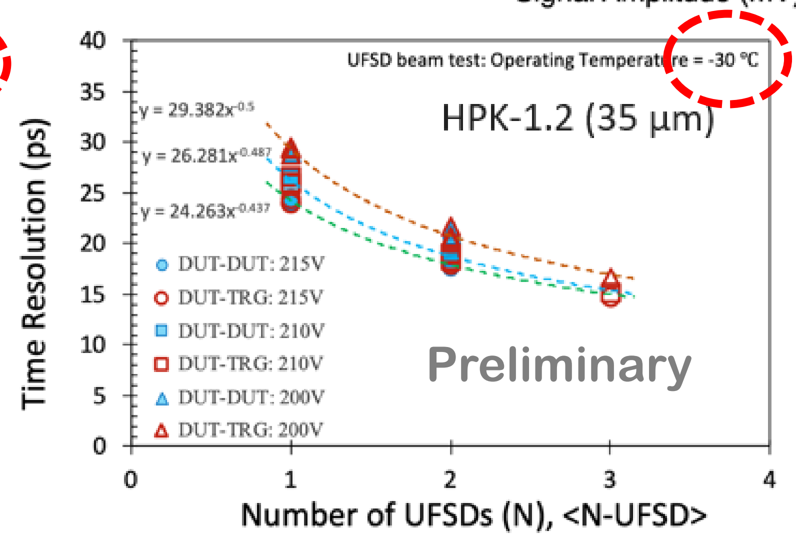
Timing Resolution: to be submitted for publication soon

- Achieved timing resolution of about 14.73 ps
- Normalized signal amplitude vs. Bias Voltage
- Time Resolution vs. No. Of UFSDs

HPK1.2	Vbias = 240V (25 °C)	Vbias = 255V (25 °C)	Vbias = 215V (-30 °C)
N = 1	34.78 ps	25.7 ps	24.17 ps
N = 2	24.77 ps	18.79 ps	18.11 ps
N = 3	-	15.04 ps	14.73 ps

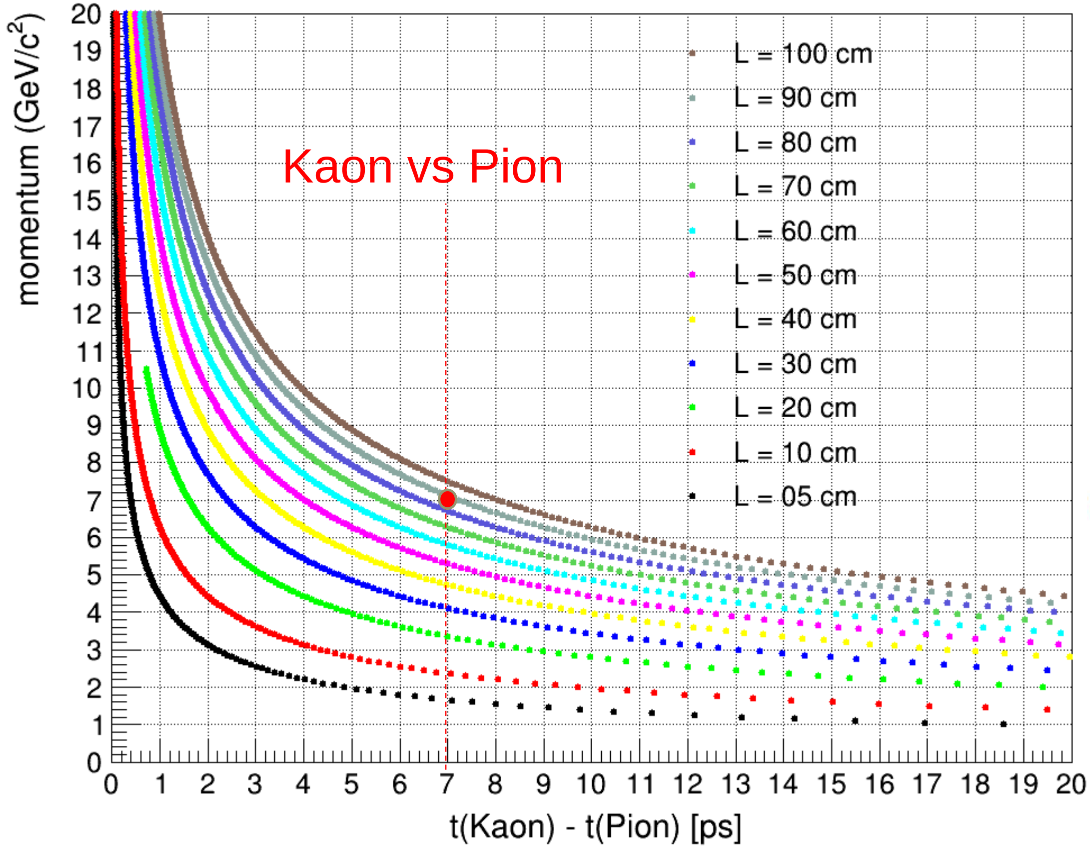






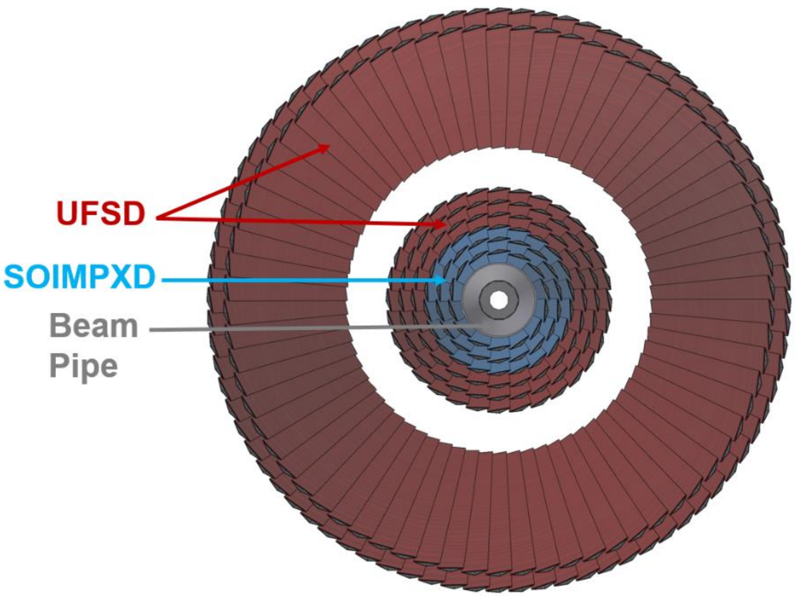
Why Ultra Fast Silicon Detector (UFSD) ?

- **3** layers UFSD (35 μm) → 15 ps time resolution (measured)
- Goal: UFSD (AC-LGAD) with 20 μm thickness of sensor → 5 to 10 ps time resolution
- **Basic Math: Two particles with the same momentum but different masses have different Time of Flight: this can be used for PID**



$$T_1 - T_2 = \frac{L}{c}\left(\sqrt{1+\frac{m_1^2}{p^2}} - \sqrt{1+\frac{m_2^2}{p^2}}\right)$$

L: path length (Silicon Barrel Position)



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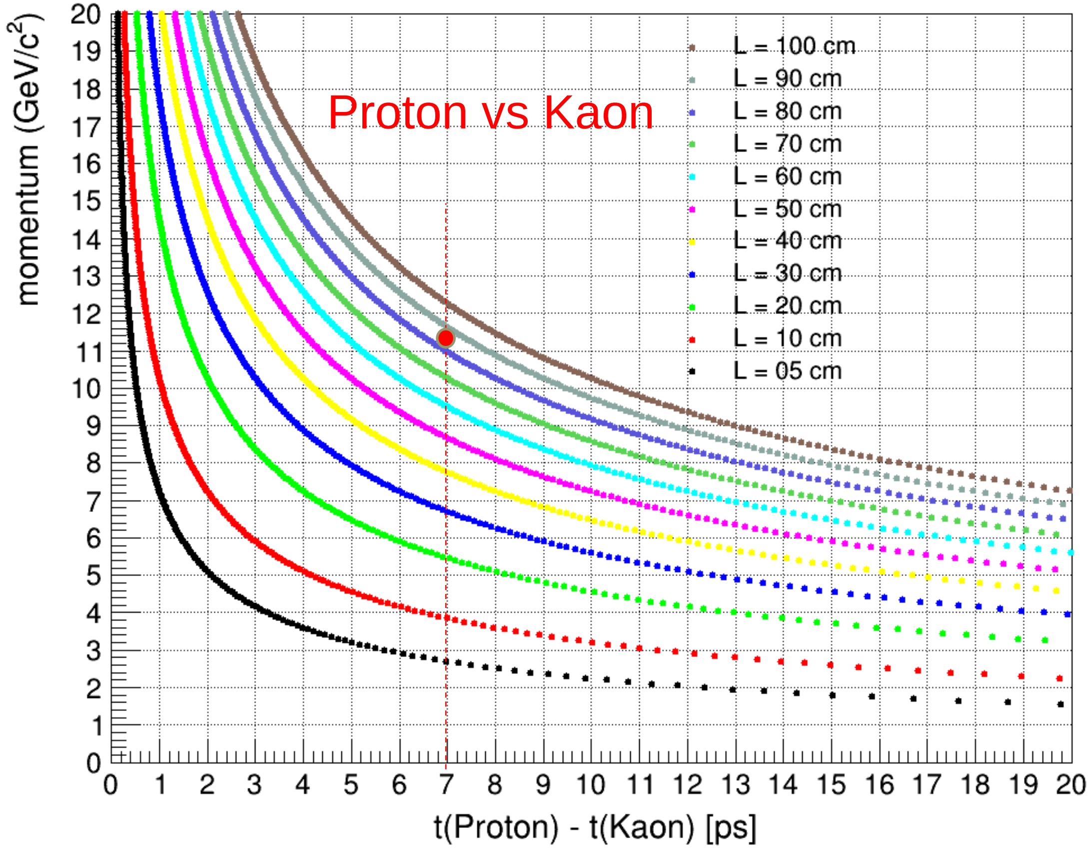

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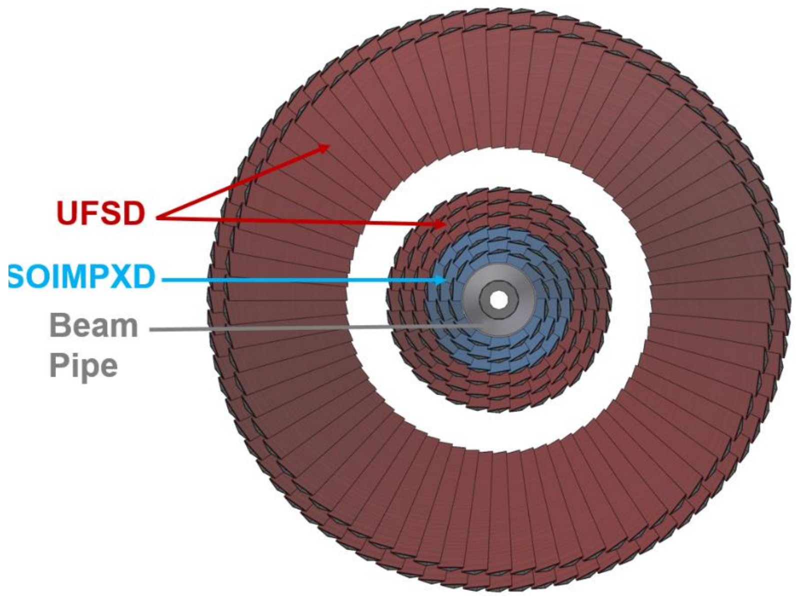
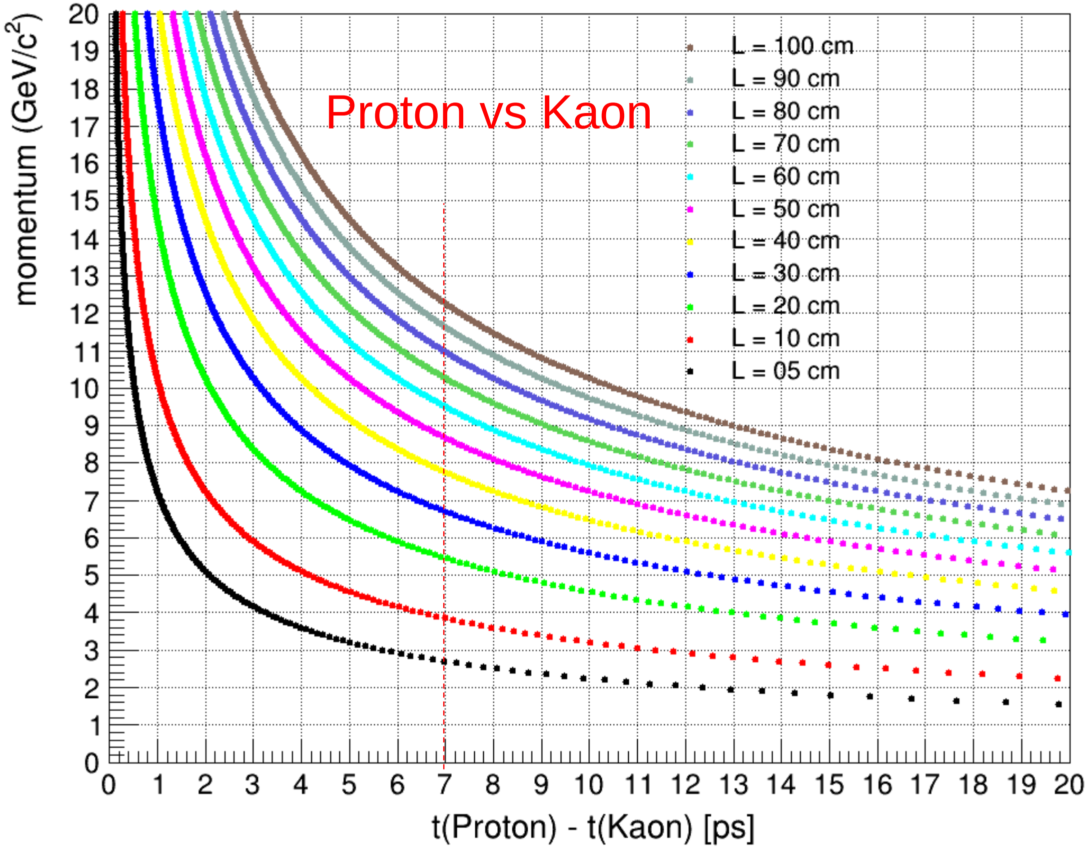


Simulation is needed to confirm PID with UFSD

Time of Flight: this can be used for PID



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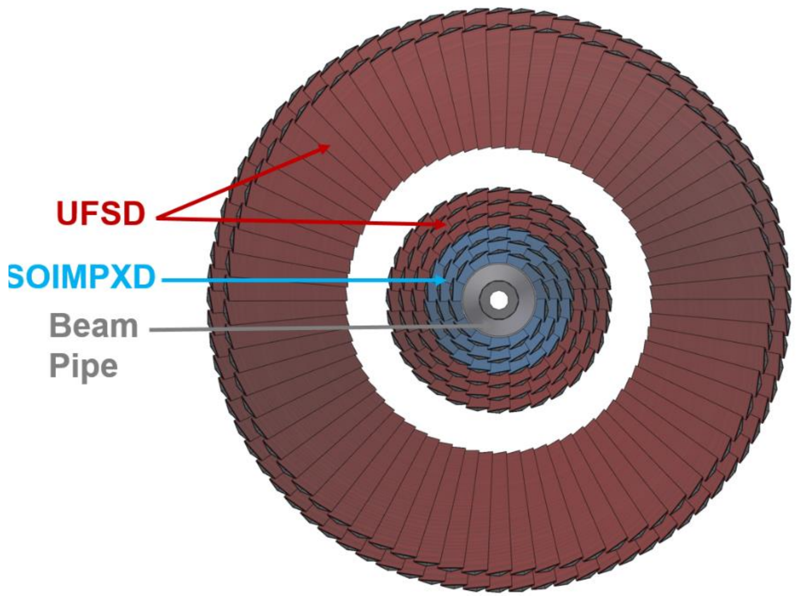

Summary

Silicon-On-Insulator Monolithic PiXel Detector (SOIMPXD) and Ultra-Fast Silicon Detector (UFSD) provide best of silicon detector technology for tracking and particle identification:

- SOIMPXD: best position resolution < 1 μm
- UFSD: best timing resolution < 16 ps (5 to 10 ps)

SOIMPXD + UFSD = Silicon Hybrid Detector is state-of-art of silicon detector technology which EIC can use to search for new physics discoveries.

Silicon Hybrid Detector = SOIMPXD + UFSD