CLAS12 Si Vertex Tracker - DAQ

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(Acknowledgement to Ben Raydo)

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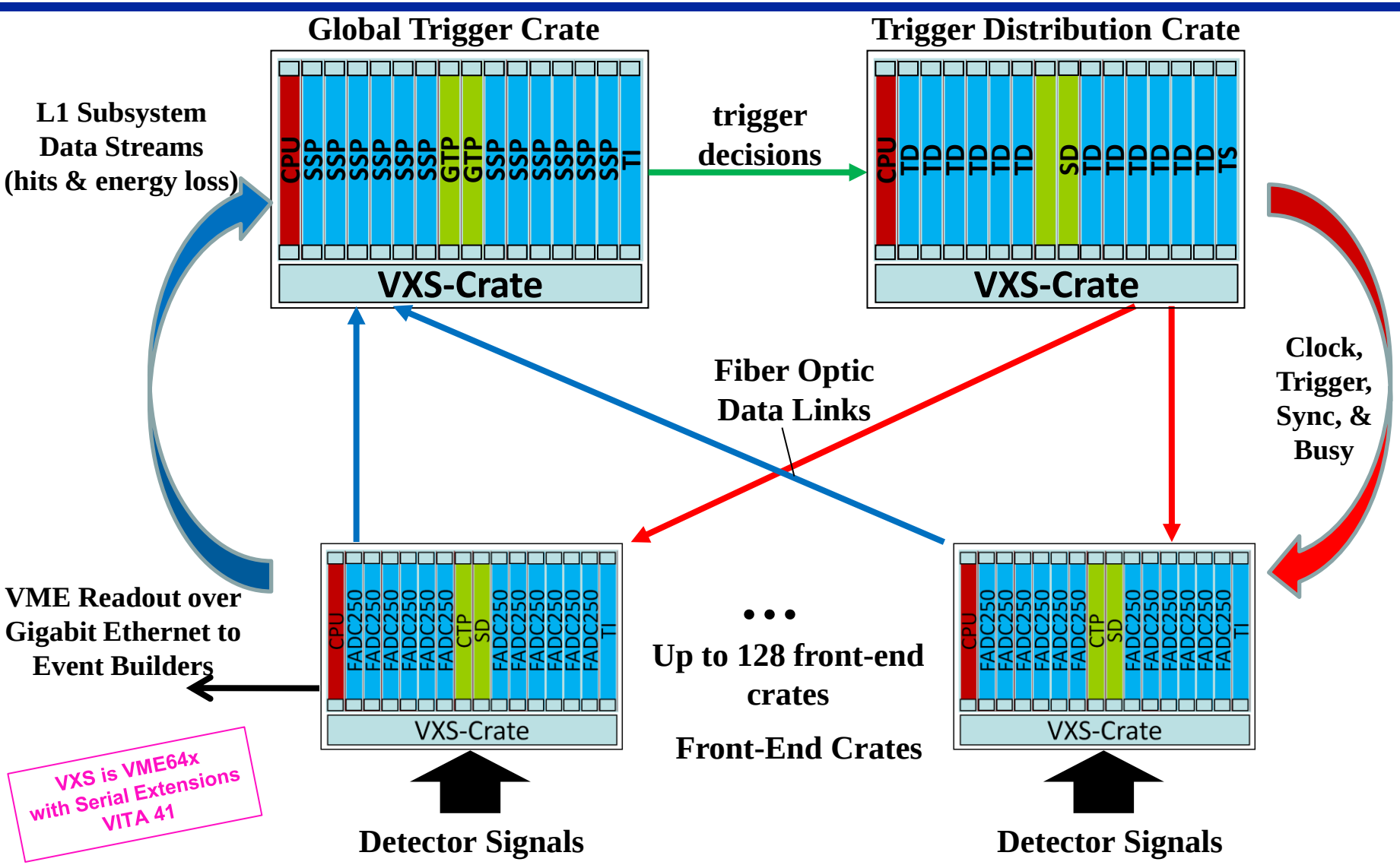
SVT DAQ Talk Overview

1. CLAS12 Trigger/DAQ
2. VXS Silicon Control Module (VSCM)
3. Summary

12GeV DAQ/Trigger System for Hall B/D



VXS is VME64x
with Serial Extensions
VITA 41

Front-End Triggering

Beam structure:

- Electron bunches ~2ns apart [499MHz]

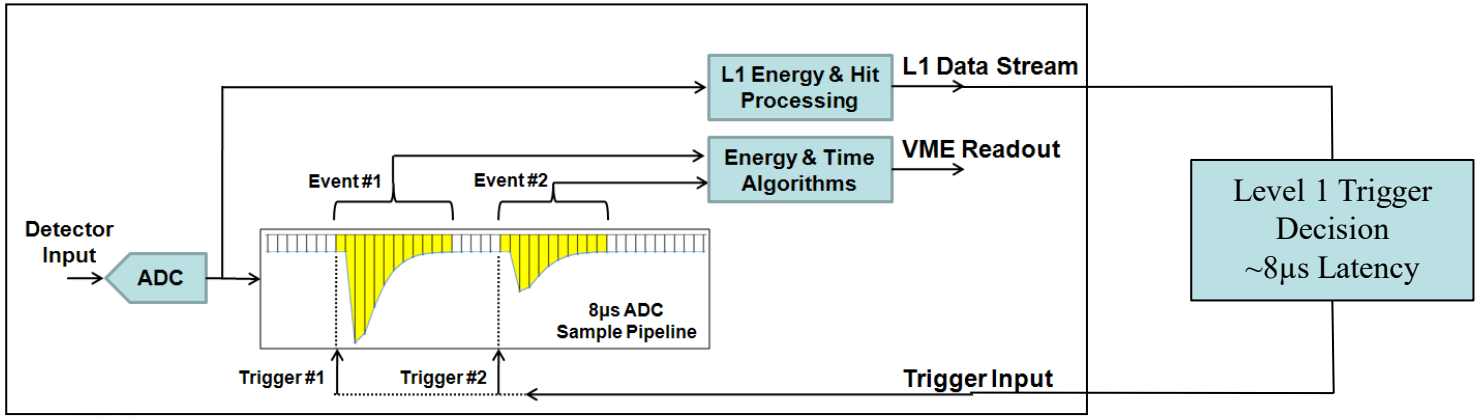
Free running Trigger:

- Front-end electronics continuously sample detector, feeding data into L1 processors, and storing in a local pipeline buffer
- When L1 trigger condition exists (e.g. based on energy deposition, cluster patterns, tracks, hits) L1 accept pulse is distributed to all front-end crates

L1 Trigger Acceptance:

- When a module receives a L1 accept pulse, it processes a time window in its front-end sampling buffer and builds an event for readout. The processing time window is defined by two parameters:
  - **Lookback**: processing starts parsing data M clock cycles before L1 accept was received
  - **Window Width**: processing parses all data N clock cycles wide after look-back point

Typical Front-End Module:



Hall B DAQ & FSSR2

General Hall B DAQ Requirements

- L1 trigger rate: 10kHz
- L1 maximum trigger latency: 8µs
- Dead time: minimal

FSSR2 / HFCB needs additional hardware to interface the Hall B DAQ

- The FSSR2 uses a data-driven (high bandwidth) event output, but Hall B DAQ needs triggered event data (low bandwidth)
- FermiLab Silicon Strip Readout ASIC; TSMC 0.25um CMOS

So the VXS Silicon Control Module (VSCM) was developed...

VSCM – Design Features

VSCM was designed to interface the FSSR2 readout/controls to the Hall B DAQ.

All features have been implemented and tested

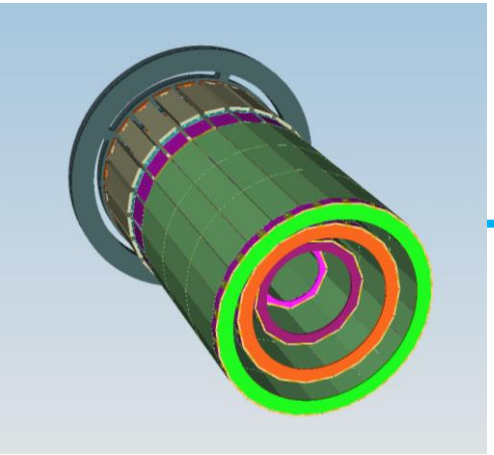
- **VXS Based Module**

- **Supports 2 Jlab Hybrid Flex Circuit Board (HFCB) Interfaces per VSCM module**
  - 8 FSSR2 chips per VSCM (4 per HFCB)→ **1024 strips per VSCM**
  - 6 readout lines per FSSR2 @ 70MHz DDR for 840Mbps operation
  - Programmable BCO clock period (128ns to 256ns)
  - BCO clock synchronized to CLAS12 global trigger clock
  - FSSR2 slow control interface accessible through VME registers

- **Event Builder**
  - >100kHz Trigger Rate, 8μs Trigger Latency, <1% Dead-time
  - 2Mbyte multi-event buffer (storage for ~500,000 triggered strip hits)
  - VME readout: 2eSST @ 200MB/s, multi-event blocking supported
  - Programmable capture window
  - Status words & hits not in defined trigger time window are suppressed from readout

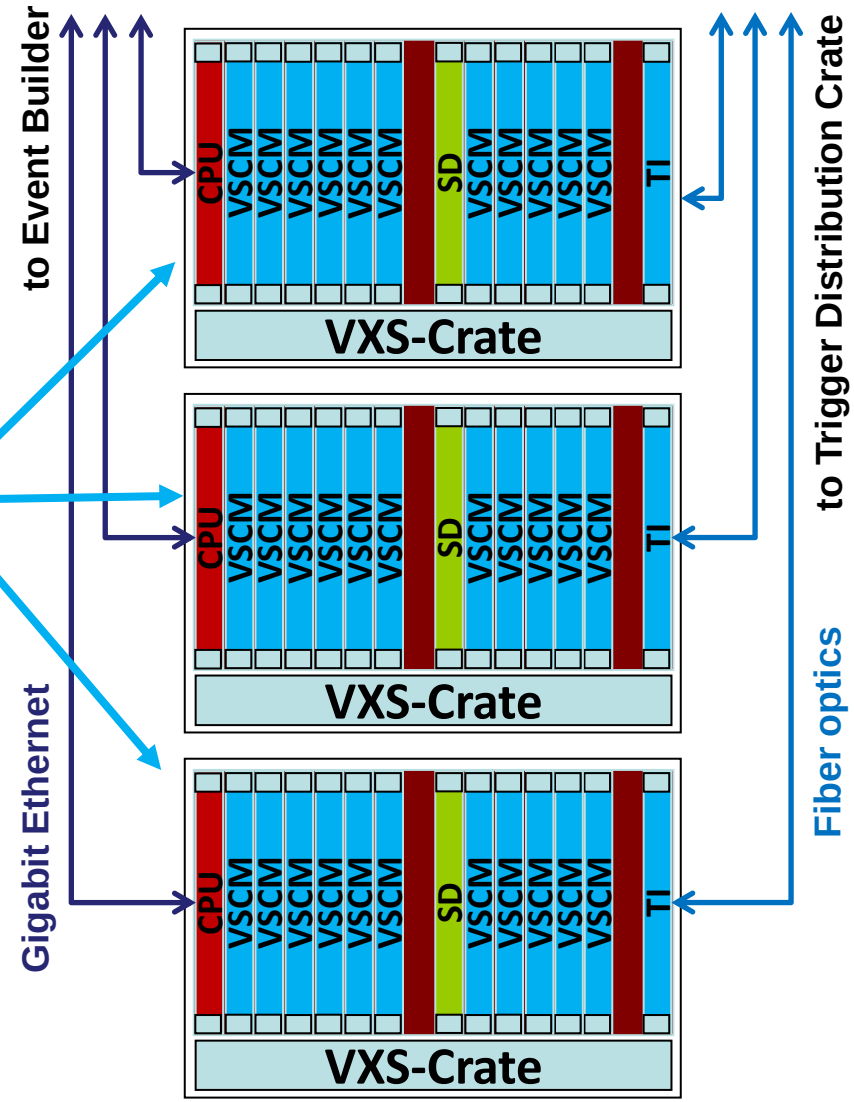
- **Diagnostics**
  - 32bit scaler for every strip
  - Arbitrary pulser for each HFCB (synchronous to BCO clock)
  - Continuous status & event word monitors used for error checking & synchronization

SVT: DAQ Crate Layout



~5m length

66x High Density Round Shielded (100ohm twisted pair)



**** See Presentations from Y. Gotra and B. Eng for SVT Detector details.***

VSCM - Quantities

Region	Si-Modules/HCFB BST Count	VSCM Count
1	10	5
2	14	7
3	18	9
4	24	12
Totals	66	33
	264 FSSR2 chips	
	33792 Si strips	

Support for 33 VSCM requires the following crate configuration (3 crates total):

1) 21 Slot VXS Crate
2) VME CPU
3) Signal Distribution Modules (SD)
4) Trigger Interface Modules (TI)

This is the standard Hall B & Hall D 12GeV readout crate configuration

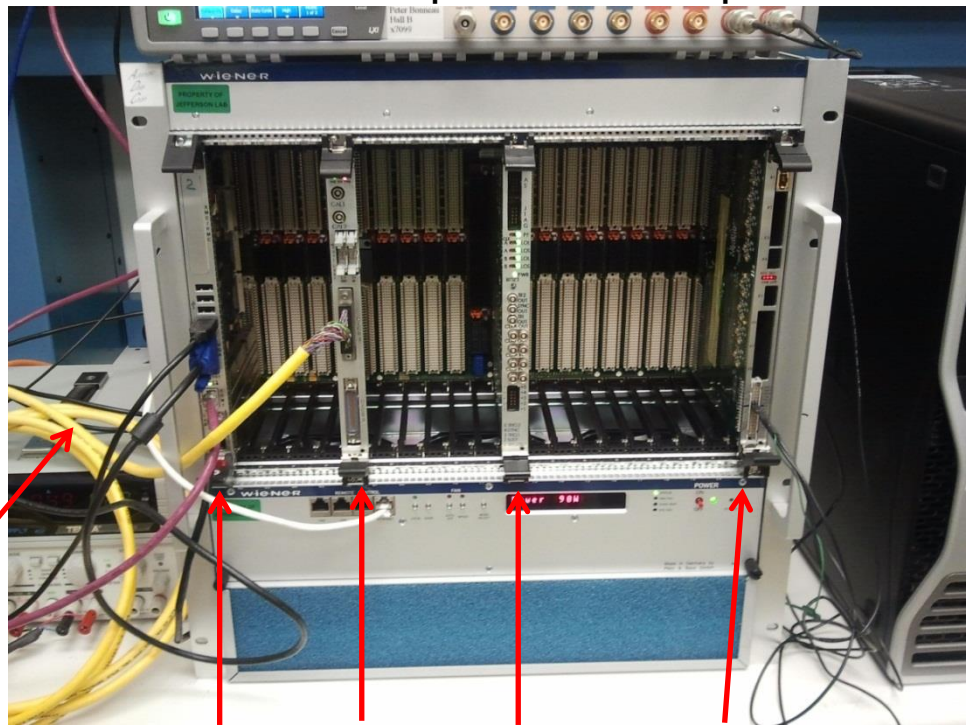
5) VSCM (11 per crate)

This is the only new DAQ component needed by the SVT system

SVT: DAQ Crate Components

SVT DAQ Components

- CPU: Commercial VME Controller (Intel 2.53GHz Core i7, 4GB DDR3 SDRAM)
- Crate: Commercial VXS Crate (Wiener 21 Slot VXS Crate)
- SD: Signal Distribution VXS Card (Standard JLab 12GeV Component)
- TI: Trigger Interface VXS Card (Standard JLab 12GeV Component)
- VSCM: VSCM VXS Card – SVT specific development



VSCM – PCB Assemblies

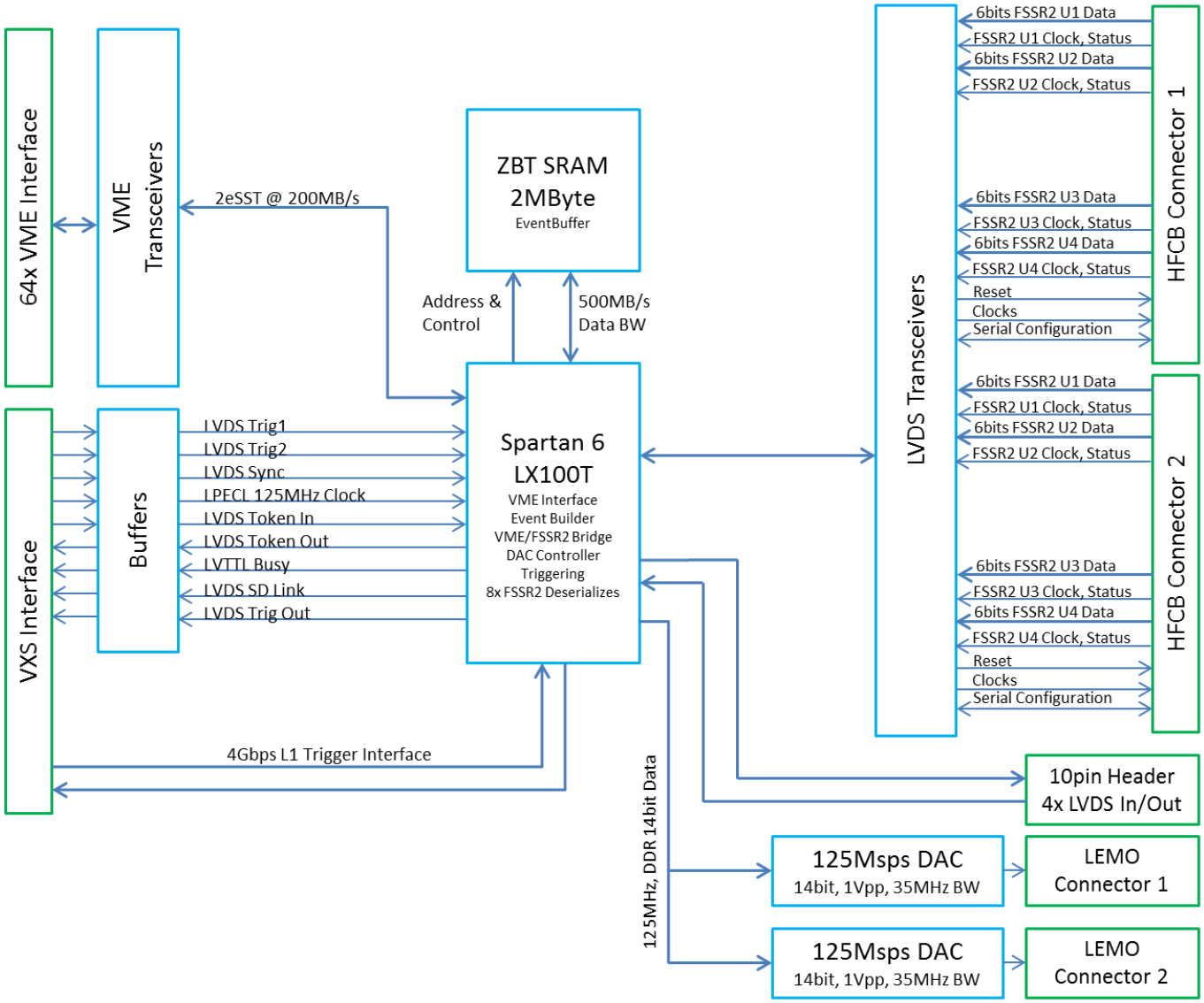
VSCM Prototype:

- Used in SVT 2012 beam test
- Used in SVT test stands for HFCB testing
- A few wires needed to get things working

VSCM Production:

- Cleaned up prototype/simplified design
- Used in SVT test stands for HFCB testing

VSCM – PCB Block Diagram



VSCM Event Structure

VSCM Event Structure

Structure Element	Size (bytes)	Element Information
Block Header	4	Block Number: 11bits VME Slot: 5bits EventsPerBlock: 11bits
Event Header	4	Event number: 27bits
Trigger Timestamp	8	Timestamp: 48bits (~13 day rollover)
SVT Hit	4	Pulse Height: 3bits BCO Number: 8bits Strip Number: 7bits Chip Identifier: 3bits Hit->Trigger Timestamp: 10bits
SVT Hit	4	
…		
SVT Hit	4	
…		
Event Header	4	
Trigger Timestamp	8	
SVT Hit	4	
Block Trailer	4	Block Word Count: 22bits VME Slot: 5bits

*** Redundant information used for consistency checking**

Maximum Channel Occupancy:

Conditions:
TriggerRate = 10,000Hz
CrateReadoutBandwidth = 115MB/s
StripsPerCrate = 11*128*8 = 11264
EventsPerBlock = 16
VSCMModulesPerCrate = 11

Calculations:
VSCM Event Size (Bytes):

$$12+4*N_{hits}+8/N_{eventsPerBlock}$$

CrateEventSize = 11,500bytes
MaxOccupancy (sustained) = 24%

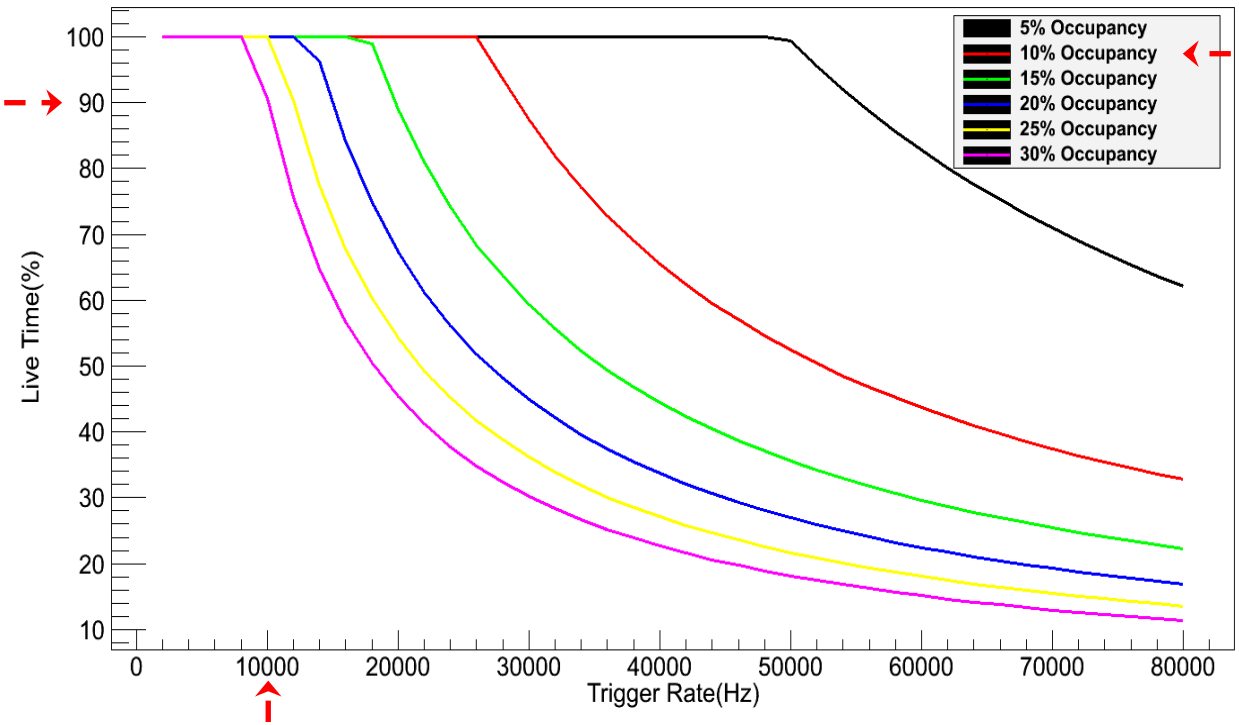
Comments:
-Bottleneck is CPU gigabit Ethernet link
-VSCM buffering support occupancies at 100% for several hundred sequential events before dead-time occurs
-Could pack 2 hits per 32bit word, doubling occupancy capacity

VSCM DAQ Efficiency

VSCM DAQ provides significant margin (assuming 10% FSSR2 occupancy):

- Up to 30kHz trigger rate (20kHz margin)
- 100% live time (10% margin)
- Up to 25% FSSR2 occupancy (2% occupancy realistic for FSSR2 high efficiency)

CLAS12 Acceptable Live Time

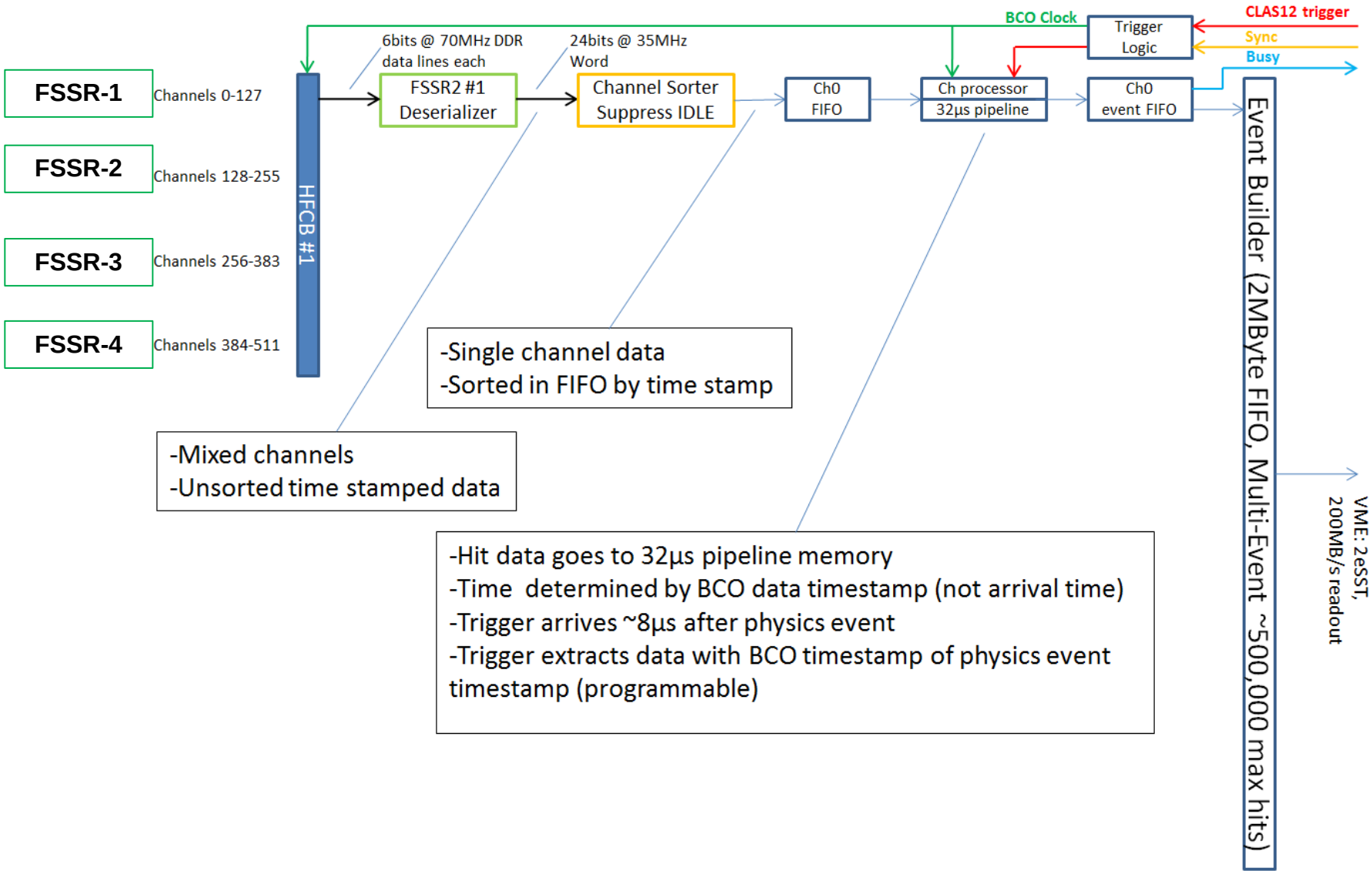


FSSR2 Hit Occupancy

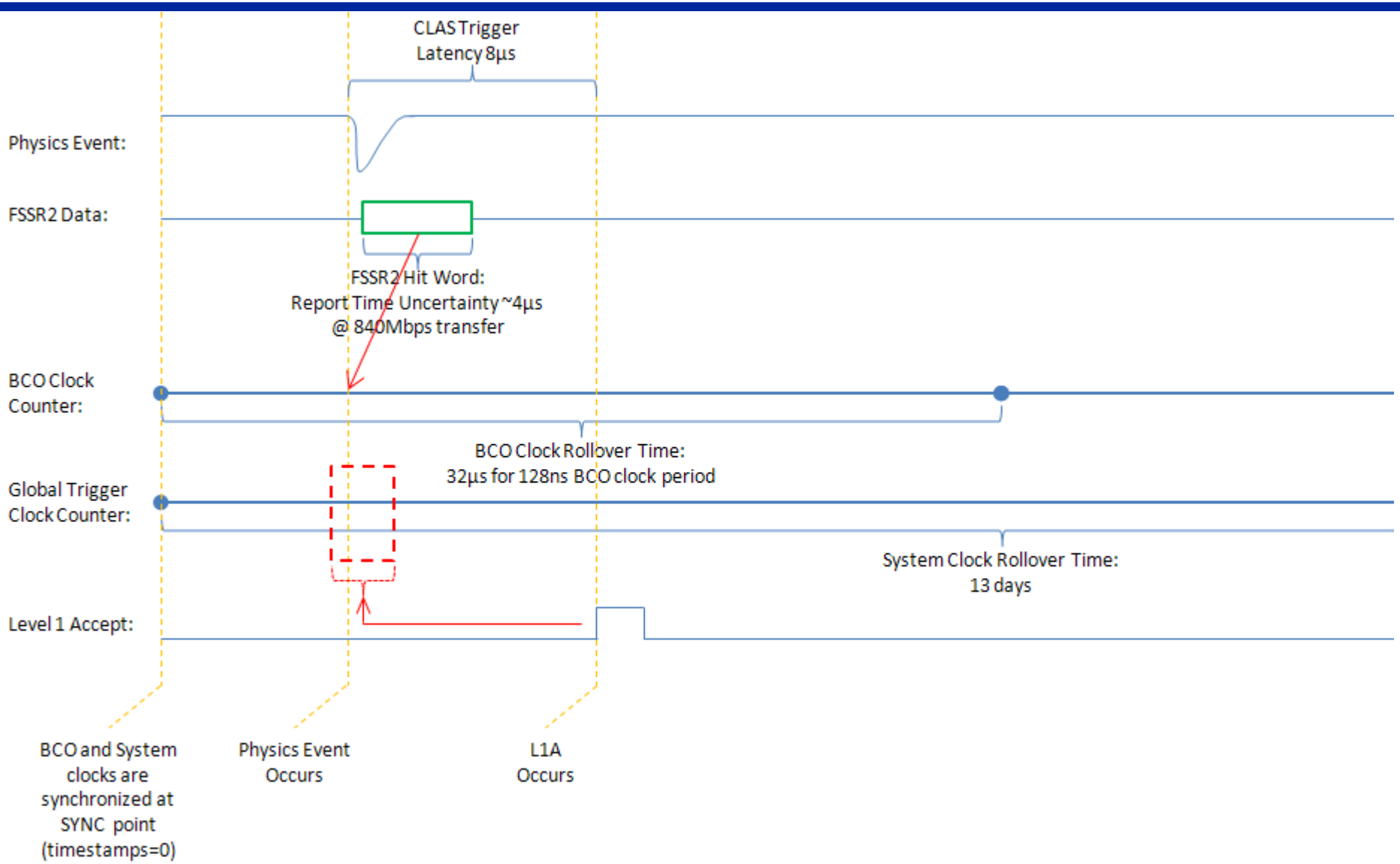
CLAS12 Trigger Rate

Plenty of margin!

VSCM – Event Building (Single Strip Shown)



VSCM Event Triggering



VSCM Firmware Status

- Initial release for 2012 SVT test run stable, though a few important bugs were identified and fixed
- **Current release is stable, no outstanding bugs**
- FPGA resource utilization has room left for future features:

Resources Show Graph

RTL Estimation | Synthesis Estimation | Netlist Estimation | **Implemented Utilization**

Part: xc6slx100tfgg676-3

Resource	Utilization	Available	Utilization
Register	22780	126576	17%
LUT	19468	63288	30%
Slice	8345	15822	52%
IO	327	376	86%
RAMB16BWER	21	268	7%
RAMB8BWER	218	536	40%
ICAP	1	1	100%
PLL_ADV	3	6	50%
BUFG	14	16	87%
BUFGMUX	1	16	6%

VSCM Production Status

VSCM Production of 40 Modules Complete:

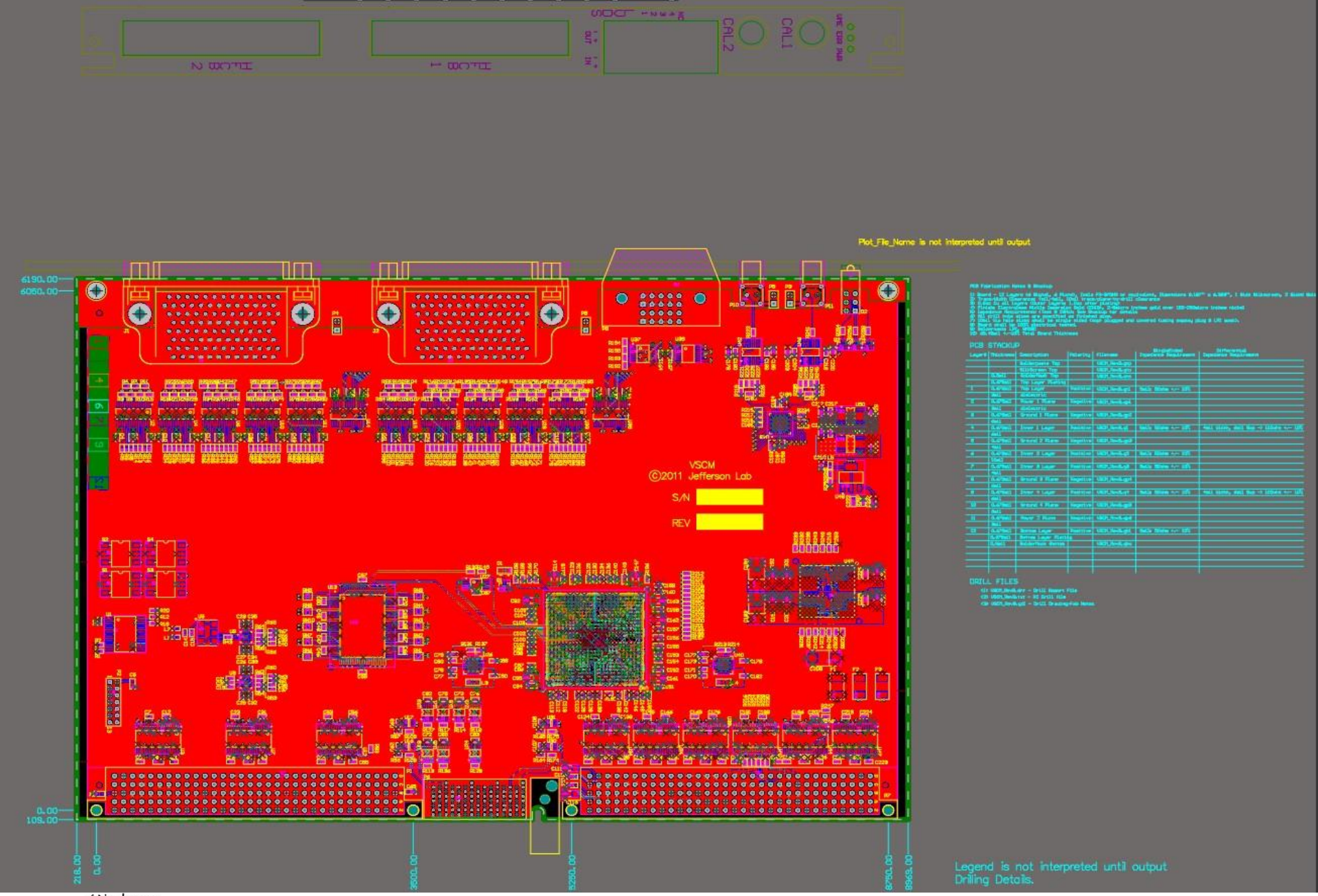
- First articles (3) received and evaluated Nov 2012 – Jan 2013 **(No issues found!)**
- **Remaining production run (37) completed Feb 2013**
- Production run testing is in progress

Summary

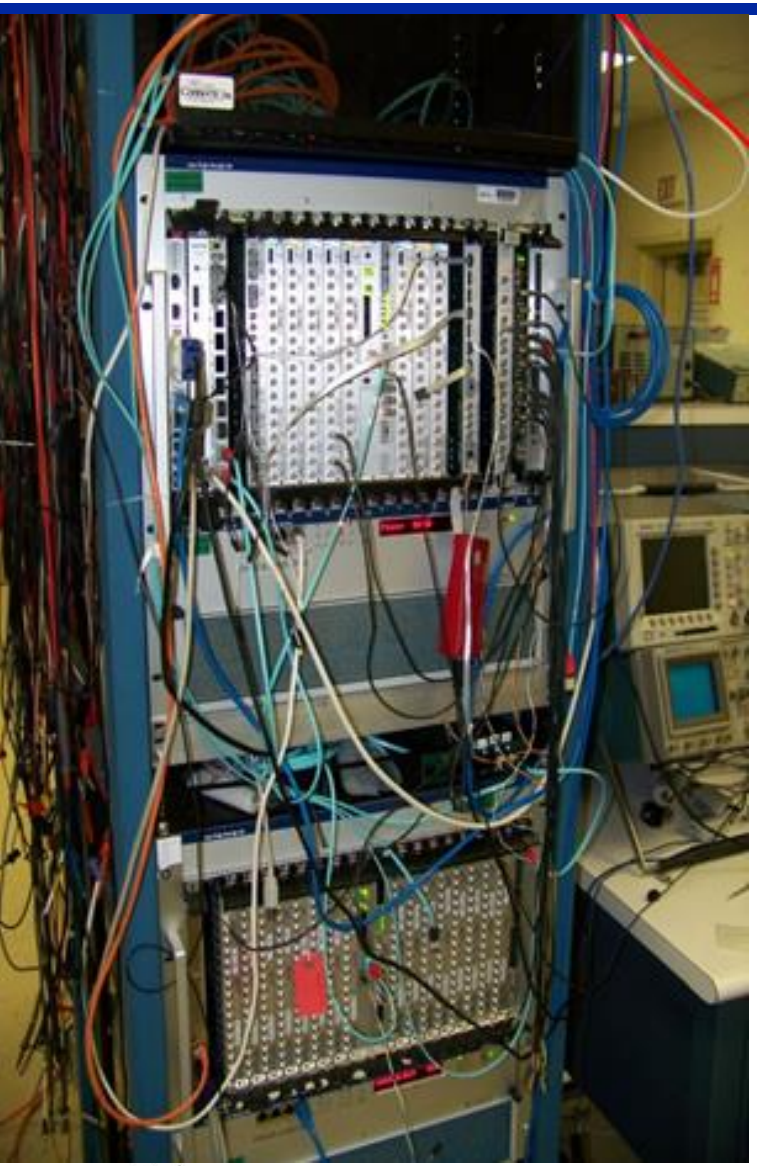
- VSCM has been very successful for control and readout of FSSR ASICs in the CLAS12 Silicon Strip Vertex Tracker.
- VSCM module could be used for other ASICs or Front-END Detector electronics.
- VSCM module includes high speed serial link to VXS Trigger Processor central switch module for higher level triggering functions. Possible features could include Streaming ReadOut options.
- Group is very experienced with analog and digital electronics design, including modeling, simulation, firmware and test verification.

- Questions?

Thank You!


Plot_File_Name is not interpreted until output
VSCM
©2011 Jefferson Lab
S/N
REV
PCB STACKUP
DRILL FILES
Legend is not interpreted until output
Drilling Details.

VXS Full Crate DAQ Tests



- A multi-crate prototype of the 12GeV DAQ/trigger system was completed successfully in 2009
- The test was with production hardware (2 Crates, 512 Flash ADC channels, TI, TD, SD)
- Larger scale tests (~15 crate system) is planned to start in April 2013

DAQ Status

Activity	Details	Status
VXS Crates	Commercial Product – Tested	**Received in full**
VME CPU	Commerical Product – Tested	**Received in full**
TI	Jlab Development – Tested	**Received in full**
SD	Jlab Development – Tested	**Received in full**
VSCM	PCB assembly – (First articles tested)	**Received in full**
	Firmware development	**Stable release**
	VSCM & HCFB integration	**Complete**
	SVT DAQ system integration w/Hall B DAQ	**Test run 2012 – Complete** Full SVT DAQ system – In progress

SVT DAQ in great shape!