The ALICE ITS3 Project: progress report

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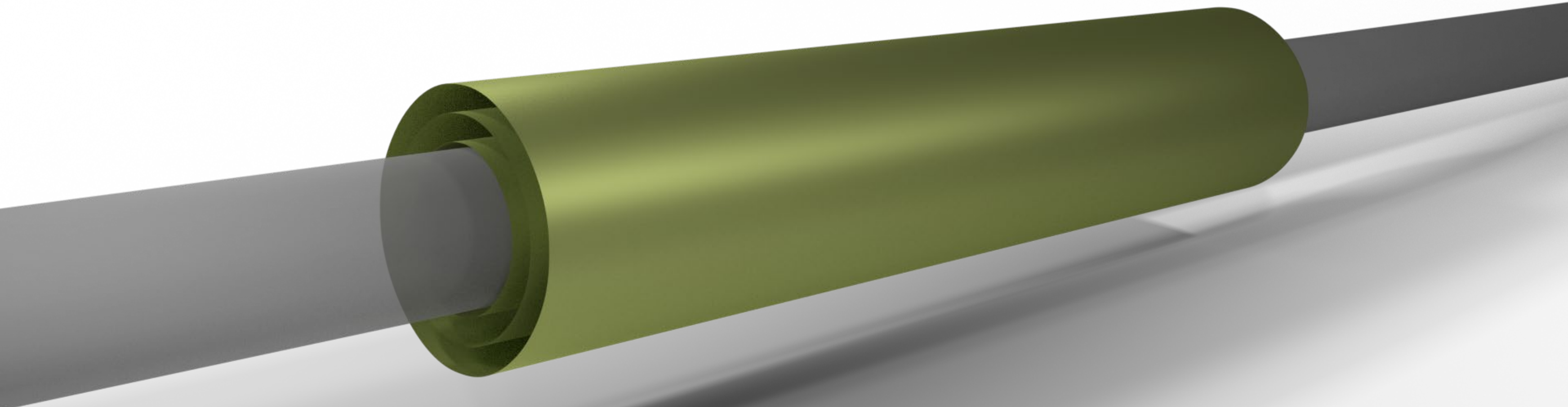
on behalf of the ALICE ITS3 Project



Outline

- The ITS3 Project
- Detector motivations and layout
- Progress report on main R&D topics:
  - Sensor development (see Iain’s talk later)
  - Thinning, Bending, Interconnections
  - Bent chip tests
  - Mechanics

ITS3 Project formation

EoI (2018-2019)


ALICE-PUBLIC-2018-013

Expression of Interest for an ALICE ITS Upgrade in LS3

ALICE Collaboration, CERN, Geneva, Switzerland

Abstract

Geneva, Switzerland
January 6, 2019

[ALICE-PUBLIC-2018-013]
https://cds.cern.ch/record/2644611

LoI (Sep 2019)


Letter of Intent for an ALICE ITS Upgrade in LS3

ALICE Collaboration, CERN, Geneva, Switzerland

Abstract

Geneva, Switzerland
September 8, 2019

[CERN-LHCC-2019-018 ; LHCC-I-034]
https://cds.cern.ch/record/2703140/

LHCC 139 (Sep 2019)

CERN/LHCC-2019-010
LHCC-139
September 2019

LARGE HADRON COLLIDER COMMITTEE

Minutes of the one-hundredth-and-thirty-ninth meeting held on
Wednesday and Thursday, 11-12 September 2019

The **LHCC is impressed** by the new concept for the ITS3 with significantly reduced material budget, recognises the physics case presented in the LoI and in the dedicated ITS3 session and appreciates the on-going simulations on various physics channels to further demonstrate the expected gain from better resolution and efficiency at low transverse momentum. The **LHCC endorses** the plan of ALICE to carry out the necessary R&D studies to demonstrate the technical feasibility of this upgrade project. A TDR to be submitted on a timescale compatible with installation in LS3 will have to include in addition a comprehensive study of its physics gains with respect to the ITS2 detector.

[CERN-LHCC-2019-010 ; LHCC-139]
https://cds.cern.ch/record/2689443

LHCC 142 (Jun 2020)

CERN/LHCC-2020-008
LHCC-142
June 2020

LARGE HADRON COLLIDER COMMITTEE

Minutes of the one-hundred-and-forty-second meeting held on
Thursday and Friday, 4-5 June 2020

ITS3 has now become a subproject of ITS, with activities ramping up. Pioneering the 65 nm technology for MAPS raised interest of many groups. Physics studies are moving towards full Monte-Carlo simulations, including the full detector geometry, and new physics channels have been explored. First R&D studies on mechanical and electrical properties of bent MAPS sensors have been performed and a full validation of MAPS curved to R = 18 mm is underway.

The **LHCC congratulates** the ITS3 groups for the successful start of the project.

[CERN-LHCC-2020-008 ; LHCC-142]
https://cds.cern.ch/record/2719880

R&D kick-off (Dec 2019)

[https://indico.cern.ch/e/its3-kickoff]

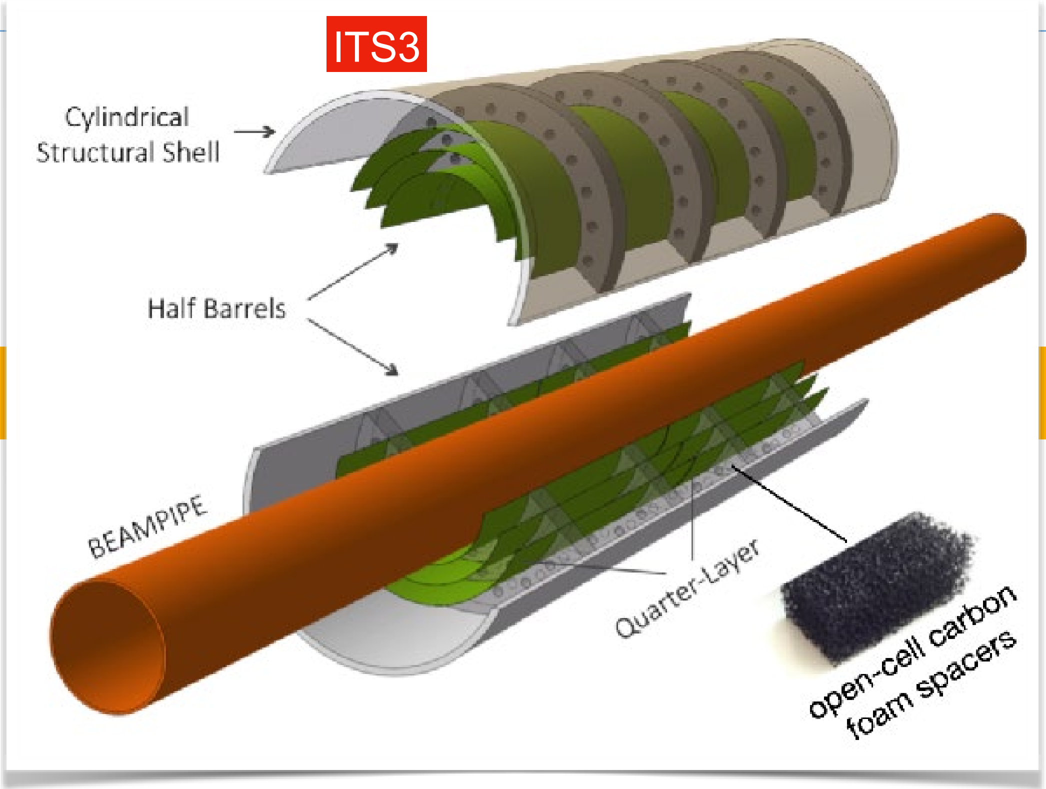
Project set-up (spring 2020)

- Project leaders
- Work packages conveners
- Discussion with institutes to participate (ongoing)

ITS3 detector layout

replace

by



in LS3

key improvements:
- closer to beam pipe: 23→18 mm
- less material: 0.3 → ~0.03 $\%X_0$

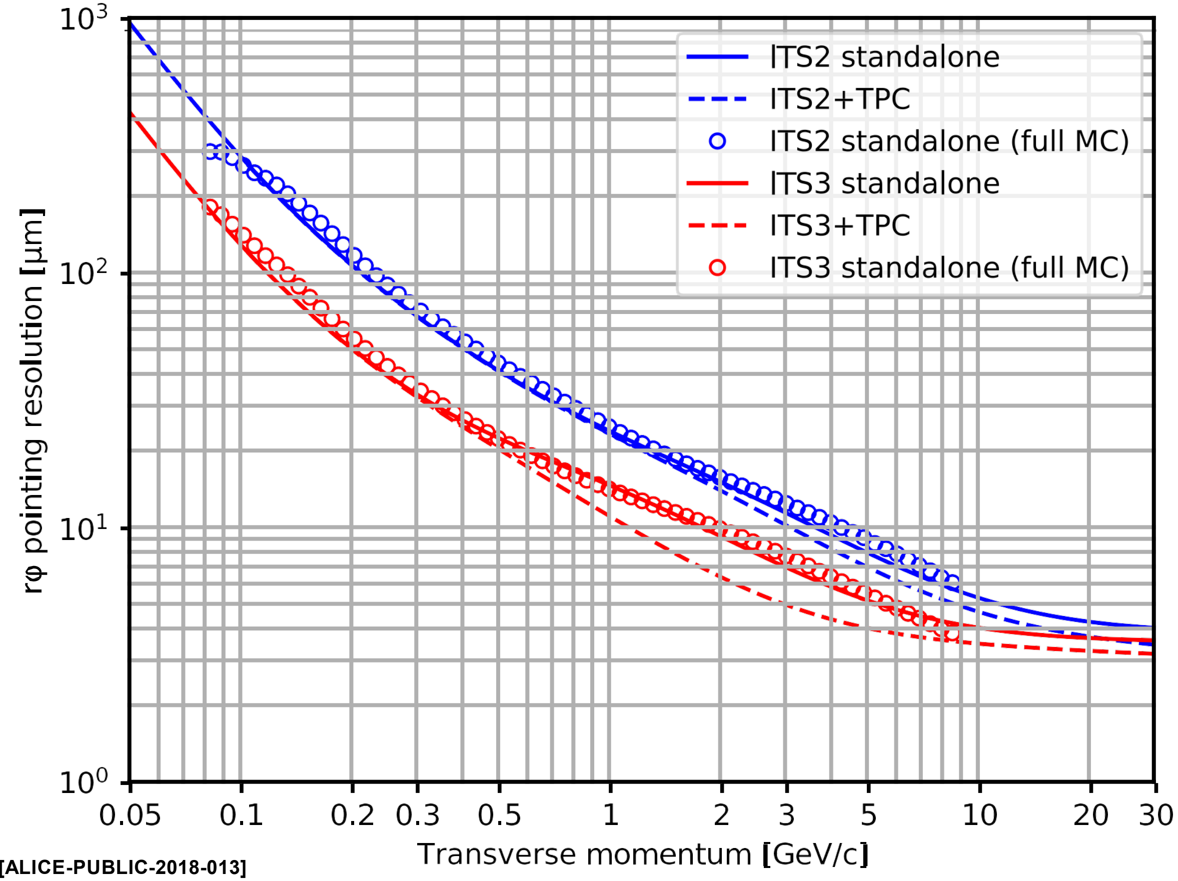
main benefit:
- better tracking performance
- especially at low p_T

based on:
- wafer-scale (up to ~28x10 cm),
- ultra-thin (20-40 μm),
- bent (R=18, 24, 30 mm)

Si sensors (MAPS)

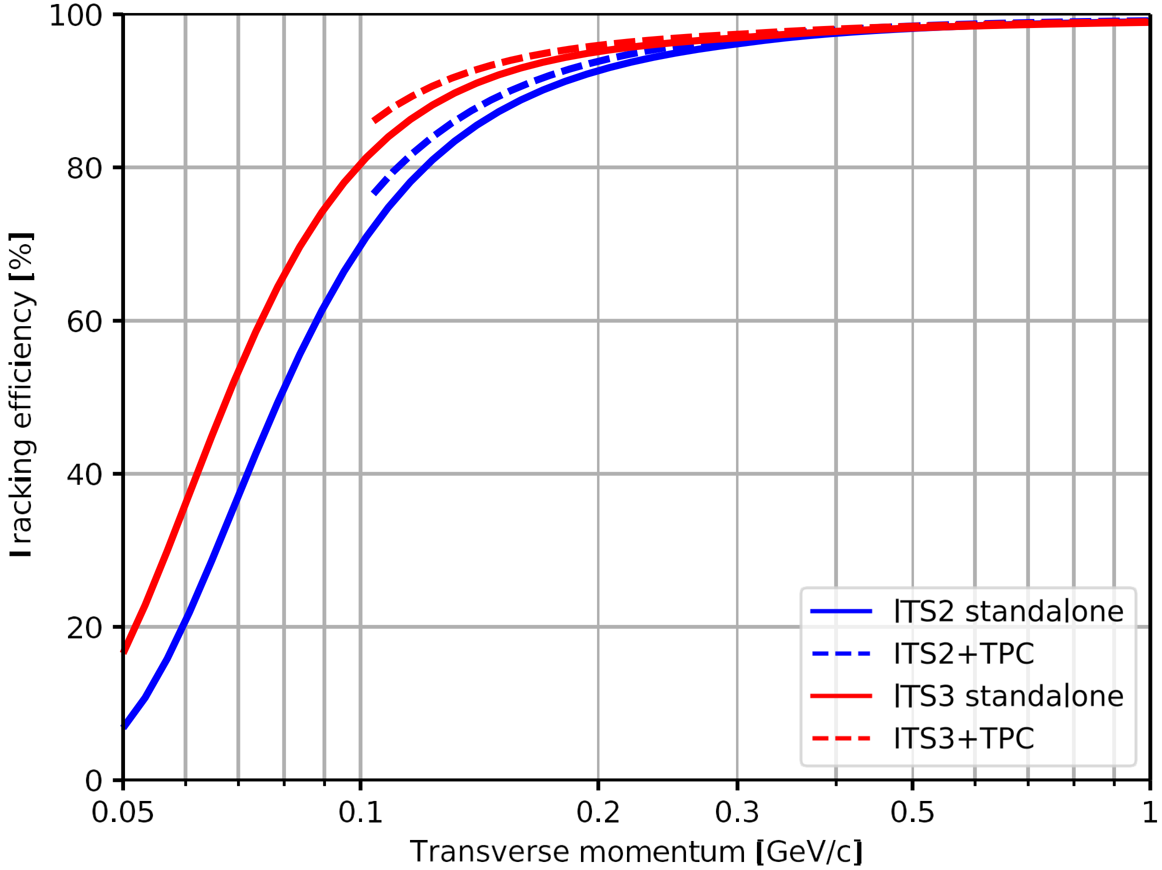
ITS3 projected performance

pointing resolution



[ALICE-PUBLIC-2018-013]

tracking efficiency



improvement of factor 2 over all momenta

large improvement for low transverse momenta

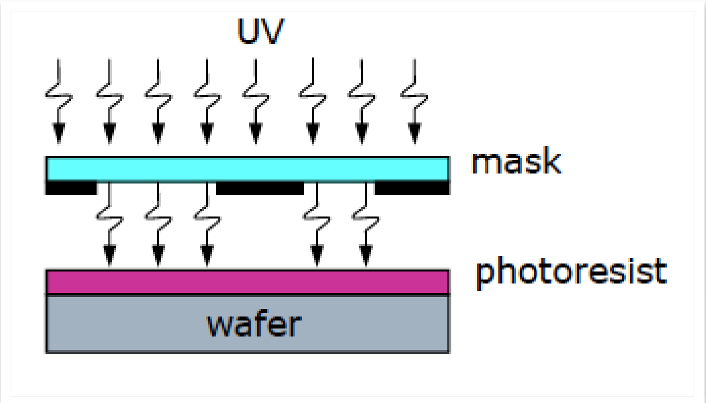
Wafer-scale chip in 65 nm CMOS process

- Switch to TowerJazz 65 nm CMOS process (ITS2/ALPIDE: TowerJazz 180 nm)
  - needed mainly because of larger wafers: ⌀=300 mm (180 nm process only available on ⌀=200 mm wafers)

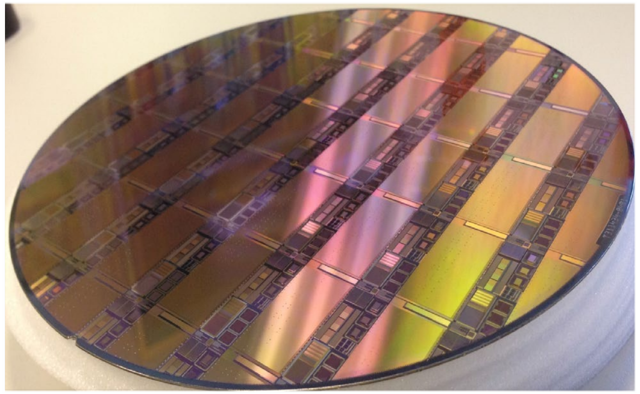
- Stitching, i.e. producing chips as big as the wafer

- More details about the sensor development in the ***next talk by Iain Sedgwick***

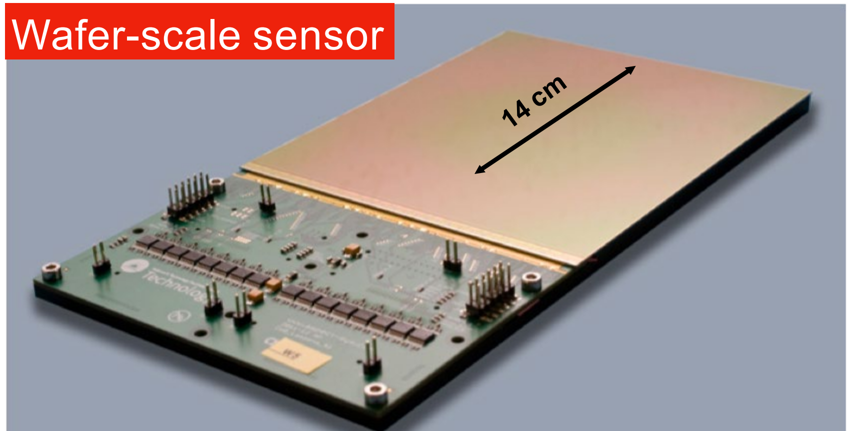
Principle of photolithography



200 mm ALPIDE prototype wafer

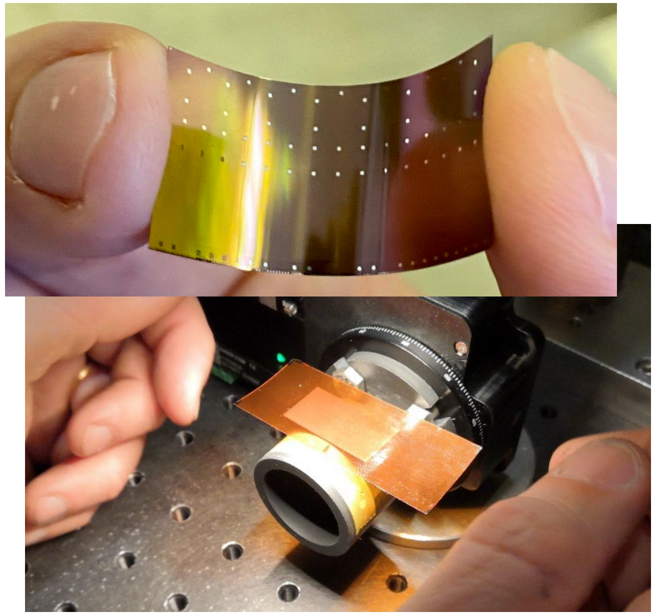


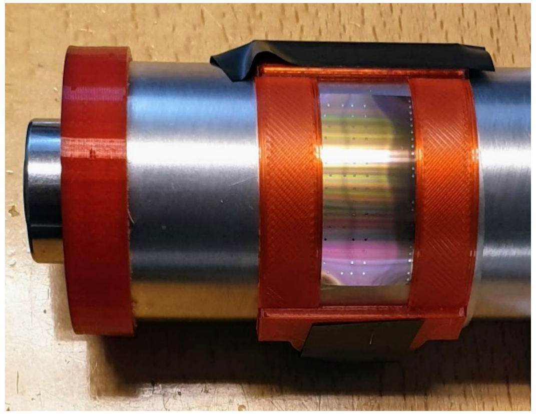
Wafer-scale sensor



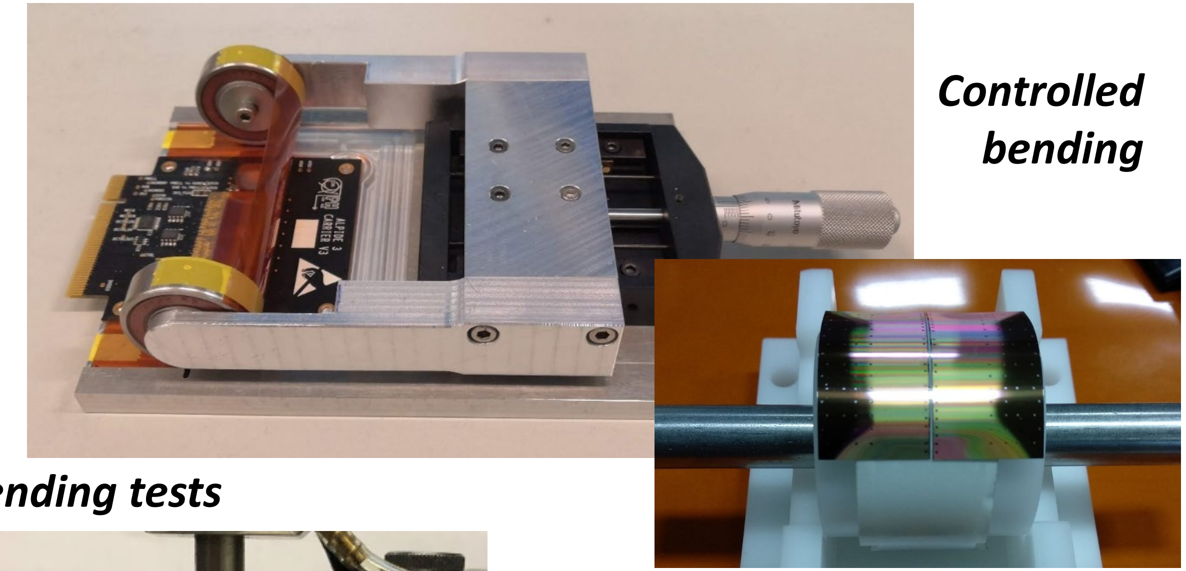
Courtesy: R. Turchetta, Rutherford Appleton Laboratory

R&D on bending and thinning



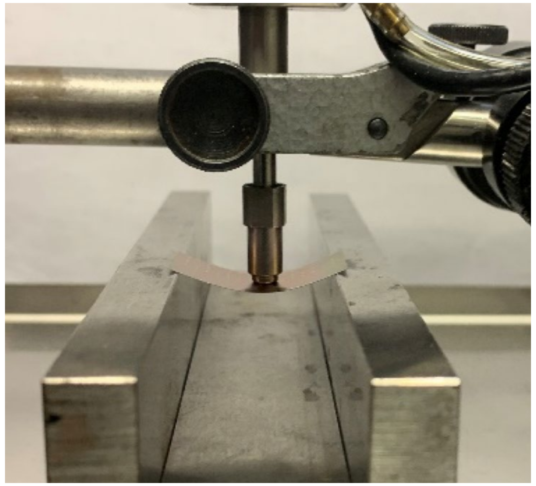


Manual bending

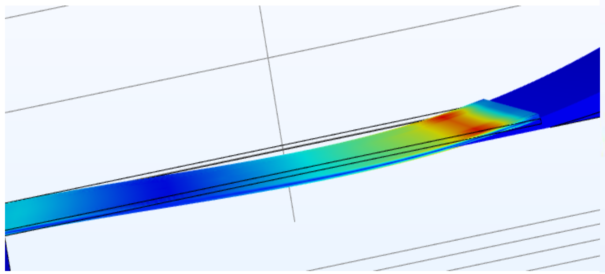


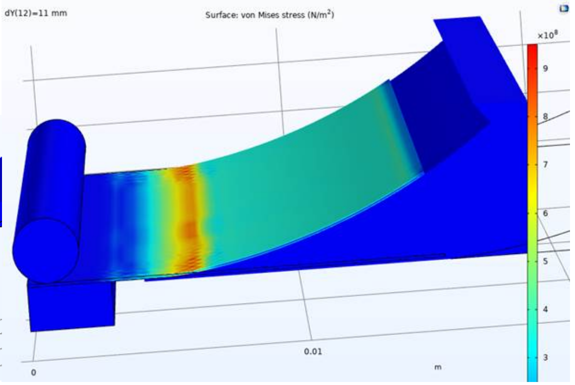
Controlled bending

Bending tests

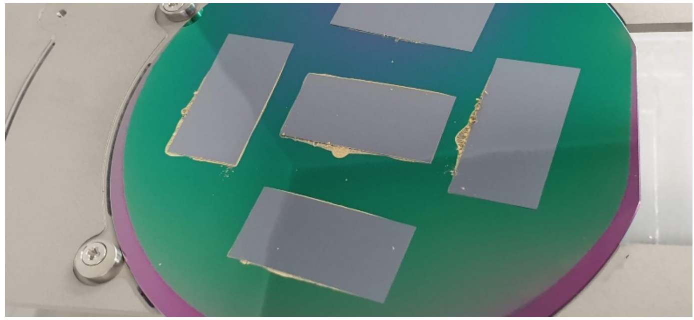


Strain simulations





DRIE thinning tests

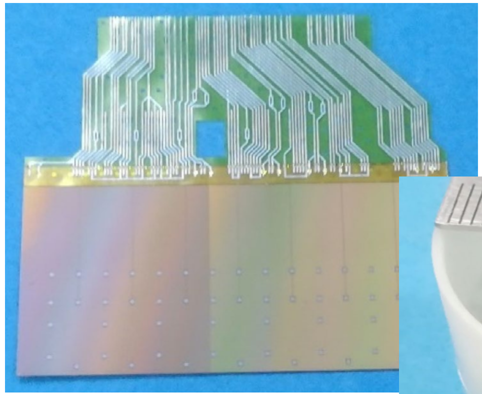


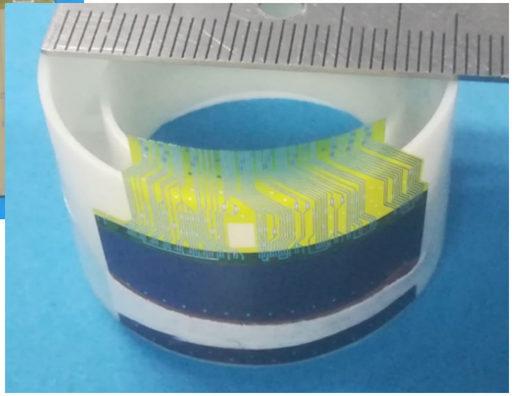
Tools and procedures for interconnections

- Several support tools and flexible circuits

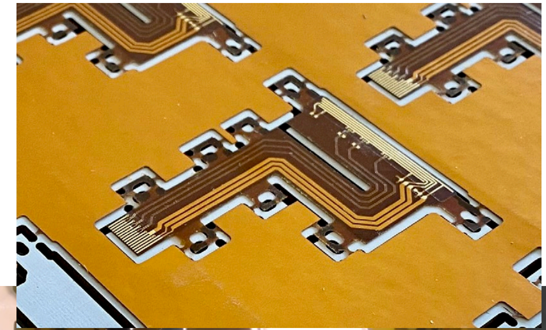
SpTAB bonding

Bending after bonding

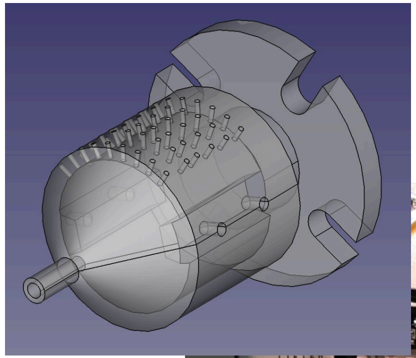


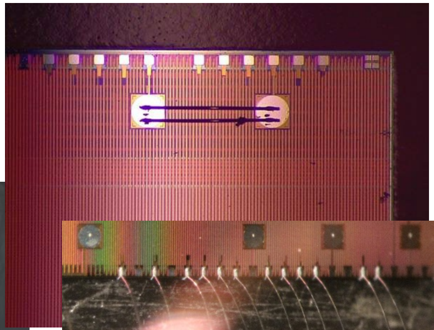


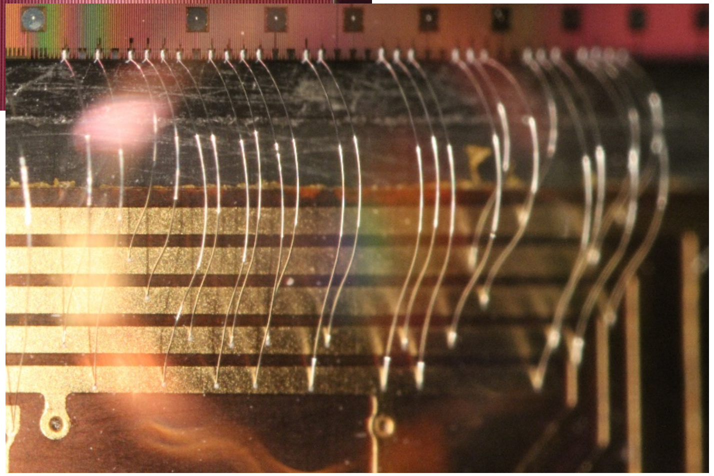
Bendable FPC



Cylindrical bonding tool

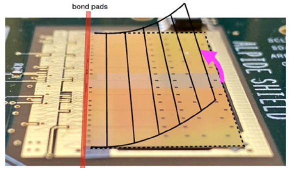






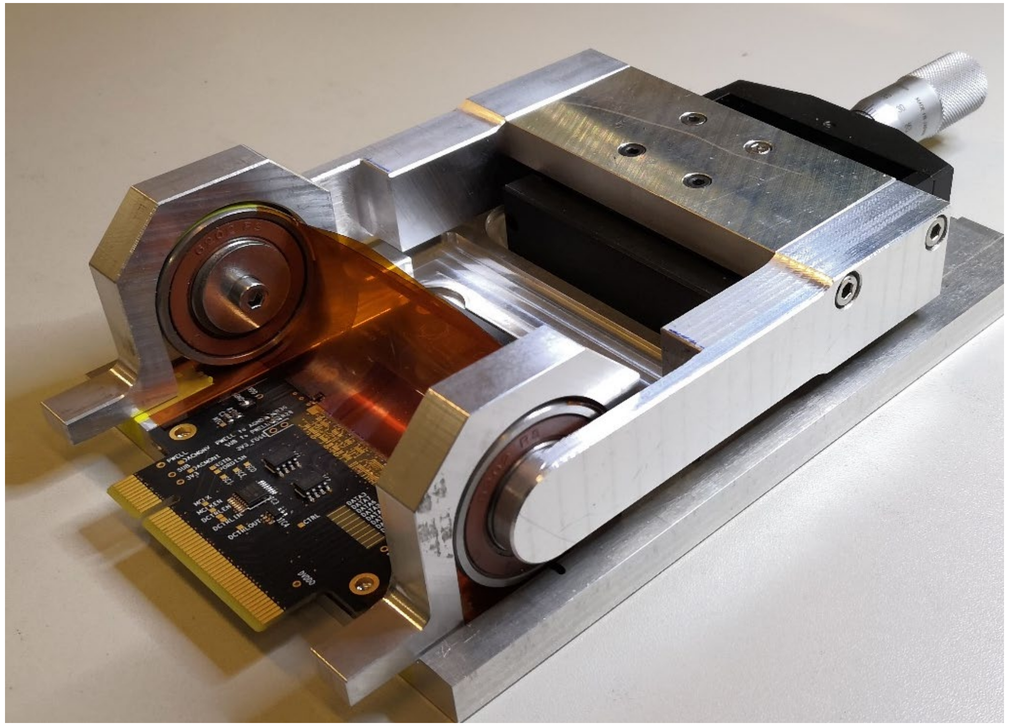
Wire bonding on curved surface

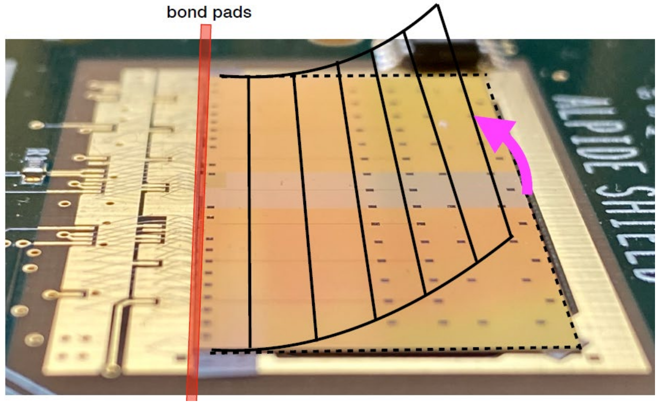
Bending after bending

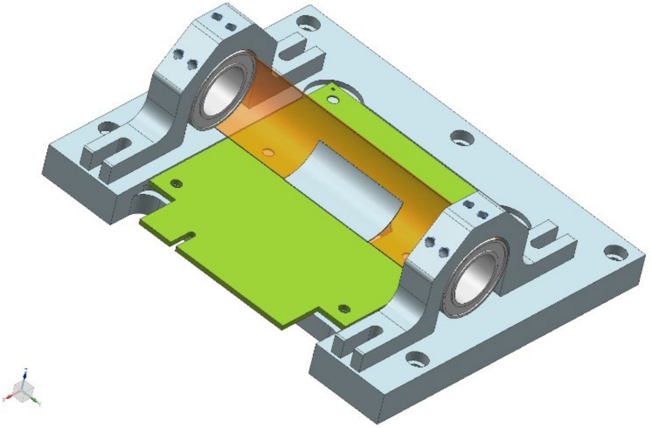


Bent 50 µm ALPIDE testing - 1

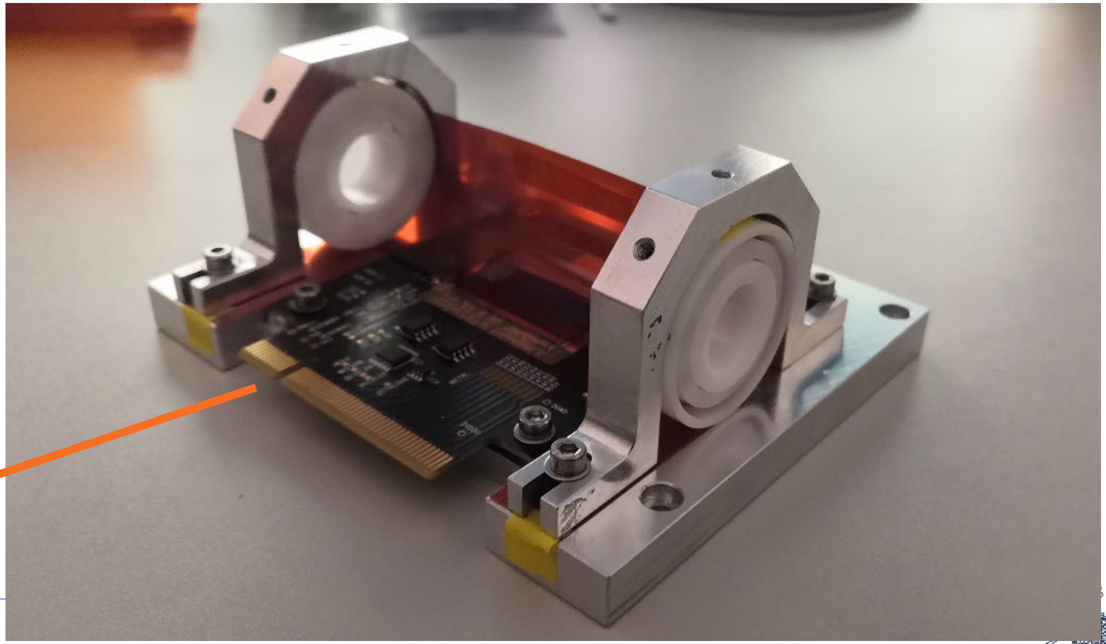
- **Bent along the short side**
  - Bending affects pixel matrix only
  - Bonding area is glued: flat and secured
  - Variable curvature (down to 1 cm radius)



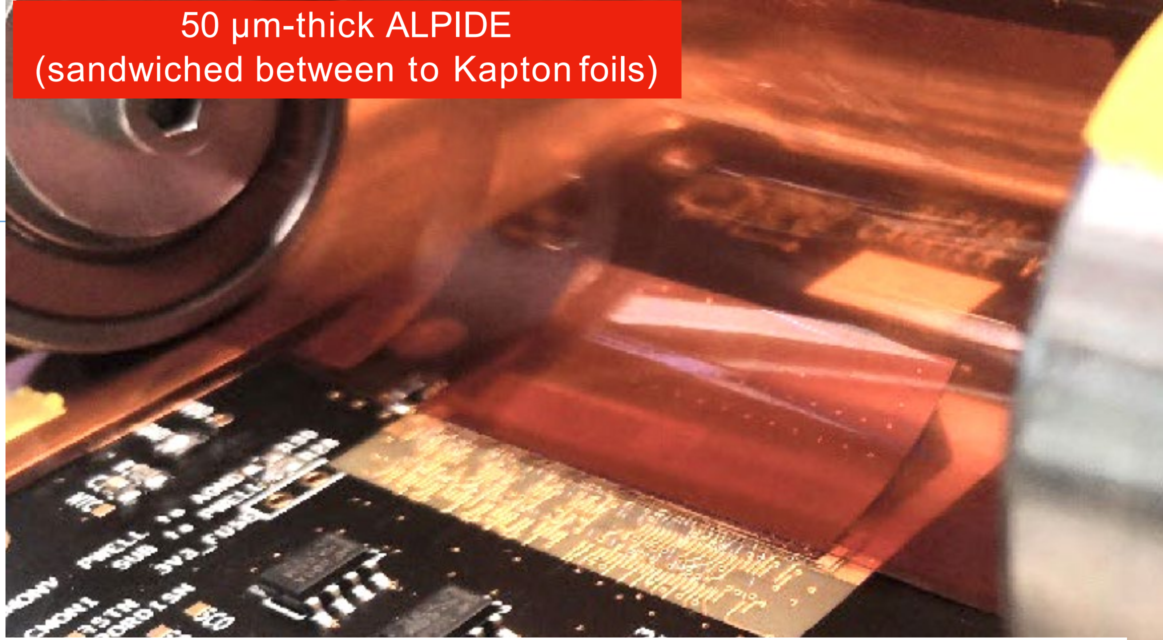




Single chip DAQ board



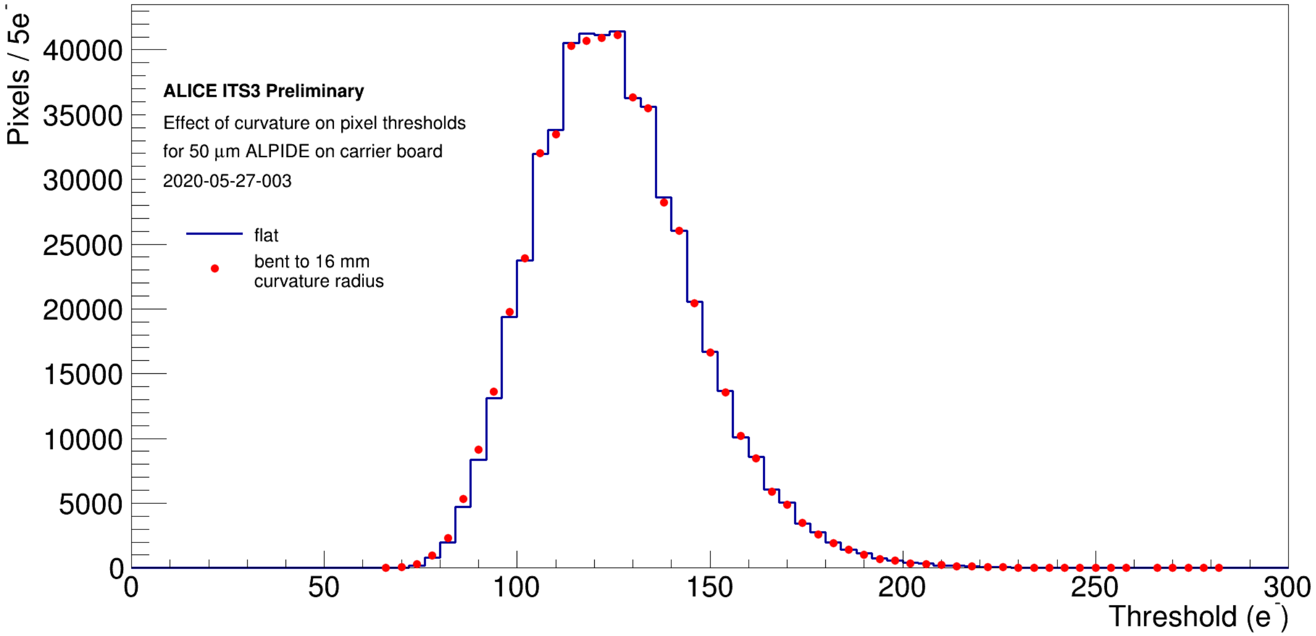
Bent chip electrical tests



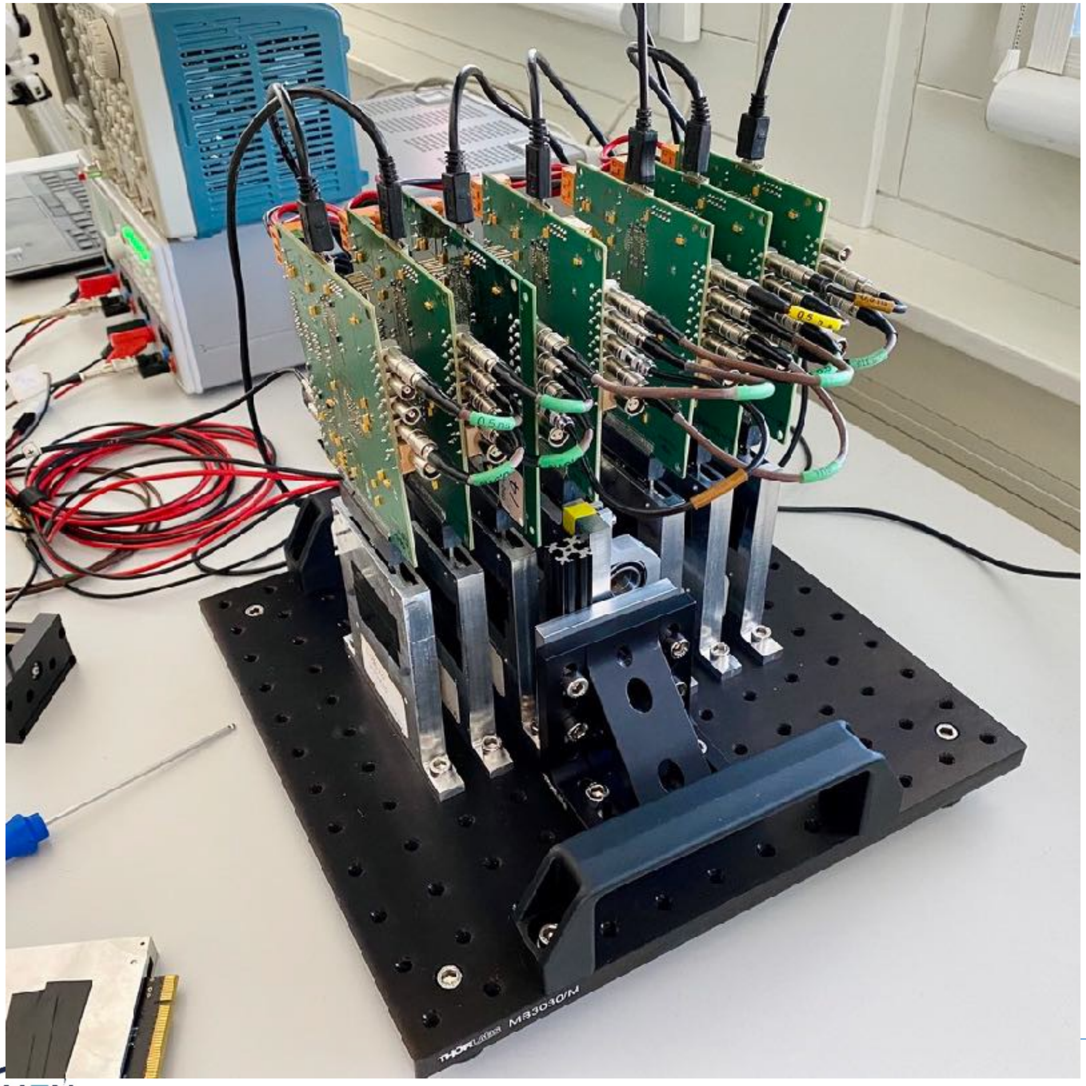
- Laboratory tests to characterize bent ALPIDEs in terms of thresholds and fake-hit rate
  - different set-ups are tried
  - experience on handling is gained

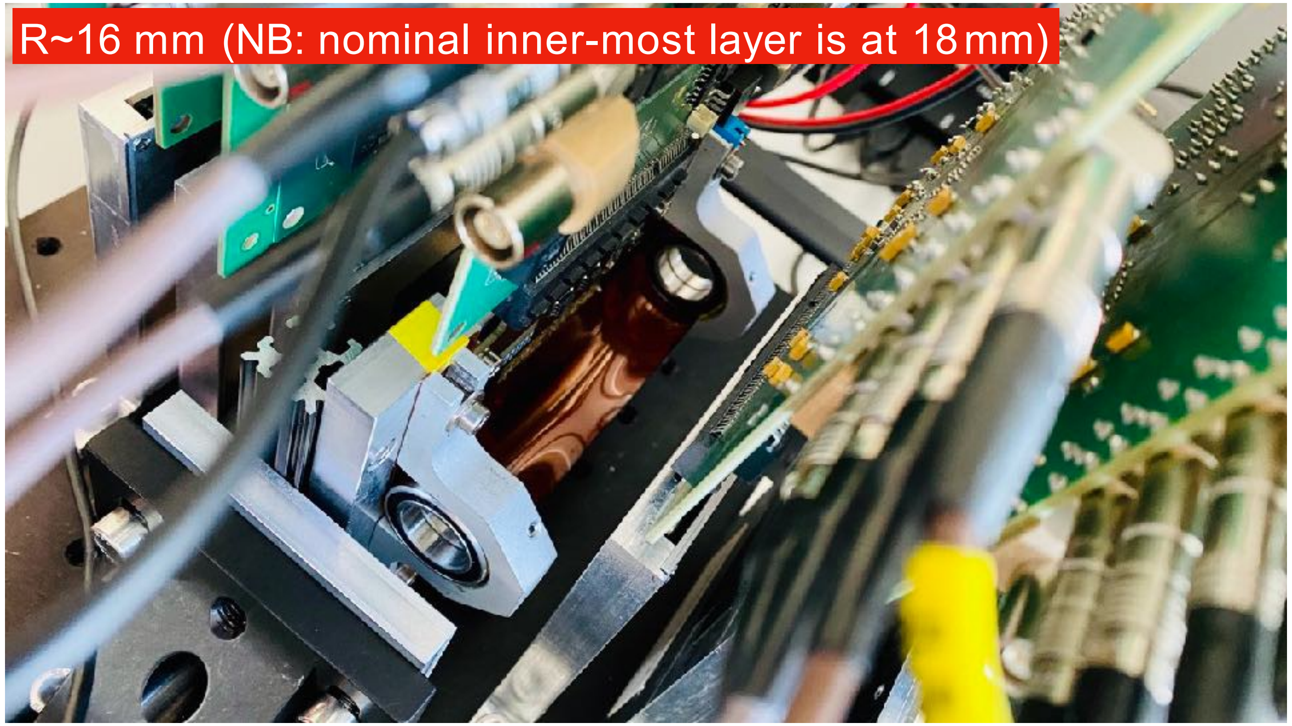
- The curvature effect is not noticeable on:
  - pixel thresholds, FHR, pixel responsiveness
  - tested down to below nominal bending radius

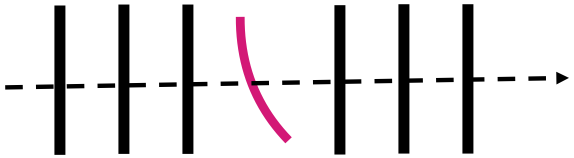
- 3 chips successfully installed and tested in lab, 2 of them sent to DESY for testbeam



Bent chip in ALPIDE-based beam telescope







+ 2nd chip at R~18 mm

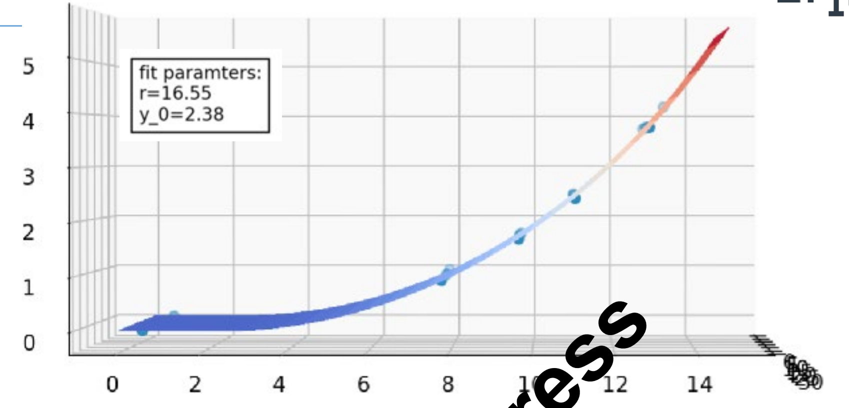
Testbeam data analysis ongoing

- Bent chip shape approximated as a purely cylindrical segment
- First look at the efficiency shows >99.9% at nominal 100 e^- threshold

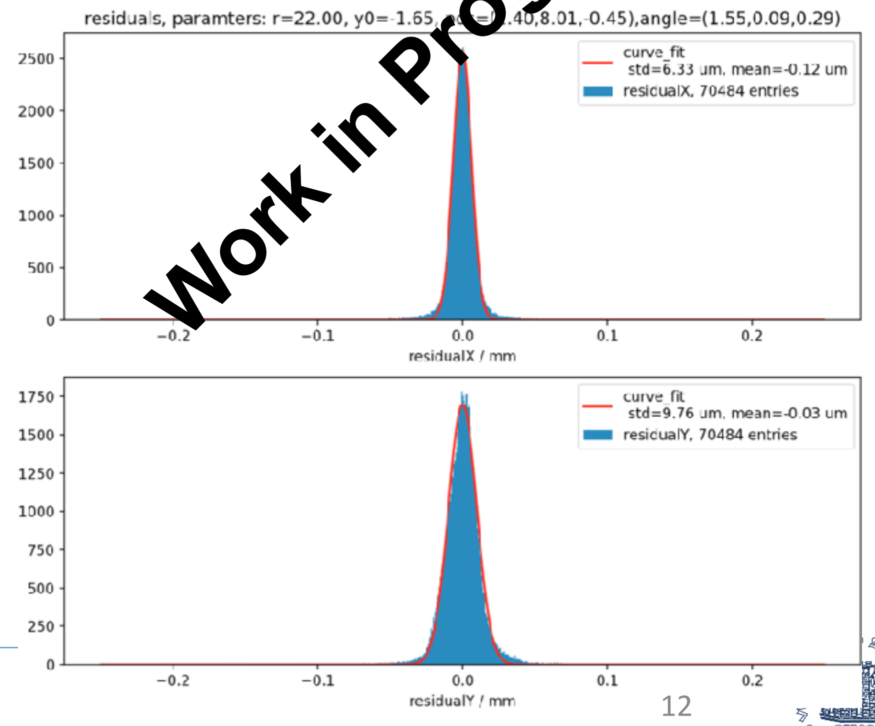
- Main challenges:
  - Describe the surface with µm-precision
  - Hold the chip at the desired curvature:
    - measurements before and after the test show a curvature relaxation from 16 to 24 mm
    - least squares optimization of the cylindrical model yielded the DUT radius of 22 mm

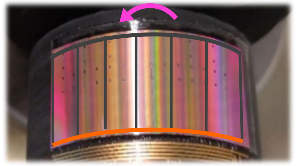
- First paper in preparation

Coordinate measurement machine



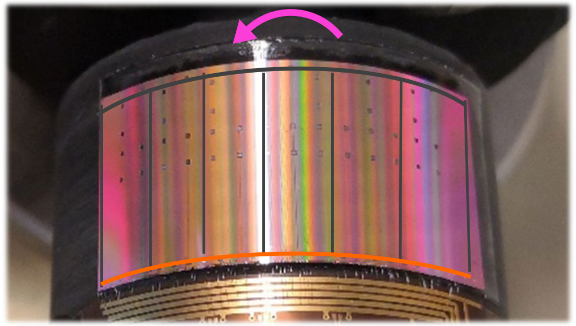
Test beam data





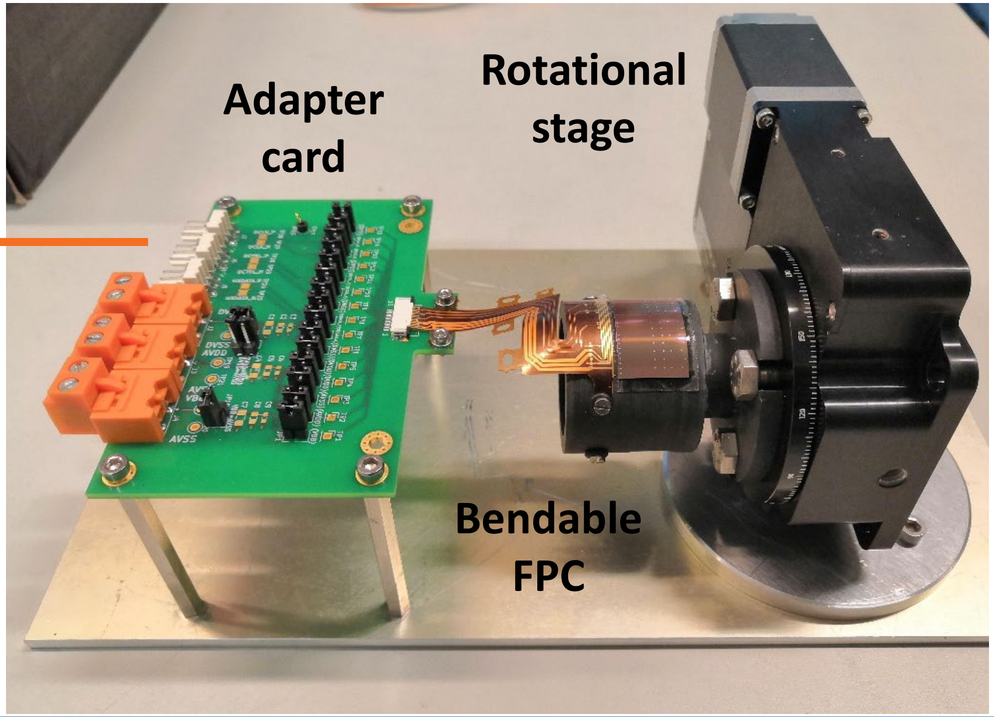
Bent 50 µm ALPIDE testing - 2

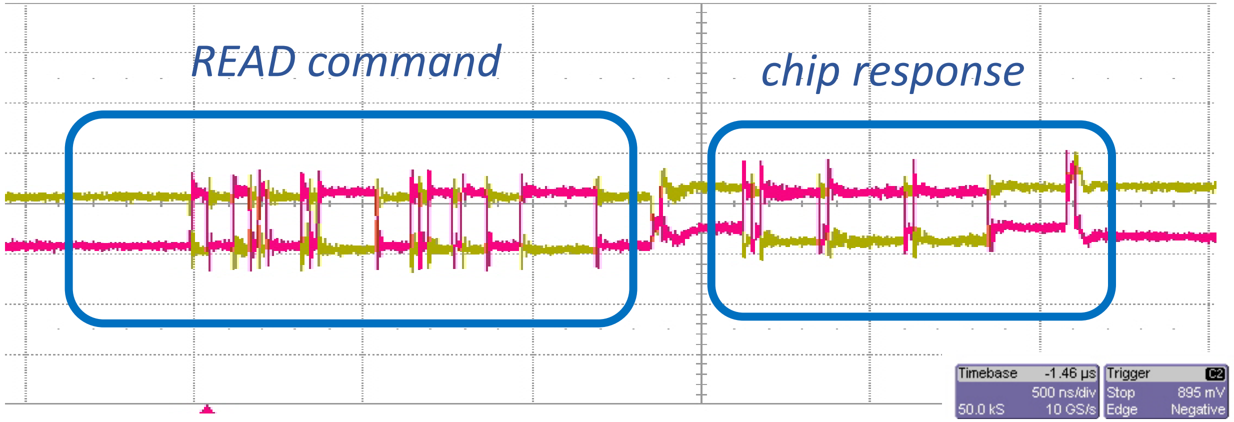
- **Bent along the long side**
  - Affecting matrix and periphery
  - Stretches the CMOS circuitry
  - Completely glued onto support
  - Fixed curvature (1.8 cm radius)



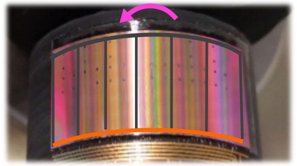
- Custom developed setup to interconnect the curved chip after bending
- I-V and response immediately checked after interconnecting the chip: works

DAQ board / Power Supply

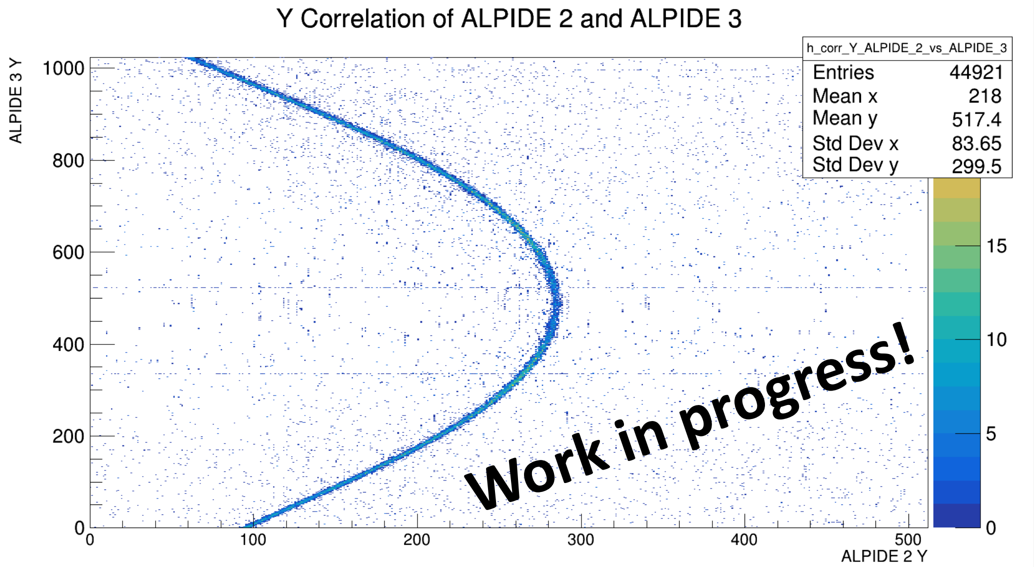




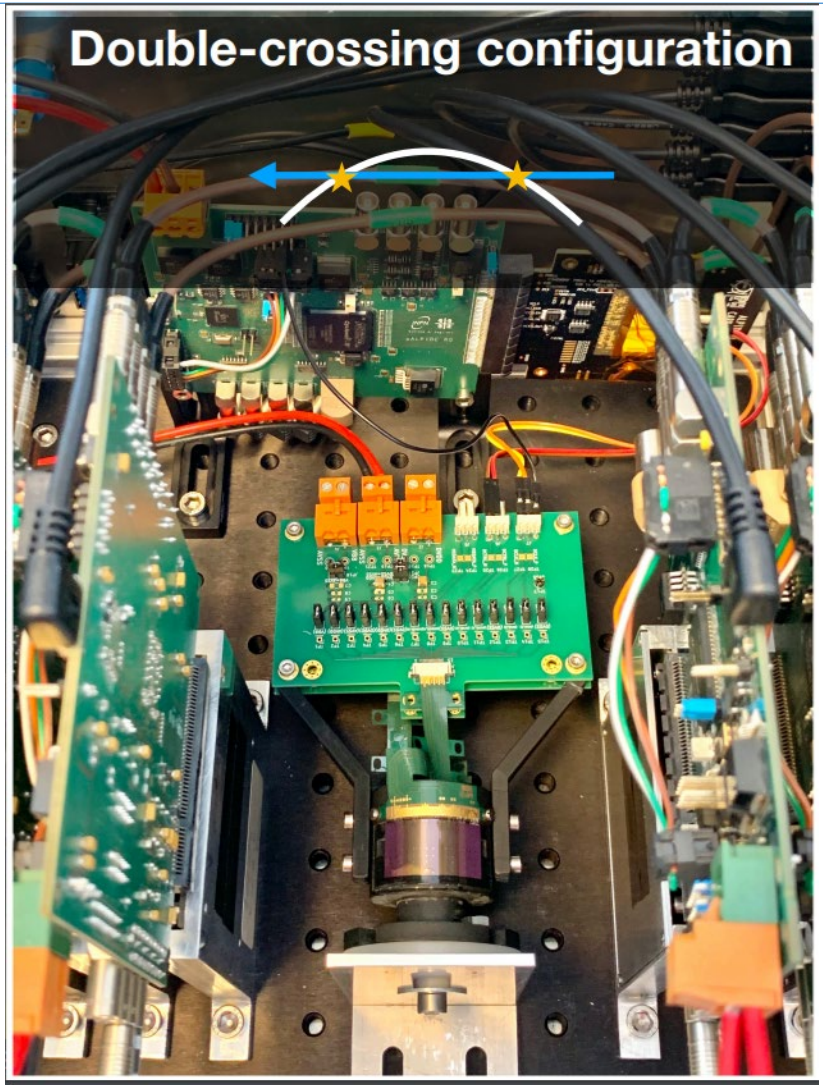
- 5 chips successfully bent and tested.
- Handling tools to be improved to avoid accidents



Testbeam happened last week



Online monitoring
Correlation bent chip – reference plane

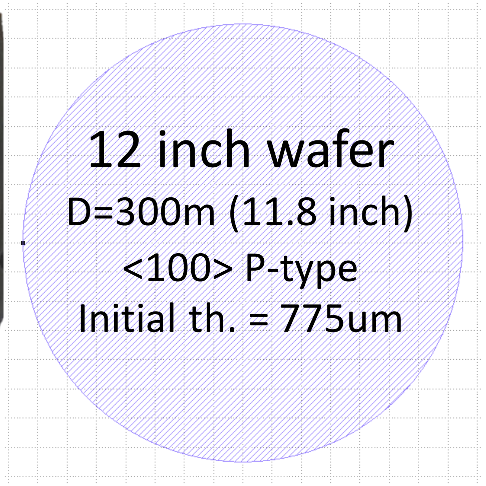


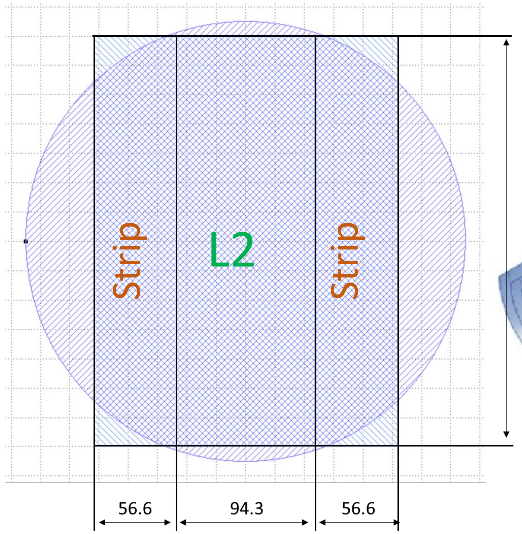
Analysis is ongoing…
but the bent chip works!

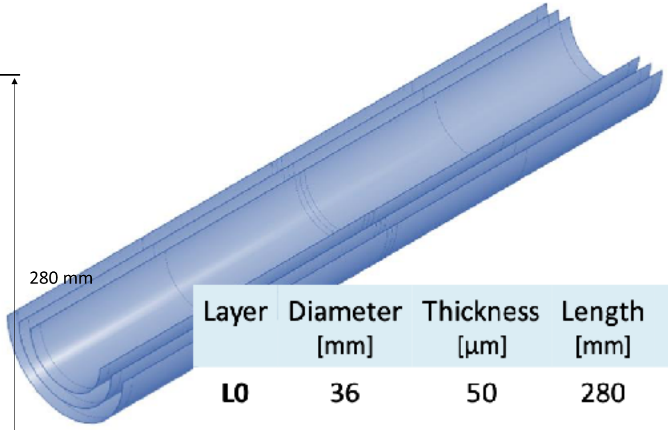
Towards the engineering module

Dummy chips: blank, 300 mm wafers were procured and thinned down to 50 µm, under test

- they will serve first integration steps
- Next: adding a metallization layer with a heater for thermal tests





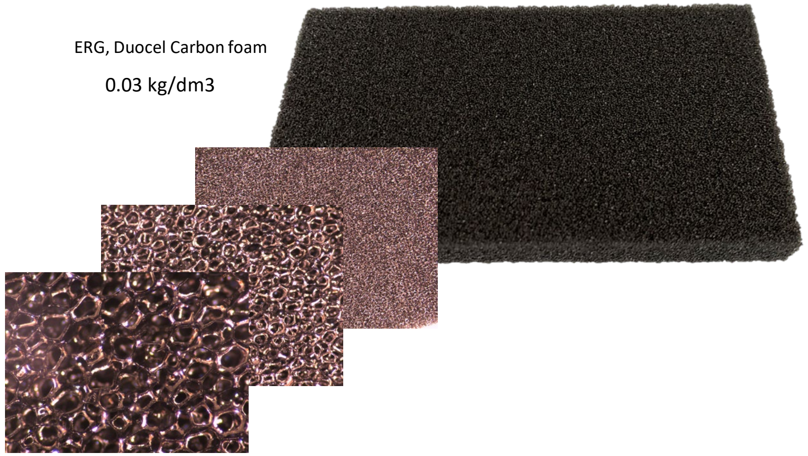


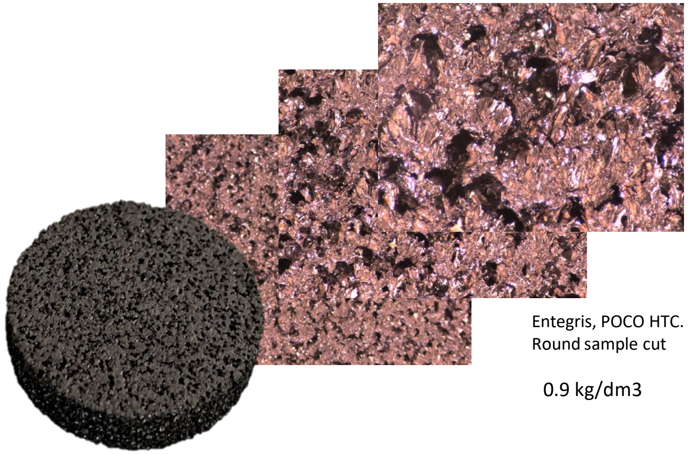
Layer	Diameter [mm]	Thickness [µm]	Length [mm]	Semi-circ. [mm]
L0	36	50	280	~56.55
L1	48	50	280	~75.4
L2	60	50	280	~94.25

Carbon foam spacer development

ERG, Duocel Carbon foam

0.03 kg/dm3





Entegris, POCO HTC.
Round sample cut

0.9 kg/dm3

Company	Foam Name	Material Ordered	T. value (CHF)	
ERG	Duocel®	3 sets of rings + 1 sample	2087	10.06.2020
ALLCOMP	K9 Hi-K	1 set of rings + 1 sample for 2 different density (0.20-0.26 and 0.45-0.68)	5360	26.06.2020
CFOAM	35HTC	3 sets of rings + 1 sample	1500	17.06.2020
ENTEGRIS	POCO HTC	3 sets of rings + 1 sample	2735	TBD

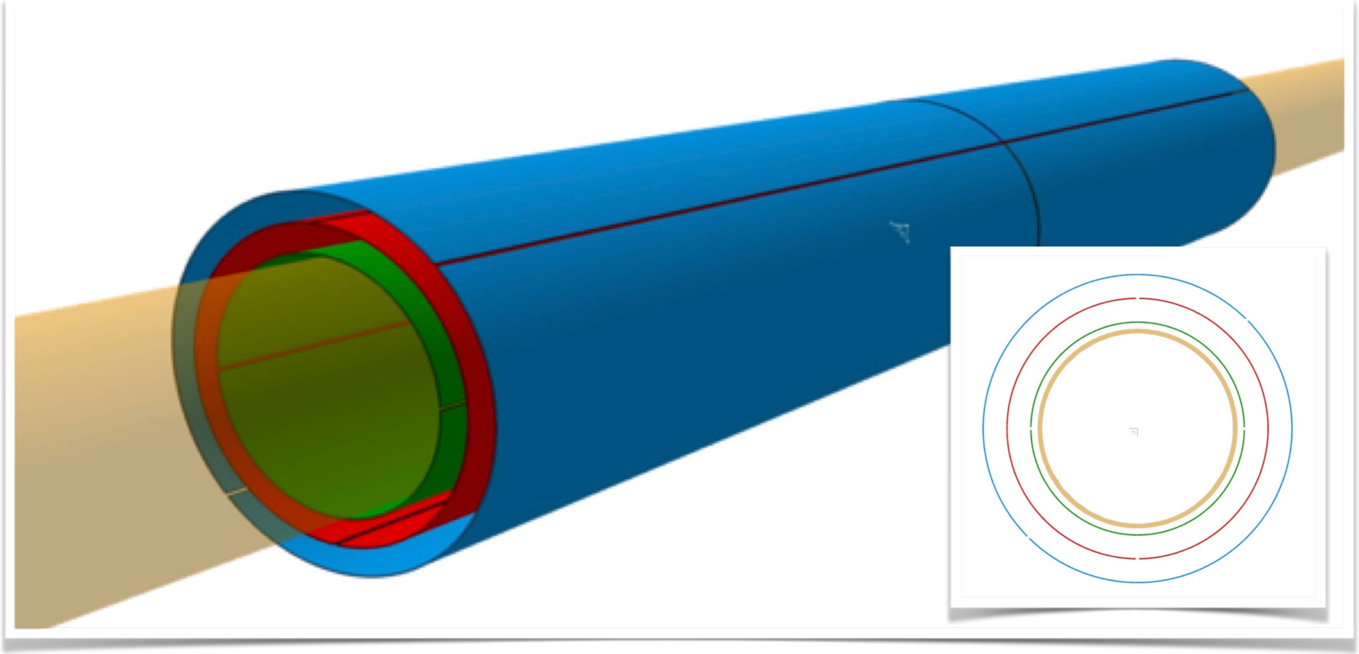
- First spacers were machined

Conclusions

- The ITS3 Project has been endorsed by LHCC and has a fully operational organization
- R&D activities on the most challenging R&D topics are progressing well, and are generating interest beyond the ALICE community
- A new sensor based on 65 nm CMOS process is being developed (*see next talk)*
- Existing 50 μm thick ALPIDEs have been bent and tested, demonstrating that an ITS3 based on bent silicon is possible

Thank you for your attention!

Layout



Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

- New beam pipe:
  - "old" radius/thickness: 18.2/0.8 mm
  - new radius/thickness: 16.0/0.5 mm
- Extremely low material budget:
  - Beam pipe thickness: 500 µm (0.14% X0)
  - Sensor thickness: 20-40 µm (0.02-0.04% X0)
- Material homogeneously distributed:
  - essentially zero systematic error from material distribution