UNIVERSITY OF BIRMINGHAM

Overview of silicon sensor technology

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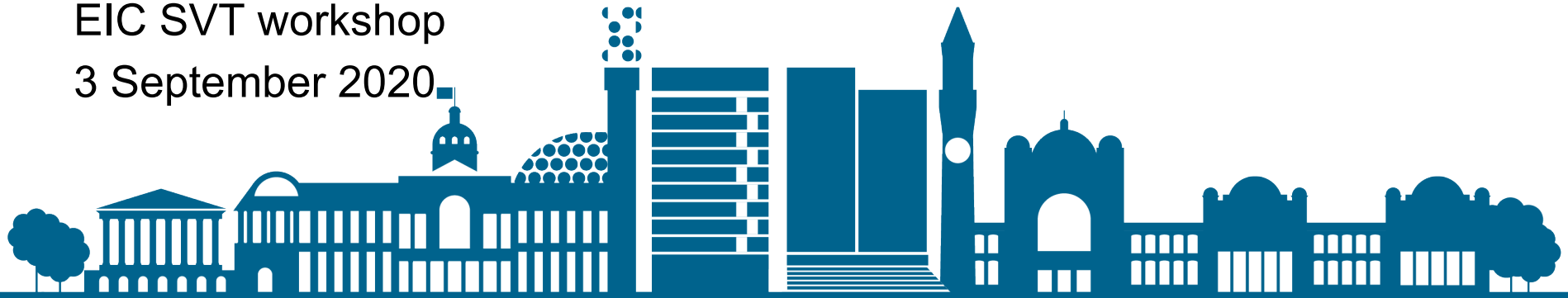
EIC SVT workshop

3 September 2020



Overview

- Introduction to EIC vertex and tracking detector
- Technology selection
- MAPS in 65 nm technology / ITS3-derived EIC sensor
- EIC Silicon Consortium
- Conclusion

Introduction

- All EIC detector concepts proposed so far are equipped with a vertex and tracking detector as their innermost element

- This detector is needed to enable high precision measurements that are key to the EIC science programme
  - Determine **primary vertices** with high precision
  - Allow the measurement of **secondary vertices** for heavy-flavor decays
  - **Low-p_T** tracking

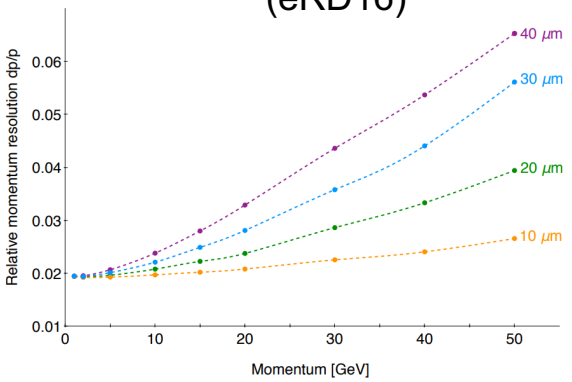
- This requires a **well integrated, large acceptance** vertex and tracking detector designed with **high granularity and low material budget**

Detector requirements

Detector requirements matrix

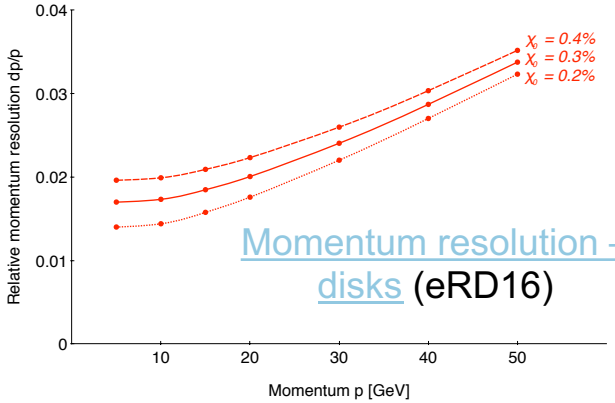
η	Nomenclature			Tracking			
				Resolution	Allowed X/X_0	Si-Vertex	pT Range
-6.9 to -5.8	↓ p/A	Auxiliary Detectors	low-Q2 tagger	σθ/θ < 1.5%; 10-6 < Q2 < 10-2 GeV2			
...							
-4.5 to -4.0			Instrumentation to separate charged particles from photons				
-4.0 to -3.5							
-3.5 to -3.0		Central Detector	Backward Detector	σ_p/p ~ 0.1%⊕0.5%	~5% or less X	TBD	
-3.0 to -2.5							
-2.5 to -2.0				σ_p/p 0.1%⊕0.5%			
-2.0 to -1.5				σ_p/p 0.05%⊕0.5%			
-1.5 to -1.0							
-1.0 to -0.5			Barrel	σ_p/p ~0.05%×p+0.5%		σ_{xyz} ~ 20 μm, $d_0(z)$ ~$d_0(r\Phi)$ ~ 20/p_TGeV μm + 5 μm	
-0.5 to 0.0							
0.0 to 0.5							
0.5 to 1.0							
1.0 to 1.5			Forward Detectors	σ_p/p ~0.05%×p+1.0%		TBD	
1.5 to 2.0							
2.0 to 2.5							
2.5 to 3.0				σ_p/p ~ 0.1%×p+2.0%			
3.0 to 3.5							

Momentum resolution – disks (eRD16)

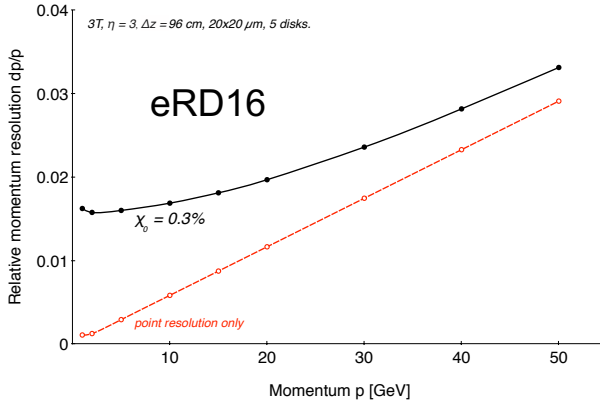


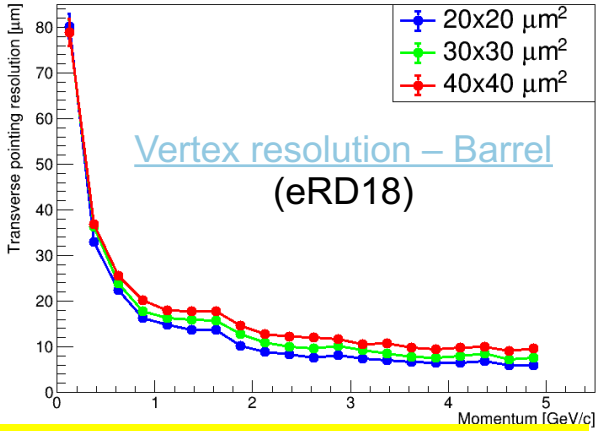
Equidistant disks, 0.25 < z < 1.21m, 3T field (open), eta =3

Point resolution is simply pixel-size/√12 here, no system effects



Momentum resolution – disks (eRD16)





Vertex resolution – Barrel (eRD18)

See also Håkan and Rey's talks

Vertex and tracking detector: pre-CDo baseline

- The majority of the proposed detector concepts assumed as baseline an **ITS2-derived** vertex and tracking detector

- For instance, the BeAST layout has a barrel region composed of two **inner vertexing layers** and two **outer tracking layers** with **0.3% X/X_0**, similar to the ITS2 detector configuration

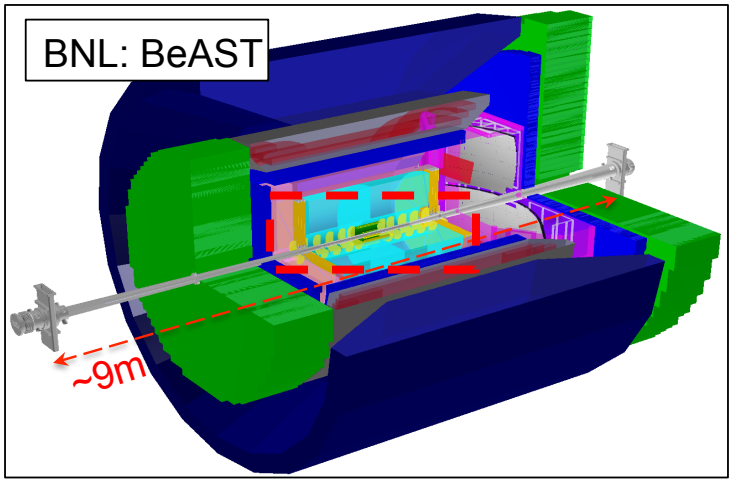
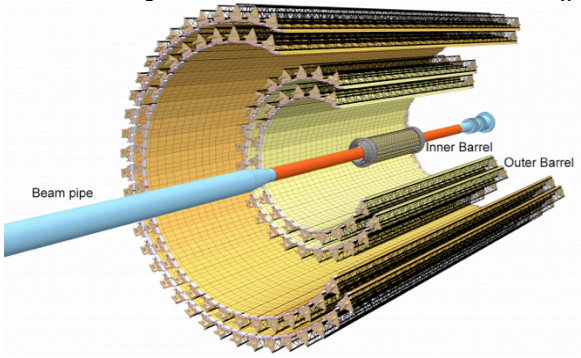


Image courtesy of Alexander Kiselev (BNL)

ALICE Inner Tracking System Upgrade at LHC (ITS2)

Inner layer thickness = **0.3%** X/X_0

Outer layer thickness = **0.8%** X/X_0



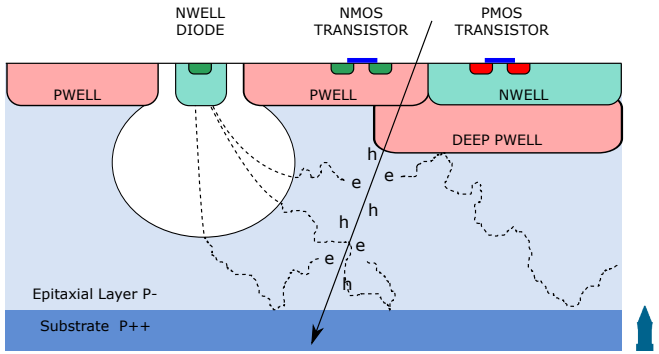
J. Phys. G: Nucl. Part. Phys. 41 (2014) 087002

Vertex and tracking detector: pre-CDo baseline

- Differently from ITS2, an EIC vertex and tracking detector also requires **disks in the forward/backward region** to provide full acceptance coverage
  - For example, BeAST has seven disks in each of these two regions

- Also, with respect to the ALPIDE sensor used in ITS2 a smaller pixel pitch and shorter integration time are needed
  - **20 µm pixel pitch** is assumed as baseline
  - Interaction frequency = 50 – 500 kHz → integration time down to **2 µs**

ALPIDE sensor
180 nm Tower Jazz
28 x 28 µm^2 pixel pitch
~ 5 µs integration time
Power density **40 mW cm^{-2}**
50 kHz interaction rate (Pb-Pb)
200 kHz interaction rate (pp)



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Sensor technology choice

- A survey of silicon technologies has been presented at the Temple EIC Yellow Report workshop

- The sensor technology identified to satisfy the requirements of an EIC vertex and tracking detector is **Monolithic Active Pixel Sensors**
  - MAPS contain sensor and electronics in the same silicon substrate

- State-of-the-art MAPS detectors
  - MIMOSA sensor at STAR HFT
  - ALPIDE sensor at ALICE ITS

- More recent development
  - **Depleted MAPS** (i.e. HV/HR-CMOS)
  - **65 nm MAPS**

Is there any existing or planned sensor that satisfies the EIC requirements?

Disclaimer

- Existing and planned MAPS sensors are shown for comparison purposes
  - **This list is not exhaustive** but represents the most applicable known designs based on work carried out by the authors
  - It is also not a review of development of MAPS sensors

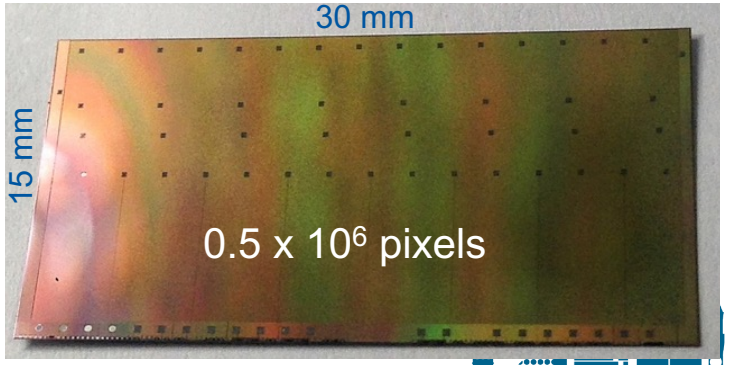
- All considered MAPS sensors are fabricated in **Tower Jazz (TJ) technology**
  - This technology (differently from other such as LFoundry or AMS/TSI) allows for the design of a **small collection electrode** resulting in a **small detector capacitance**
  - This translates into **low power (key for low material budget), compact FE design (key for small pixels)**, low noise

See also Leo's talk

ALPIDE

- ALPIDE can meet the requirements with some work
  - Smaller pixel size: 28 to 20 μm
  - Shorten integration time: 5 to 2 μs
  - Possibly smaller power consumption to improve on the material budget requirements
- However the performance is marginal compared to the EIC requirements
- It is suggested that ALPIDE serves as a possible **alternate backup sensor** if existing efforts at new sensor designs are not successful or are delayed past the needed construction timeframe

https://indico.cern.ch/event/632608/attachments/1445423/2239598/Detector_seminar_priedler_28042017_final.pdf

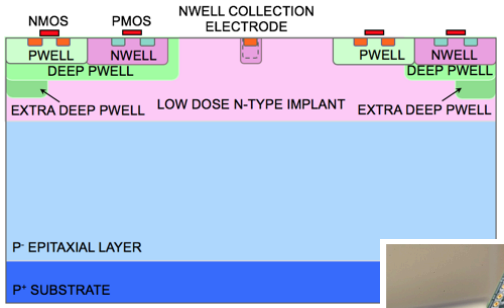


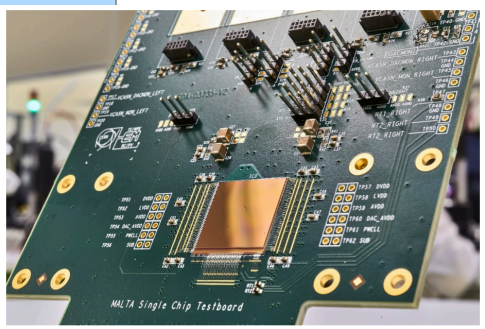
MALTA

H. Pernegger et al 2017 JINST 12 P06008
W. Snoeys et al NIMA 817 (2017)
M. Munker *et al* 2019 JINST 14 C05013

G. Aglieri Rinella, NIMA 845 (2017) 583 - 587
R. Cardella et al 2019 JINST 14 C06019
M. Dyndal et al 2020 JINST 15 P02005
I. Berdalvic, PhD thesis

- Depleted MAPS prototype developed for the ATLAS pixel outer layer at the HL-LHC
- Designed in TJ 180 nm process with modification for full depletion
  - Deep planar junction to achieve depletion under electronics p-well
- Successfully meets requirements for operation at the HL-LHC
  - **High time resolution and radiation hardness**
  - Pixel size and power consumption not compatible with EIC requirements





	ALPIDE	MALTA
Experiment	ALICE ITS (inner/outer layers)	ATLAS ITk pixel Phase II (outermost layer)
Technology	TJ 180 nm CIS	TJ 180 nm CIS modified
Substrate resistivity [kOhm cm]	> 1 (epi-layer 18-25 um)	
Collection electrode	small	
Detector capacitance [fF]	<5	
Chip size [cm x cm]	1.5 x 3	2 x 2
Pixel size [um x um]	28 x 28	36.4 x 36.4
Peaking time [ns]	2×10^3	20 – 50
Time resolution [ns]	N/A	< 5
Particle rate [kHz/mm^2]	10	10^3
Readout architecture	Asynchronous	
Analogue power [mW/cm^2]	5.4	~ 70
Digital power [mW/cm^2]	31.5/14.8	2.5 (0.84 MHz/mm^2) 79.6 (27.2 MHz/mm^2) (matrix only)
Total power [mW/cm^2]	36.9/20.2	~70 – 150 depending on rate
NIEL [1MeV n_{eq}/cm^2]	1.7×10^{13}	$> 1.0 \times 10^{15}$
TID [Mrad]	2.7	100

MALTA

- Significant modification/re-design needed to meet EIC requirements

- The current version of the sensor is a prototype, **not experiment ready,** more submissions planned to get to the final version of the sensor

- However…
  - An experiment ready version of the MALTA may be interesting for forward tracking with added timing, see **LANL proposal for disks at large z**

  - The **TJ 180 nm modified technology itself could be used to design a dedicated EIC MAPS**; a feasibility study had been carried out by RAL CMOS Sensor Design group and Birmingham, see Iain's talk

New emerging development: 65 nm MAPS

- Recently, an effort is emerging to develop new generation **MAPS in a 65 nm CMOS imaging technology**

- Large interest in the HEP community to develop this process for future experiments
  - **ALICE ITS3 project**
  - **CERN Experimental Physics department R&D programme (WP1.2 MAPS)**

- This path is more attractive for the development of an EIC MAPS
  - **Improved performance** for precision measurements at the EIC
  - **Process availability** on the EIC project timescale
  - … but higher cost and complexity than older technology nodes

ITS3/EIC projects overlap

- The ALICE ITS3 project aims at developing a new generation MAPS sensor at the 65 nm node with extremely low mass for the HL-LHC
  - See Giacomo's talk

- As presented by Leo Greiner (LBNL) at the EIC Yellow Report Kick-Off meeting, this effort is particularly interesting for the EIC
  - The ITS3 **sensor specifications and development timescale** are largely compatible with those of the EIC
  - **Non-ALICE members are welcome** to contribute to the R&D to develop and use the technology for other applications

- Joining the ITS3 collaboration, the EIC can leverage on a large effort at CERN, sharing development costs, to design an innovative sensor solution at the 65 nm node, suited for an experiment starting in ~ 2030

This has been identified has the most efficient way forward

ITS3 sensor vs. EIC sensor

- The ITS3 sensor specifications even **exceed the EIC requirements**
  - Chosen technology: **TJ 65 nm process (backup: TJ 180 nm)**
  - **Higher granularity and lower power consumption** with respect to current simulation baseline (ITS2/ALPIDE-like)
  - **Shorter integration time, lower fake hit rate** (and better time resolution) than required at the EIC

ALICE

Specifications

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

M. Mager | ITS3 kickoff | 04.12.2019 |

[1] From EIC white paper, [2] ITS2/ALPIDE specification

Preliminary EIC MAPS sensor requirements compiled by Birmingham & RAL CMOS

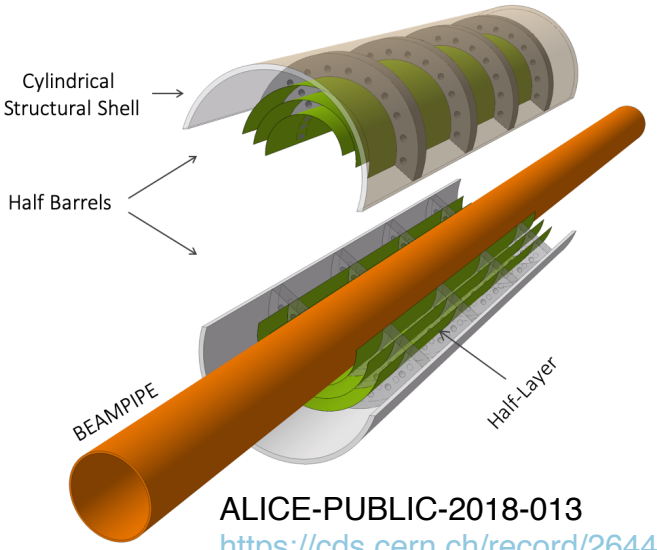
Parameter	EIC Vertex and Tracking MAPS	
Technology	TJ ISC 65 nm (Backup: TJ CIS 180 nm)	
Substrate Resistivity [kohm cm]	1 or higher	
Collection Electrode	Small	
Detector Capacitance [fF]	<5	
Chip size [cm x cm]	Full reticule or stitched	
Pixel size [µm x µm]	20 x 20	
Integration Time [µs]	2	
Timing Resolution [ns]	< 9 (optional)	
Particle Rate [kHz/mm^2]	**TBD**	
Readout Architecture	Asynchronous	
Power [mW/cm^2]	< 20	
NIEL [1MeV neq/cm^2]	10^{10}	[1]
TID [Mrad]	< 10	[1]
Noise [electrons]	< 50	
Fake Hit Rate [hits/s]	< 10^{-5}/evt/pix	[2]
Interface Requirements	**TBD**	

ITS3 detector concept & EIC vertex layers

- ITS3 uses design and post-processing techniques to reach an extremely low material budget of **0.05% X/X_0** per layer

- **Low power wafer-scale** sensors, thinned to **20-40 µm, bent** around the beam pipe → **air-cooling, support and services outside active area**

- Very attractive for the EIC vertex layers, possible option under investigation



ALICE-PUBLIC-2018-013
https://cds.cern.ch/record/2644611

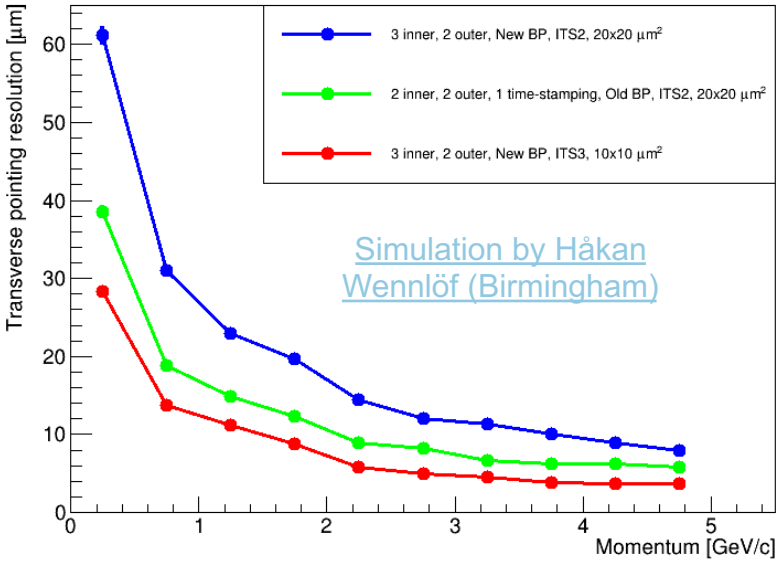
Advantages of ITS3-like vertex layers at EIC

- Pre-CD0 simulations assumed an 18 mm beam pipe (green line)
- With the increased beam pipe diameter, an ITS2-derived EIC SVT would see a significant degradation of vertex resolution (blue line)
- Vertex layers based on the ITS3 design with **10 µm pixel pitch** and **0.05% X/X_0 (red line)**, allow to **overcome performance degradation due to the larger beam pipe and reach the same (even improved) vertex resolution**

ITS2 vertex layers & old beam pipe:
20 µm pixel pitch, 0.3% X/X_0

ITS2 vertex layers & new beam pipe:
20 µm pixel pitch, 0.3% X/X_0

ITS3 vertex layers & new beam pipe:
10 µm pixel pitch, 0.05% X/X_0



Path to an EIC detector based on 65 nm MAPS

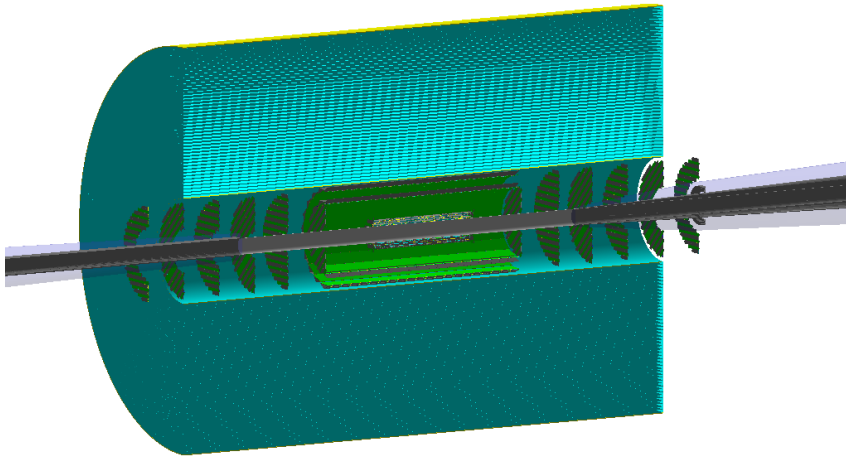
- Despite the large overlap, the EIC and ITS3 detectors have some significant differences, most notably the size
  - ITS3 is a **0.12 m^2**, three layers, **vertex** detector
  - The new YR baseline configurations of the EIC SVT have an area of approximately **12 m^2 and 15 m^2**, for hybrid and all-Si respectively

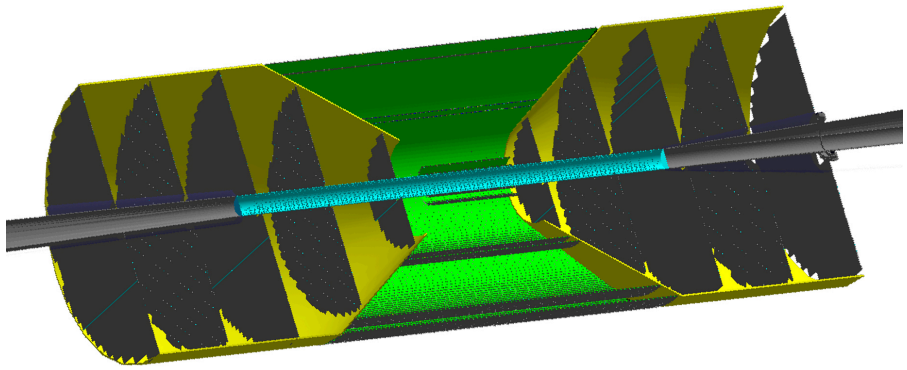
- Cost and yield of stitched wafer-scale sensors not compatible with use in the EIC detector outside the vertex layers → a **reticule-size sensor version needed for the EIC tracking layers and disks**

- Tracking layers and disks also need a dedicated, possibly more conventional design of support structures (**staves, disks**)
  - Dedicated engineering solutions need to be developed

YR baseline detector configurations

- New baseline based on the ITS3 sensor, services and support design
- Two configurations are simulated within the YR effort
  - Hybrid with gas outer tracker and end-caps
    - TPC barrel and large area MPGDs for end cap tracking
    - MPGD barrel and large area MPGDs for end cap tracking
  - All-Si compact tracker





10 μm pixel pitch
0.05% X/X_0 vtx layers
0.55% X/X_0 tracking layers
0.24% X/X_0 disks

EIC Silicon Consortium

- A group of institutions interested in joining the ITS3 R&D effort as a path to an EIC detector is starting to join together to form the EIC Silicon Consortium

- This group currently consists of **LBNL, Birmingham, RAL CMOS Sensor Design group, Wuhan, BNL instrumentation division, JLAB, Daresbury and Liverpool**
  - …. many other groups expressing strong interest and expected to join soon

- Very early/informal phase of development
  - Institutes joined, expressing areas of interest/contribution
  - A mailing list is setup for communications

EIC Silicon Consortium: sensor design effort

- The first effort of the consortium concentrates on contributing to the **silicon design and characterization by joining the ITS3 sensor R&D**
  - Work already underway with CERN/ITS3 to access the technology and join the relevant work packages

- Some of these institutes have already joined the ITS3 R&D effort formally, and more institutes will be joining the ITS3 R&D effort formally in the next few months

- See Iain's talk for ongoing and planned work within ITS3 to develop the EIC MAPS sensor

EIC Silicon Consortium: planned activities

- As the silicon design progresses and the outlines of the EIC specific sensor fork take shape, we will start organizing **our own internal work packages** to address the parts of the detector implementation needed for an EIC application
  - These will include mass testing, module design, stave design, disc design, EIC specific infrastructure, etc.

It is our intention to develop a full silicon detector implementation and to integrate the consortium into an EIC Silicon Detector collaboration

- If you want to join, please contact Leo Greiner lcgreiner@lbl.gov

Conclusion

- An efficient design path to an EIC silicon vertex and tracking detector has been identified based on 65 nm MAPS
- An international silicon consortium is forming to develop an ITS3-derived EIC MAPS sensor with associated services, support and readout infrastructure
- ITS3-derived baseline detector configurations for hybrid and all-Si SVT concepts prepared for the EIC YR tracking WG studies
- Work has started towards the MAPS sensor development in 65 nm for the EIC SVT