

Required Sites and Infrastructure for Assembly: The ALICE ITS Upgrade

Nicole Apadula Lawrence Berkeley National Lab EIC Silicon Workshop September 4, 2020



Outline

- Background on the ALICE ITS upgrade
 - What & Why
- Scope of the project
 - What does it take to build something of this scale?
 - Time, manpower, sites
- LBL contribution to stave assembly

ALICE Upgrade: Motivation & Needs





Motivation: QGP precision study

- High precision measurement of heavy flavor hadrons
 - Large range of p_T & rapidity, centrality & reaction plane binned

• Requires:

- Excellent tracking efficiency & resolution at low pT
- Large statistics with MB trigger

Strategy:

- Readout all Pb-Pb interactions at 50 kHz
- Improve vertexing & tracking capabilities



ALICE ITS: Design Requirements

- Higher resolution of impact parameter (Factor of 3 in $r\phi$, 5 in z)
 - Reduce beam-pipe diameter
 - 29 mm → 17.2 mm
 - Minimize distance between beam axis and first detector layer
 - 39 mm → 21 mm
 - Reduce pixel size
 - 50 μm x 425 μm → ~30 μm x 30 μm
- Increase tracking efficiency at low p_T (60% at 100 MeV/c)
 - Reduce material budget (sensors, power, cooling)
 - > 1% $X_0 \rightarrow$ < 0.5% X_0 inner layers
 - Added layer of silicon detectors
- More statistics
 - Faster read-out (100 kHz) for increased luminosity (10 nb⁻¹)



ALICE Inner Tracking System





The ITS Upgrade

7 layer barrel geometry, fully equipped (~24000 chips) with dedicated **MAPS**:

ALice Plxel DEtector (ALPIDE)

r-coverage: 23 – 400 mm

 η coverage: $|\eta| \le 1.3$



Monolithic Active Pixel Sensors



Material /layer : $0.3\% X_0$ (IB), $1\% X_0$ (OB)

12.5 G-pixel camera (~10 m² active Si) Binary read-out

Chip Development



Design team from CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC



P.Riedler, CERN | PSI Seminar



Detector Construction: Blank Wafers

Sun SEMICONDU 1500 wafers TOWERJO 1% for QA **//TMEC** Blank Wafers (1500 25-µm high resistivity epitaxial) - produced by MEMC (SunEdison): all done - QA (surface resistivity map and resistivity profile) by Thai Microelectronics Centre (TMEC)



FuRex

Detector Construction: CMOS production

CMOS Production (baseline: 1200 wafers)

8% for wafer test

- produced by TowerJazz: all done waiting for yield numbers
 + requests from other projects
- shipped to Furex for thinning and dicing
- 2 wafers per lot to CERN for wafer probe testing and quick feedback to foundry

after wafer test

TOWERJAZ



FuRex

Detector Construction: Chip thinning and dicing

Thinning and Dicing (50 µm for Inner, 100 µm for Outer Barrel)

50 µm chips

- done by FuRex: production ongoing
- 50% of 100 µm chips to Seoul (Yonsei University)
- 50% of 100 µm chips to Pusan (Pusan and Inha Universities)
- 100% of 50 µm chips to CERN

Magnus Mager (CERN) | 6th Annual MT Meeting | 17.06.2020 |

Detector Construction: Chip testing







Detector Construction: Module assembly

Module assembly and distribution (100 μm) at Bari, Pusan, Liverpool, Strasbourg, Wuhan done

Nikhef

INF

Stave assembly





Detector Construction: Stave assembly, detector integration



Detector Construction: Extras (PB, RB, FPC, CP, SF, small parts)







Pieces for Stave Assembly



OB Module Production







- Modules assembled with custom machine (ALICIA)
 - Aligned chips with +/- 5 µm precision
 - Can probe & automatic visual inspection
- Produced at 5 sites worldwide
 - Strasbourg, Bari, Liverpool, Pusan, Wuhan



ITS Outer Barrel Structure



Outer Barrel (OB)

<radius> (mm): <u>194, 247</u>, 353, 405 Nr. staves: <u>24, 30</u>, 42, 48 Nr. Chips/layer: <u>6048 (ML)</u>, 17740 (OL) Power density < 100 mW / cm²

LBL built Middle Layers in Red

Length (mm): 900 (ML), 1500 (OL) Nr. modules/stave: 4 (ML), 7 (OL) Material thickness: ~ 1% X_0 Throughput (@100kHz): < 3Mb/s × cm⁻²



Stave Assembly Requirements

- OL (4 sites): 30 staves per site, 1 stave every 2 weeks
- ML (LBL): 60 staves, 1 per week
- >90% production yield
 - > 10 assembly steps \rightarrow each must have ~99% yield
- Within 1 mm tolerance for planarity
 - Clearance for neighboring staves
- Noisy pixel rate below 10⁻⁵





Stave Assembly Dependencies

- Each Stave takes ~5-6 days to complete
 - 1 per week requirement for ML
- Modules arriving from 5 different sites
- Carbon Fiber Cold Plates & Space Frames from CERN
- Power & Bias Bus shipped through CERN





Infrastructure for Stave Assembly

- 3 separate spaces
 - Module testing (small)
 - HS assembly
 - Stave completion

CRYSTA-Apex S 900 Series









- HIC arrives
 - Tested and tab cut







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- 4 HICs glued to CP (1 HS)
 - Aligned within 20 µm of nominal







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- Stave gets final metrology





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- Stave is folded & tested





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- PB soldered to Stave & tested
- Stave is folded & tested
- Stave is boxed & stored/shipped to CERN

Production completed in October '19





- Planned deliverables: 60 staves (54 + 6 spares)
 - Constructed 68 staves, 64 detector grade (no more than 1 dead chip per HS)
 - Rate ~1/week
- 17 trips made delivered 4 at a time
 - Last trip made October 2019





https://newscenter.lbl.gov/ 2019/09/19/how-to-get-a-particledetector-on-a-plane/

Activity at CERN



- Both half barrels complete
- Commissioning shifts restarted ~ 2 weeks ago
- Installation planned for Jan







Summary



Expect any EIC silicon detector to be similar

- Power, mechanics, silicon, detector assembly
- Requires investment in expensive machine infrastructure
 - E.g. CMM, probe testing, other assembly tooling