CDET DAQ Upgrade

SBS Collaboration Meeting

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Jefferson Lab

U.S. DEPARTMENT OF ENERGY | Office of Science

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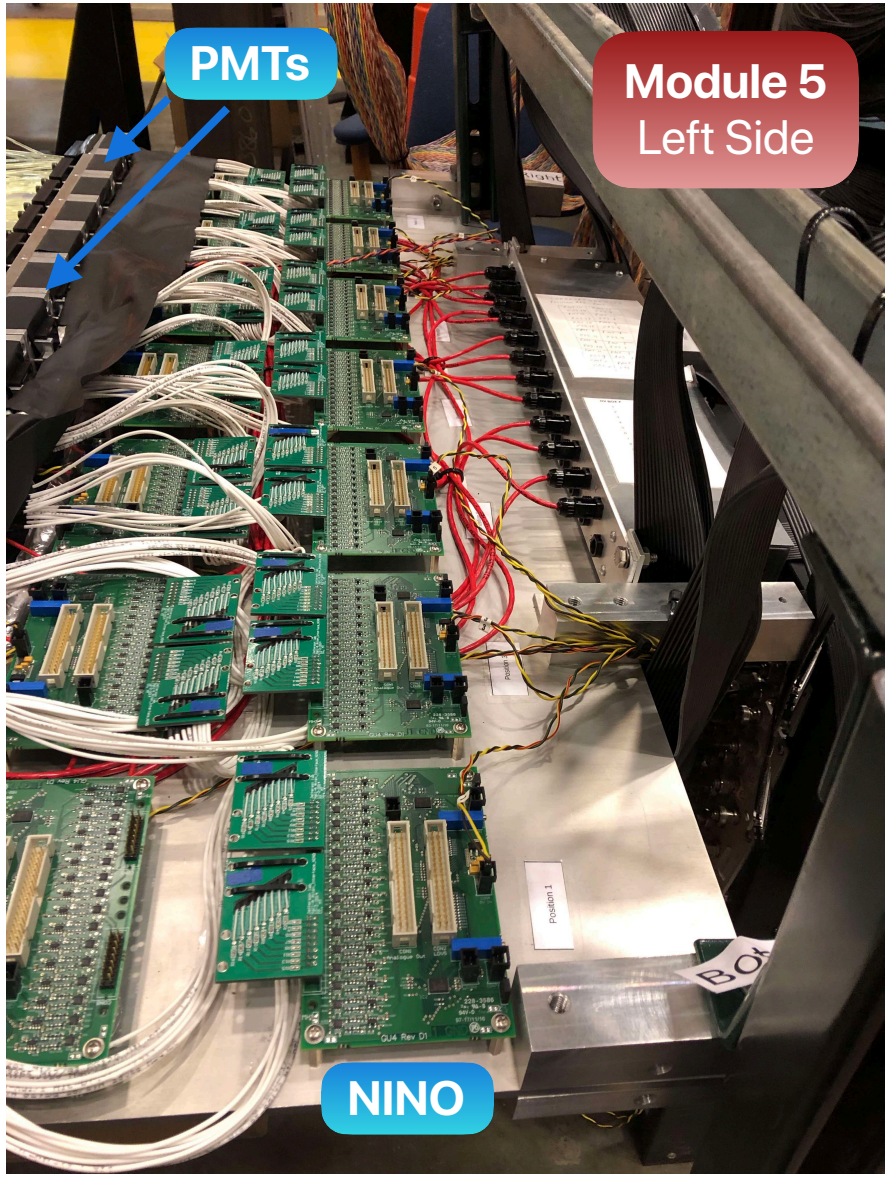
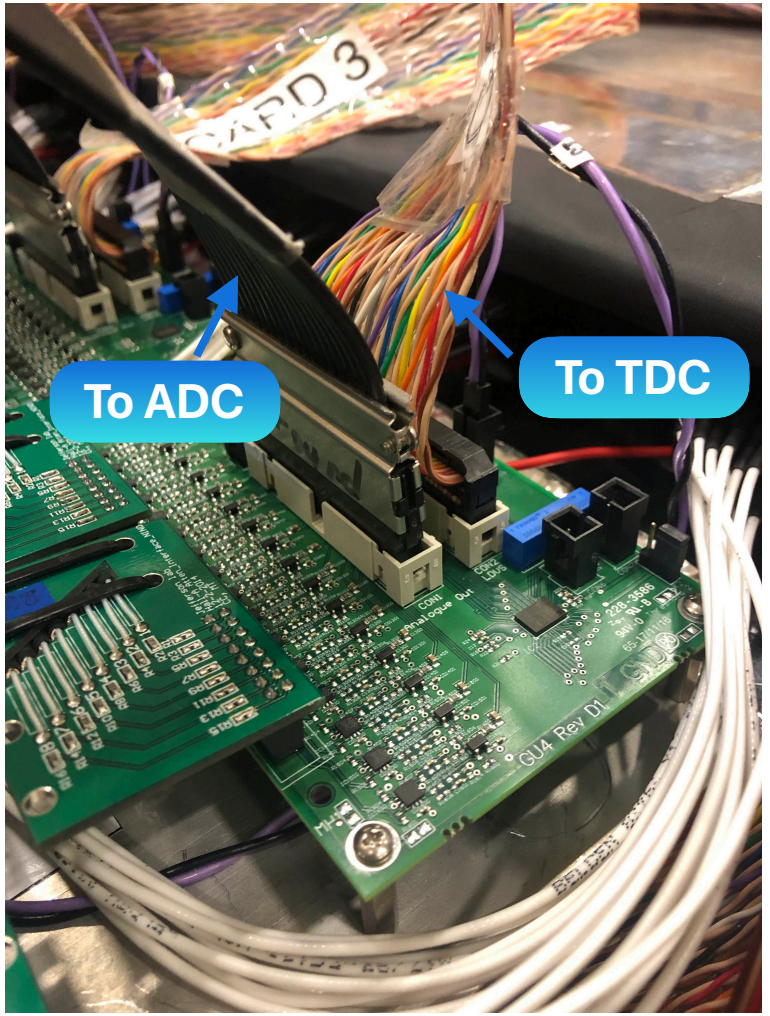
Setup in Test Lab

- Cosmic test stand: Assembled modules taking data
  - **Complete**: 1, 2, 3, 5 (right side)
  - **Remaining** to test: 4 and 6
- Stand-alone DAQ
  - Hardware:
    - FE NINO (Glasgow U)
    - Fastbus: ADCs, TDCs
    - HV PS (on loan from FNAL)
  - Software: CODA 2.6





Pictures: Taylor Edwards

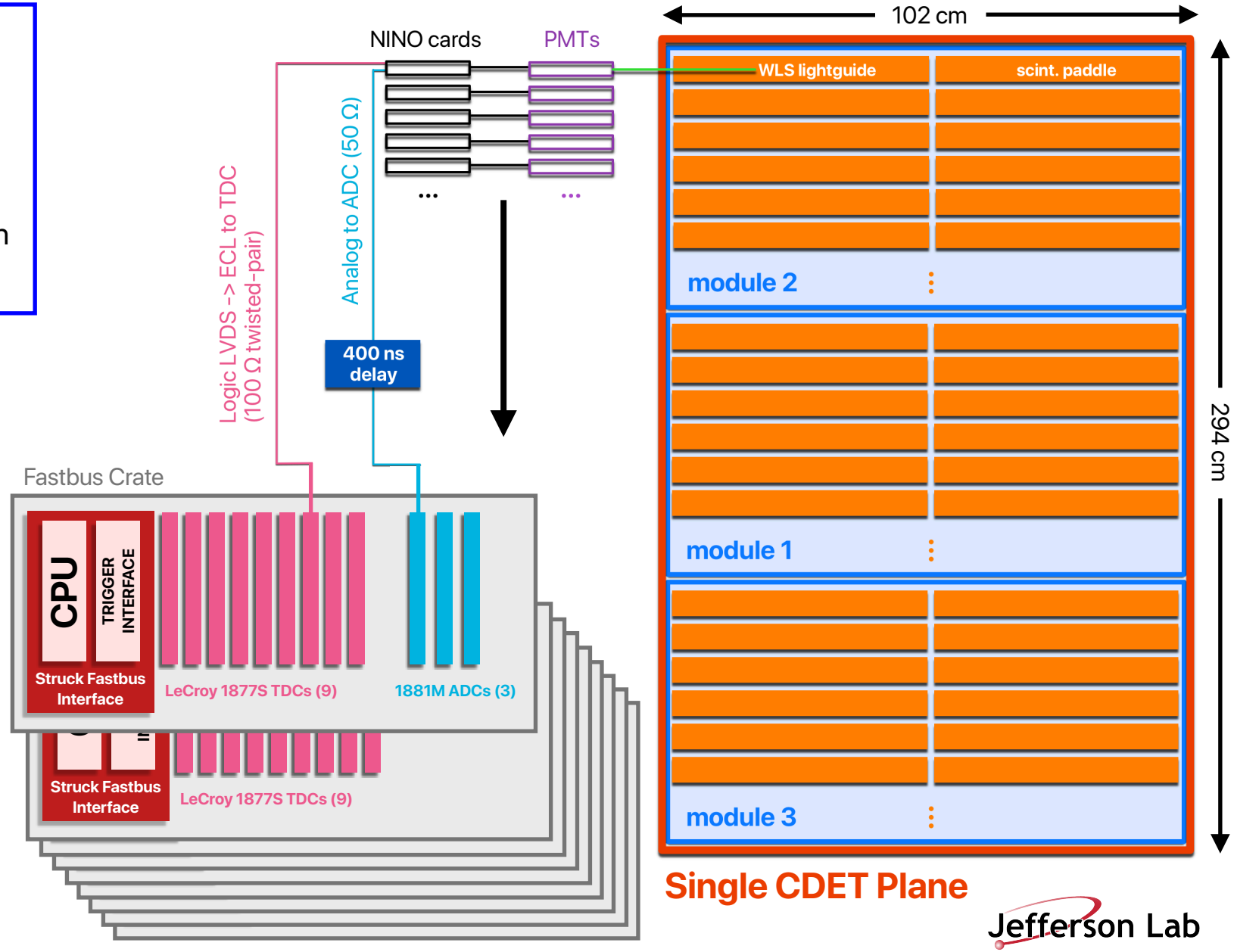
Current Setup

Limitations & Challenges

- TDC sustained data transfer rates ~20 MB/s
- ECAL trigger rate ~200 kHz => ***44% dead time***
- Present solution: Split TDCs across 9 Fastbus crates => need 84 TDC modules; necessitates an additional weldment for this DAQ

Hardware

- 392 scintillator paddles/module (2352 total)
- 28 16-channel PMTs/module (168 total)
- 28 16-channel NINO cards/module (168 total)
- 3 modules/plane (6 total)
- 2 planes
- 9 Fastbus crates
- 84 LeCroy 1877S TDCs
- 3 LeCroy 1881M ADCs (PMT HV tuning use only)



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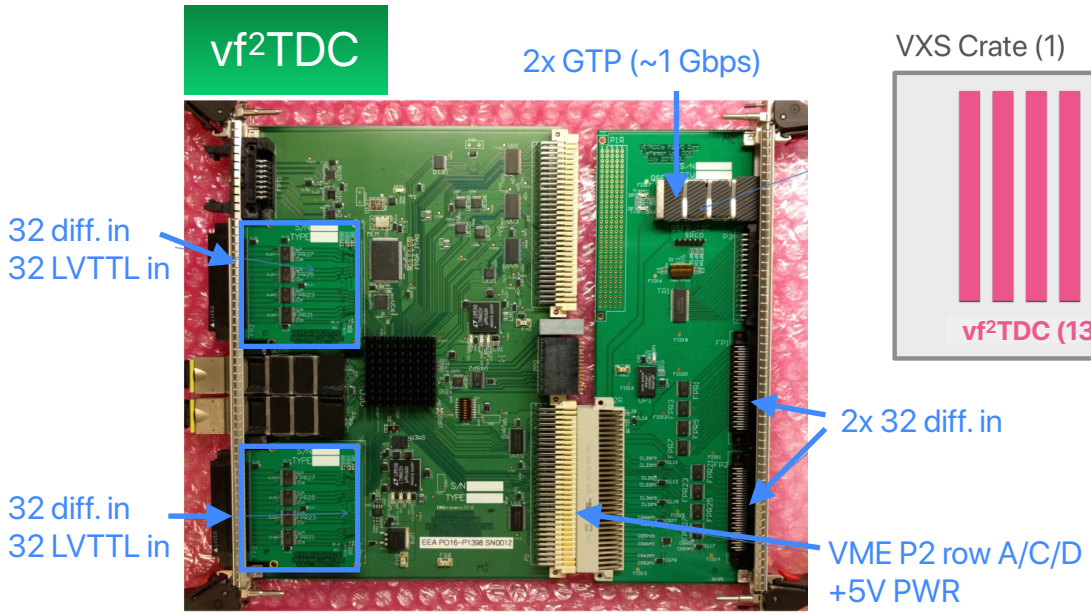
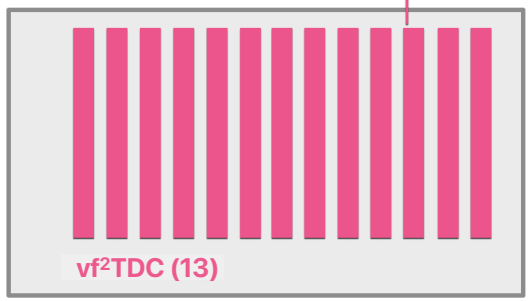
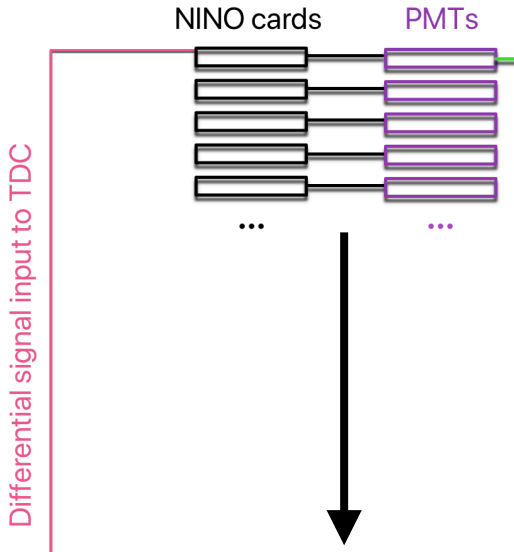
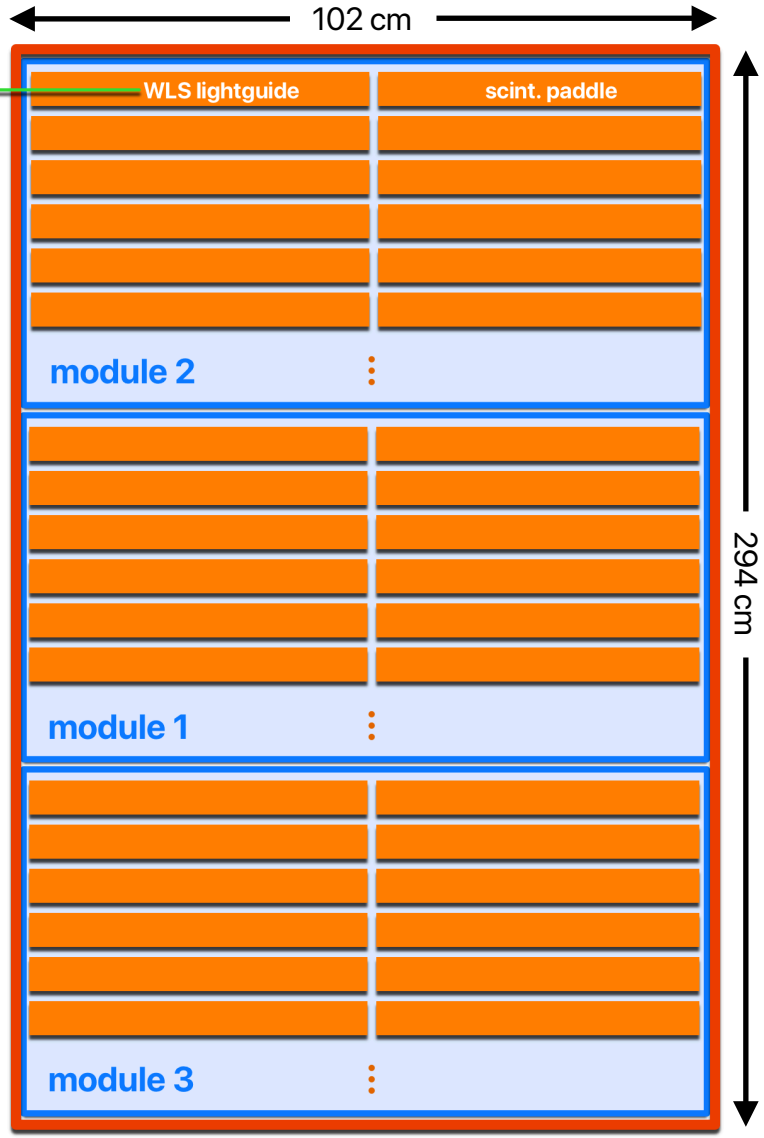
Approved Upgrade

- Move to **VETROC** system
- VXS FPGA-based flash TDC (vf²TDC)
- Single board: 128 (64) front (back) panel inputs (192 total)
- 13 vf²TDC boards in a single VXS crate
- Reduction of space needed









Single CDET Plane

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Comparing Fastbus and VETROC

Item	Fastbus	VETROC
Data Transfer Rate	20 MB/s	200 MB/s
Trigger Rate	10 kHz (L2A)	200 kHz (L1A)
Timing Resolution	0.5 ns	≤ 1 ns
Dead Time	4%	1%
Deployment	Triple number of cables	Standard cables

Implementation in the Hall

- **Have to work through and finalize the details**
- Separate weldment for CDET
- VXS crate + patch panels + cables + …
- Test everything before moving into hall
- Note: We can generate a trigger from VETROC for TDIS (RICH Cherenkov)

VETROC Timeline and Cost

- Will use the same setup as Compton Electron Detector => minimize development time
- Main tasks
  - Order vf²TDC boards (3 month acquisition time)
  - Set up VXS crate (1 month)
  - Merge with high-resolution firmware (1 month)
  - Update software to handle high resolution (1 month)

Item	Quantity	Extended Cost ($k)
VXS Crate	1	15
vf²TDC Boards	15 (13 + 2 spare)	28
Signal Distribution	1	1
TOTAL		44

Funding from collaborators
- $25k from INFN
- $20k from UConn
- Split into two installments

Summary and Plans

- CDET system set up in test lab, taking cosmics data
  - Existing system capable of handling high-rate data, at the cost of tripling number of components
- VETROC: reduced dead time, compact & modern setup
  - Cost ~$44k
  - 3-month acquisition time, ~3–4 month development time
- What's Next?
  - Get vf^{2}TDC boards ordered
  - Evaluating hardware and software needs for VETROC transition
    - Learning CODA
    - Getting familiar with Compton DAQ setup

Backup

Fastbus Dead Time

- Trigger rate
  - From GEp(5) proposal: ~100 kHz for threshold corresponding to e- with 85% of elastic energy
  - SBS DAQ Implementation Note: 200 kHz
- Assume 10% occupancy of CDET (rate per bar ~ 2 MHz, 50-ns window)
  - 0.1*(~2400 channels) = 240 channels per event
  - Let's say 1 hit per channel
- LeCroy 1877S TDC encoding time:
  - From the manual: 1.7 us + $(N_{ch})(N_{hits}/ch)$(0.05 us/hit)
- We have 9 Fastbus units, 84 TDCs (total)
- Number of channels per TDC: 240/84 = 3 ch/TDC
- Encoding time per TDC = 1.7 us + (3 ch)(1 hit/ch)(0.05 us/hit) = 1.85 us
- Dead time = (200 kHz)(1.85 us)(1/9) = (0.37)/9 = 0.04 => **4%**

9 Fastbus units; switch to new one when receive busy signal

VETROC Dead Time

- VETROC notes: vf²TDC dead time ~ 3 ns/hit
- Assuming 240 hits/event (see previous slide)
- 13 modules in VXS crate => 240/13 = 18 hits/module
- Module dead time = (3 ns/hit)(18 hits) = 54 ns
- Dead time = (200 kHz)(54 ns) = 0.01 = **1%** (assuming parallel readout)
- **Firmware Notes**
  - Standard firmware (w/ trigger generation): 1 ns resolution
  - Separate firmware (w/o trigger): < 1 ns; Could use for GEp