CODA Evolution
Concepts for Streaming Readout

Streaming Readout VI – May 13-15, 2020

Virtual Meeting

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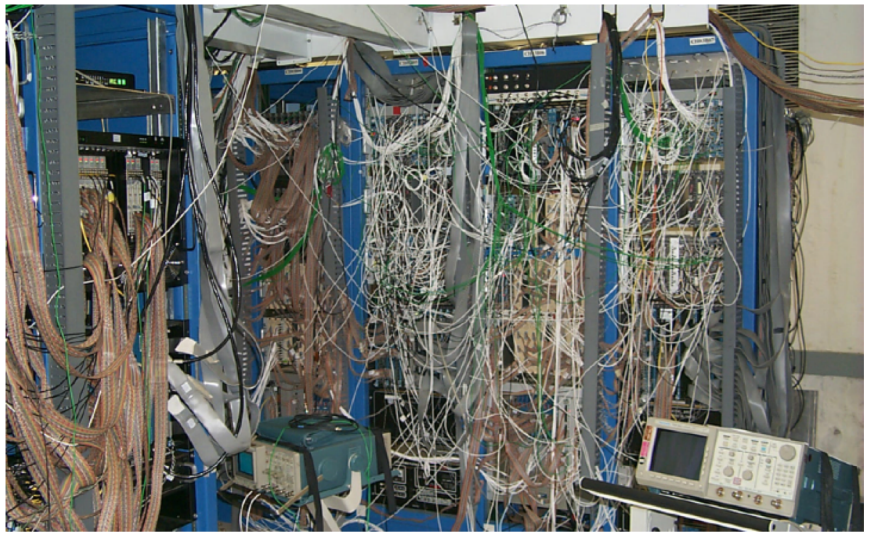
Data Acquisition Support

Jefferson Lab – Physics Division

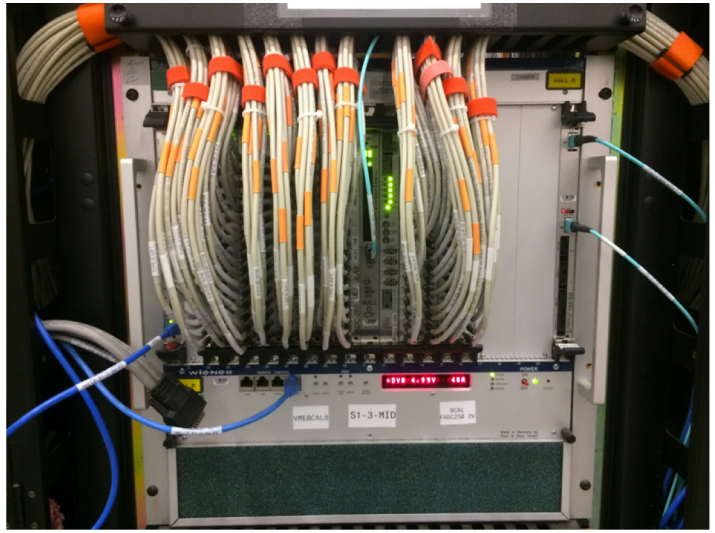
Jefferson Lab

We have come a long way…



1994 Hall C – Trigger and DAQ

25 Years



2019 Hall D – VXS Readout Crate with Trigger Processor (CTP/VTP)

- Circa 1988 – The Lab is under construction
- The plan – 3 Experimental Halls
- Why not – "*One DAQ to run them all*"
- Dedicated "DAQ" Group was formed
- CODA (CEBAF Online Data Acquisition) was born

- 25+ Years later CODA is in its 3rd generation and we are now contemplating the 4th for Streaming Readout support.

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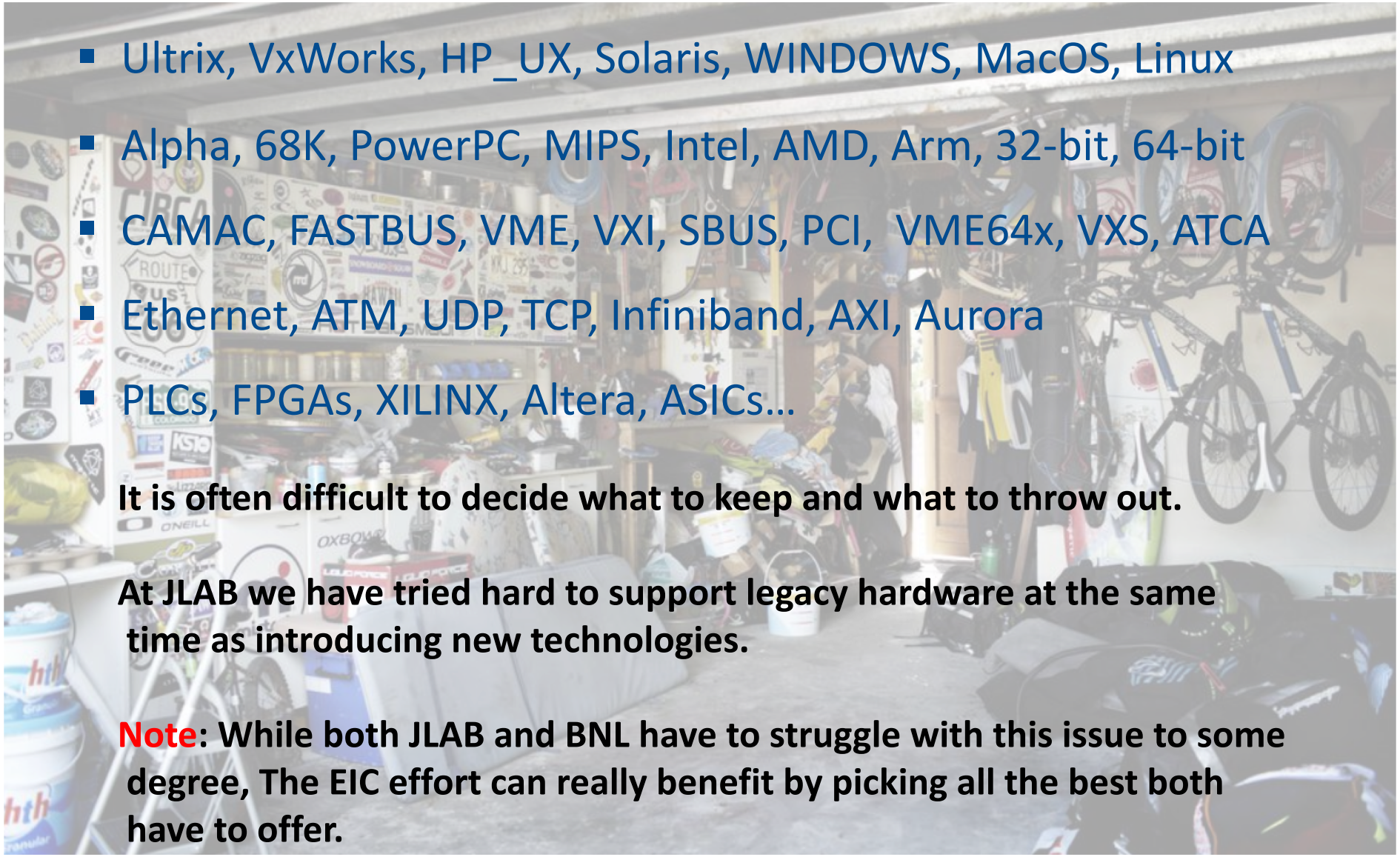
After 25 years the garage is a bit cluttered



- Ultrix, VxWorks, HP_UX, Solaris, WINDOWS, MacOS, Linux
- Alpha, 68K, PowerPC, MIPS, Intel, AMD, Arm, 32-bit, 64-bit
- CAMAC, FASTBUS, VME, VXI, SBUS, PCI, VME64x, VXS, ATCA
- Ethernet, ATM, UDP, TCP, Infiniband, AXI, Aurora
- PLCs, FPGAs, XILINX, Altera, ASICs…

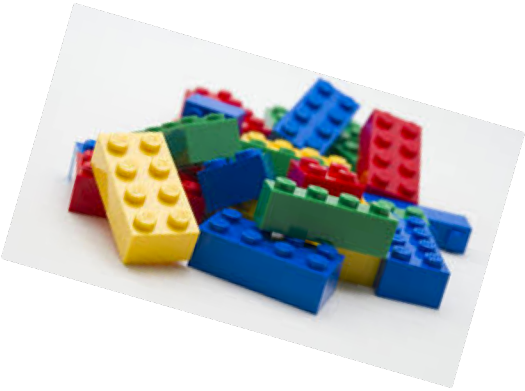
It is often difficult to decide what to keep and what to throw out.

At JLAB we have tried hard to support legacy hardware at the same time as introducing new technologies.

Note: While both JLAB and BNL have to struggle with this issue to some degree, The EIC effort can really benefit by picking all the best both have to offer.

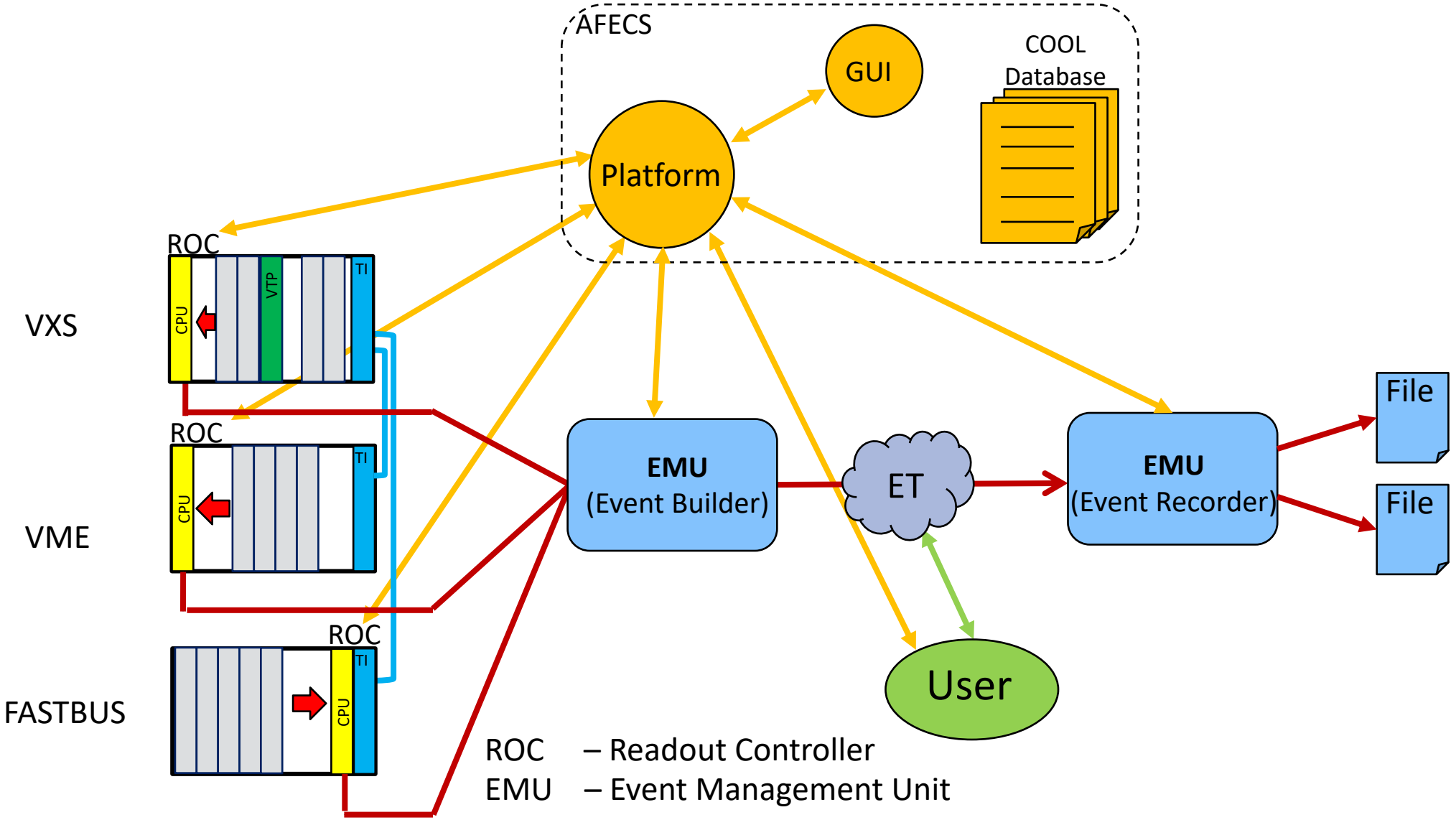
CODA

- What is CODA (also see coda.jlab.org)
  - Software toolkit for implementing data acquisition systems.
  - Hardware/Electronics
    - Custom boards like trigger, TDCs and ADCs.
    - Support for commercial hardware.
  - Software includes :
    - Interface with electronics (libraries/drivers).
    - Readout Front End and format data (ROC)
    - Inter-process communication - Control and Data (cMsg)
    - Merge data streams (DC, PEB, SEB)
    - Give users access to data for analysis and monitoring (ET System)
    - Write data to files (EVIO, ER)
    - Manage and control the data acquisition system (AFECS)



- CODA is modular. Build a single crate DAQ or a full Experimental Hall system

CODA 3



ROC – Readout Controller
EMU – Event Management Unit
ET – Event Transport
AFECS – Agent Framework Experiment Control System

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Multi-staged and parallel

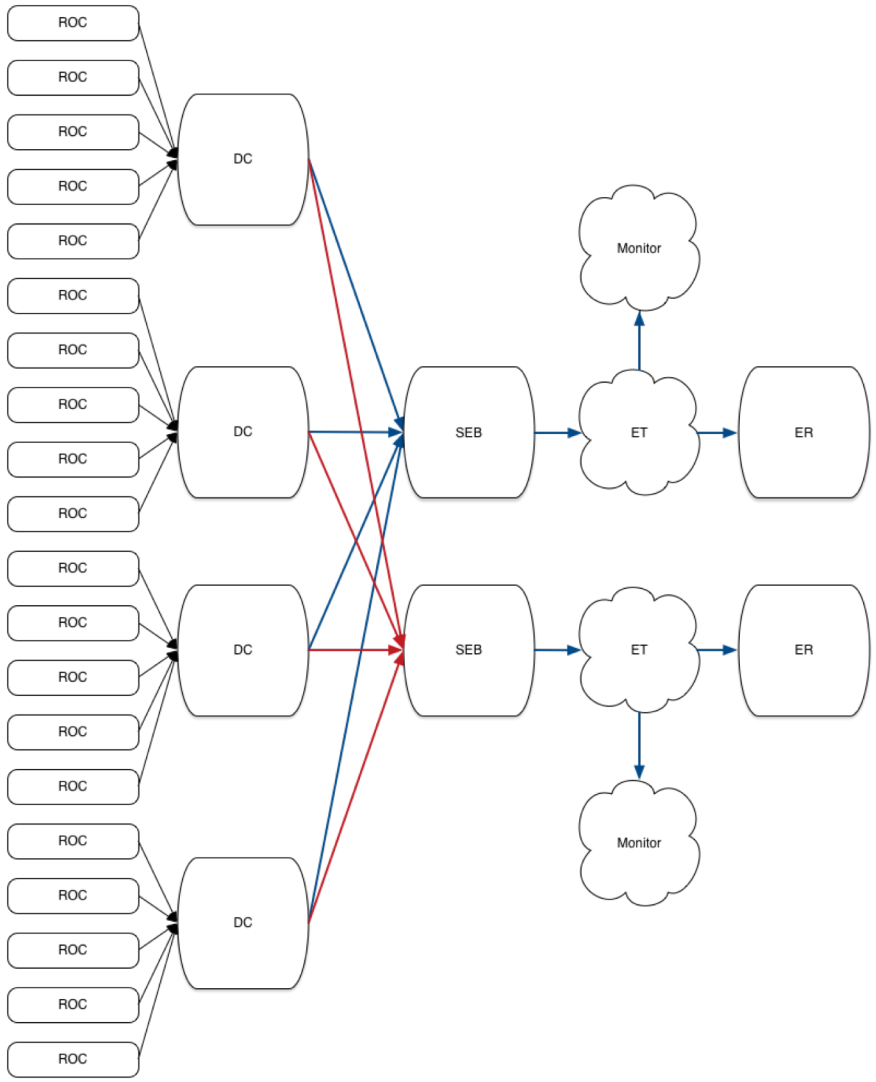
- CODA is modular and can be scaled
  - Multi-stage Event Building
  - Parallel “streams”

- Looking at the diagram however one can not really differentiate if it represents a “Triggered” system or a “Streaming” system.

- In evolving CODA to support streaming readout we are initially looking to the Front-End - where the streams originate.

- We have seen the initial experience with TRIDAS tests in Hall B (see S. Boyarinov talk) which provide a proof of principle.

- Now at JLAB we want to work on how to standardize the Front-End to support both Triggered and Streaming architectures in all 4 Experimental Halls.



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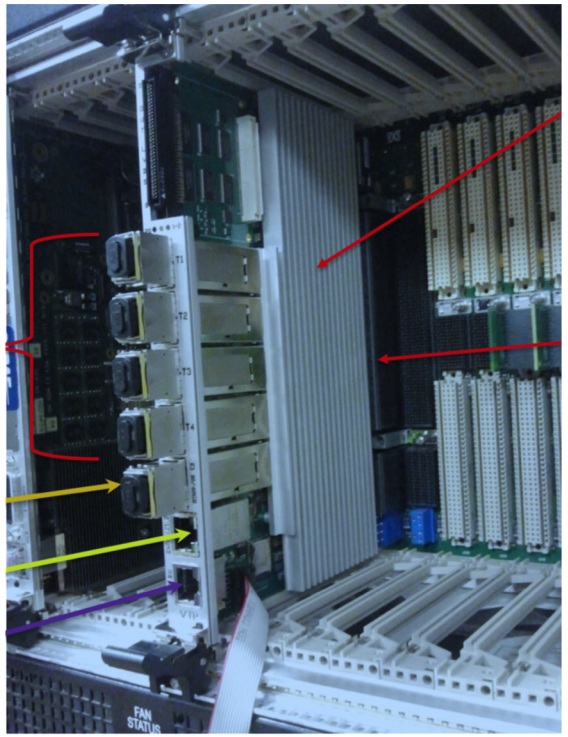
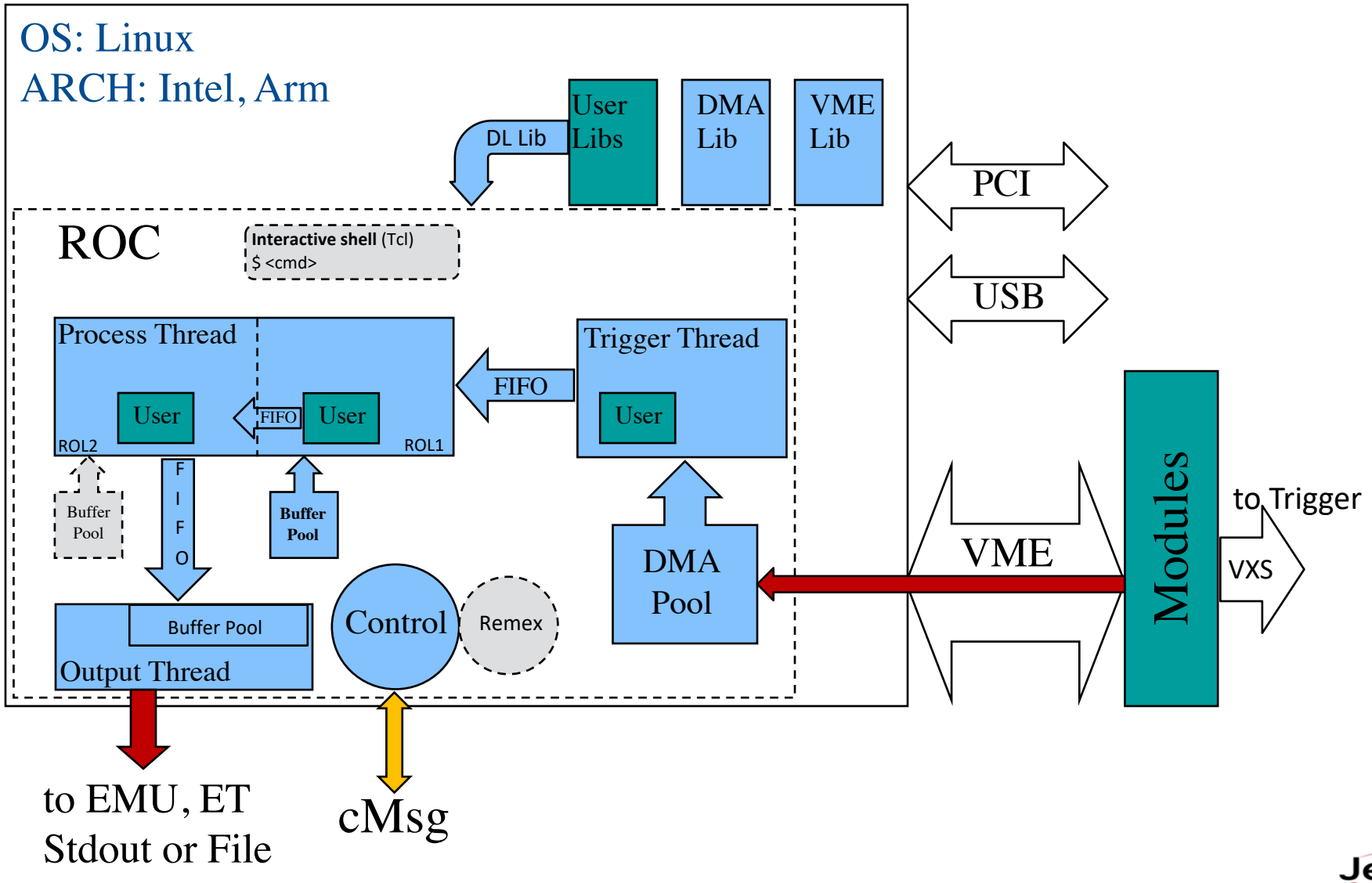
CODA – VXS Front-end

- The VXS crate supports
  - VME64x Backplane (19 slots) Readout ~200MB/s
  - High speed serial crossbar (20Gbps from each of 18 payload slots to 2 switch slots).
- VME CPU + JLAB Trigger Processor (VTP) provide Linux OS with access to both.
- Payload modules include:
  - 250 MHz Flash ADCs (16 chan/module)
  - JLAB SSP: general FPGA board supporting up to 32 fiber links from custom front-end electronics.
- We standardized on this platform for the 12GeV upgrade. JLAB bought a bunch of these crates. We need to use them for a long time.

VTP



CODA 3 – Current Front End



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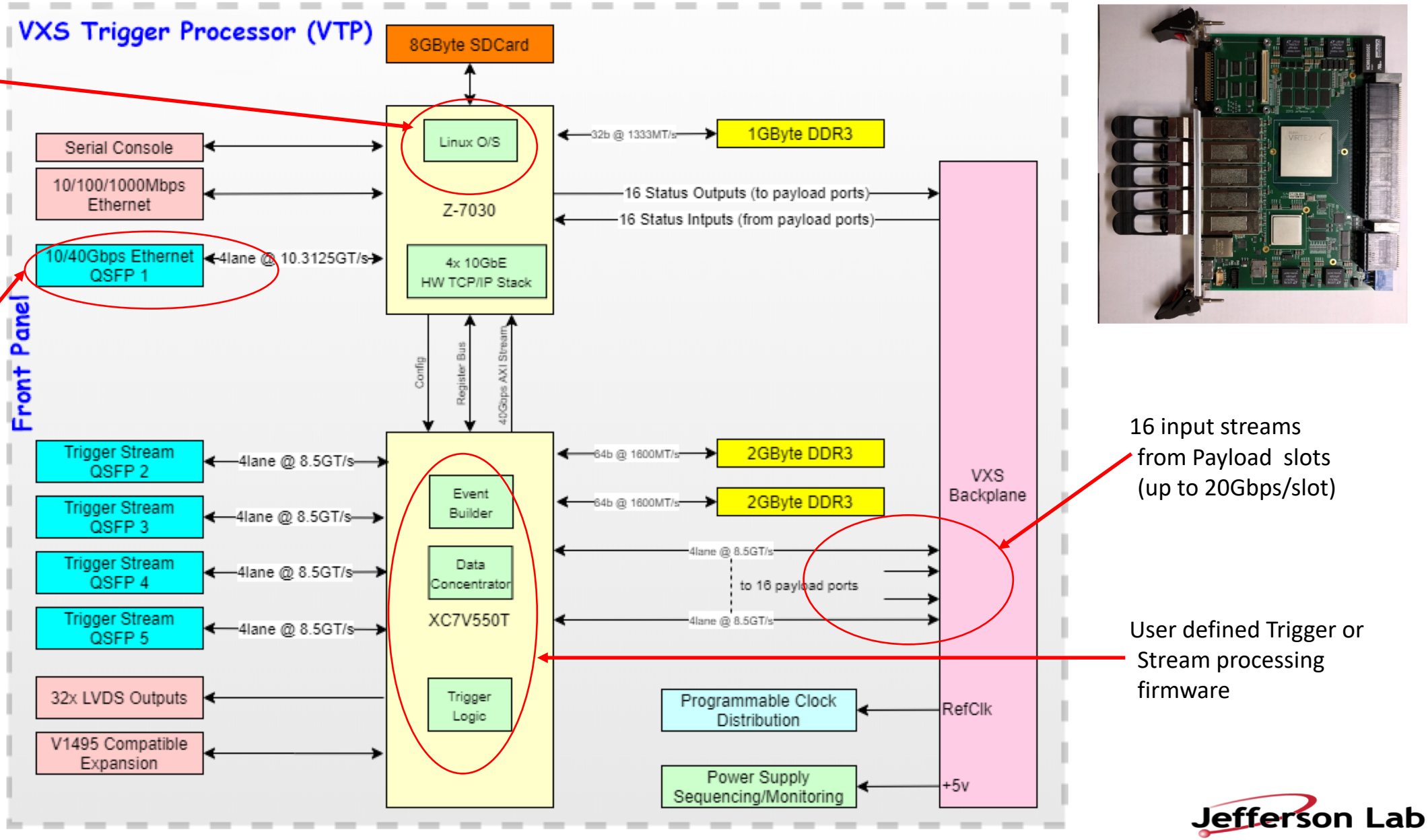
JLAB – VTP Board

CODA ROC Component

Four independent 10Gbps Ethernet ports



16 input streams from Payload slots (up to 20Gbps/slot)

User defined Trigger or Stream processing firmware

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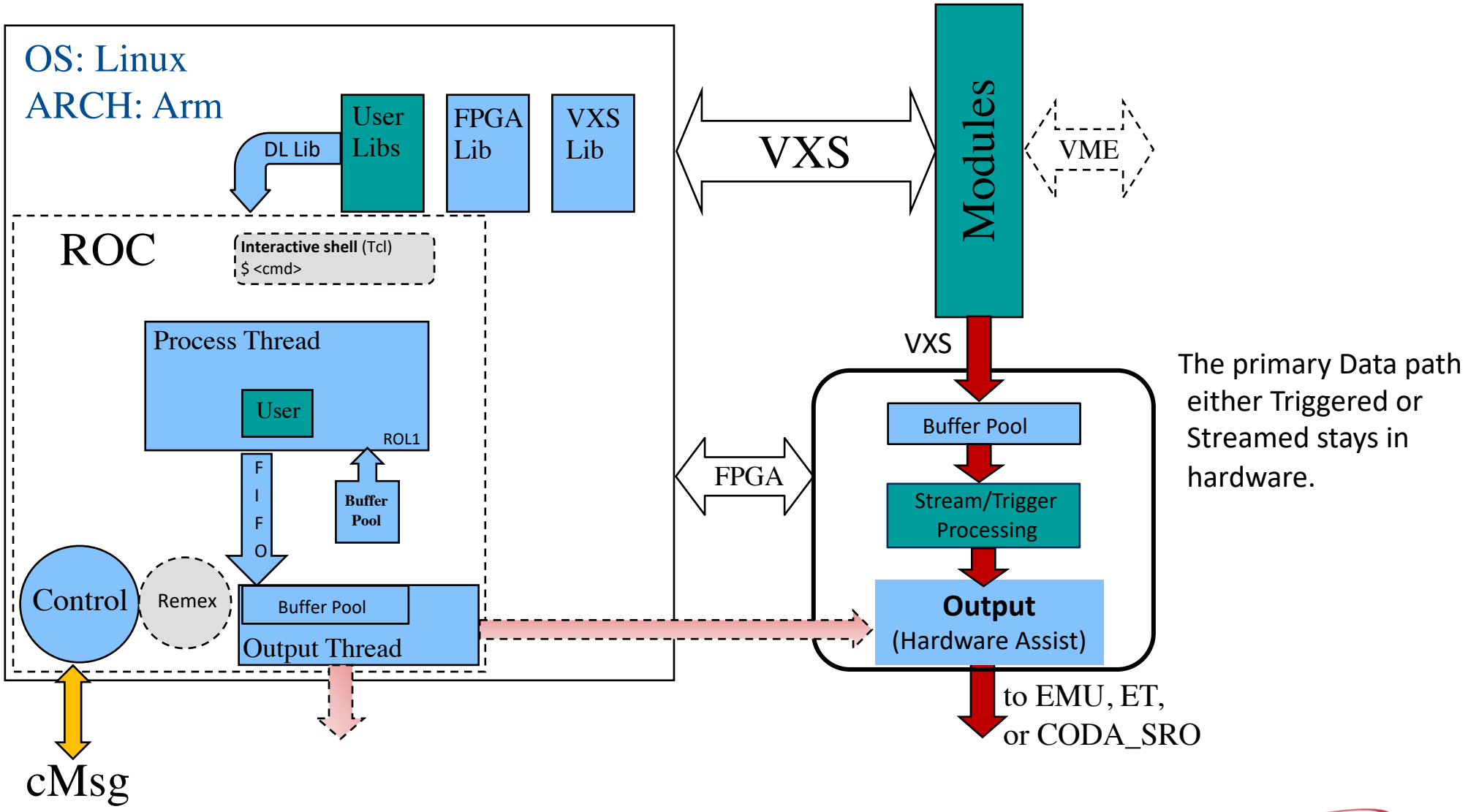
CODA – SRO Front End (on VTP only)



The primary Data path either Triggered or Streamed stays in hardware.

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CODA “Gen 4” – Streaming

- A transition to support of Streaming does not have to be done at the expense of the older Trigger based systems. A “Hybrid” system seems not only possible but actually preferred.
  - JLAB clock/trigger distribution already exists and is suitable for both. Upgrades are also being considered (see J. Gu talk)

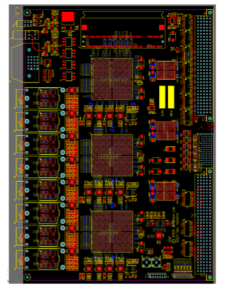
- Flexible FPGA front-ends can be enhanced by providing a User friendly and adaptable software framework (the CODA ROC) along with general driver libraries allowing User configuration and/or loading of custom firmware objects in the FPGA at runtime.

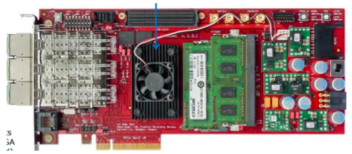
- CODA Back-End components supporting the streaming model are being developed (see V. Gyurjyan talk) and can be integrated with the AFECS control system as well as with possible online processing/filtering framework like JANA2 (see D. Lawrence talk).

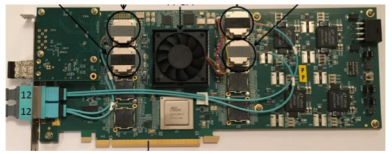
- Future experiments at JLAB (eg TDIS, MOLLER, SoLID) can benefit from current proposed developments with or without streaming.

CODA “Gen4” Extensions and User Support

- Proliferation of ASIC/FPGA front-end electronics for detectors is growing. Streaming data directly from the card via:
  - Standard ethernet(UDP/TCP) direct to PC or commercial network
  - Proprietary fiber link to another FPGA board (eg SSP, C-RORC, FELIX)

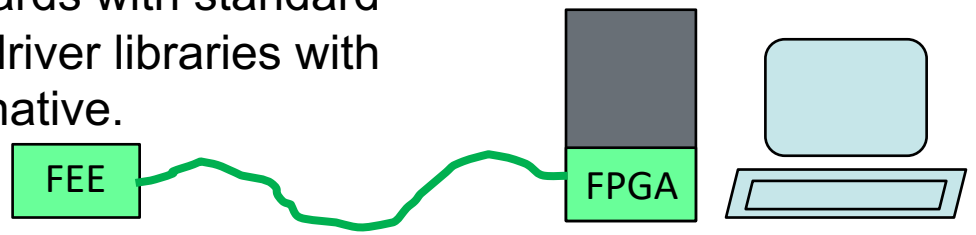






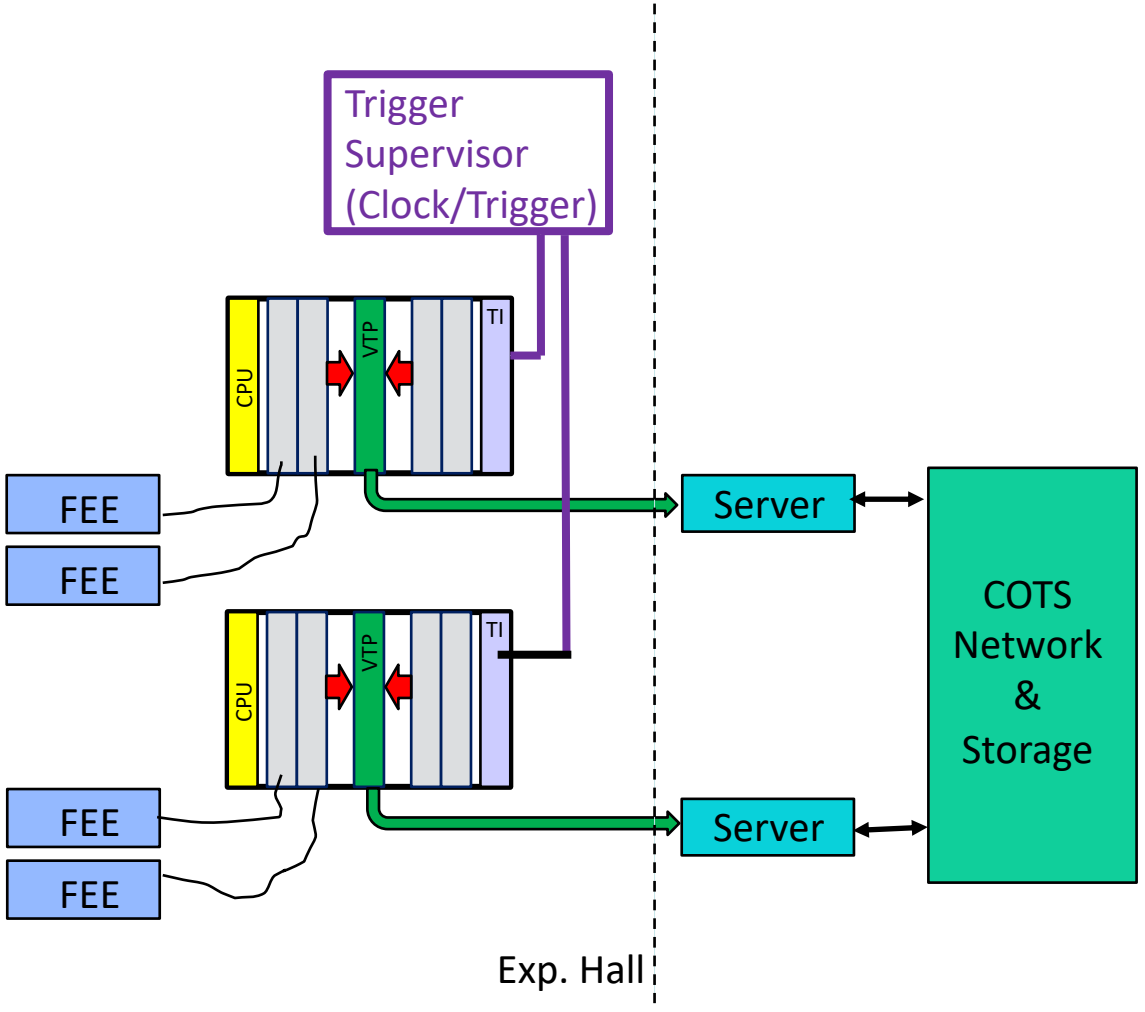
- General support for these architectures seems appropriate and we are doing this (see E. Jastrzembski talk). However there are obstacles:
  - Custom hardware (at both ends) not always readily available.
  - Requires more responsive collaboration with other labs/groups.

- User support of small development test beds is often greatly appreciated. Anything commercially available that can be User purchased and supported for DAQ (but not necessarily used in the “BIG” experiment) is worth supporting.
- There are many commercially available FPGA development boards with standard fiber interfaces in a PCIe formfactor. Developing firmware and driver libraries with these in mind would allow for an easy and less expensive alternative.

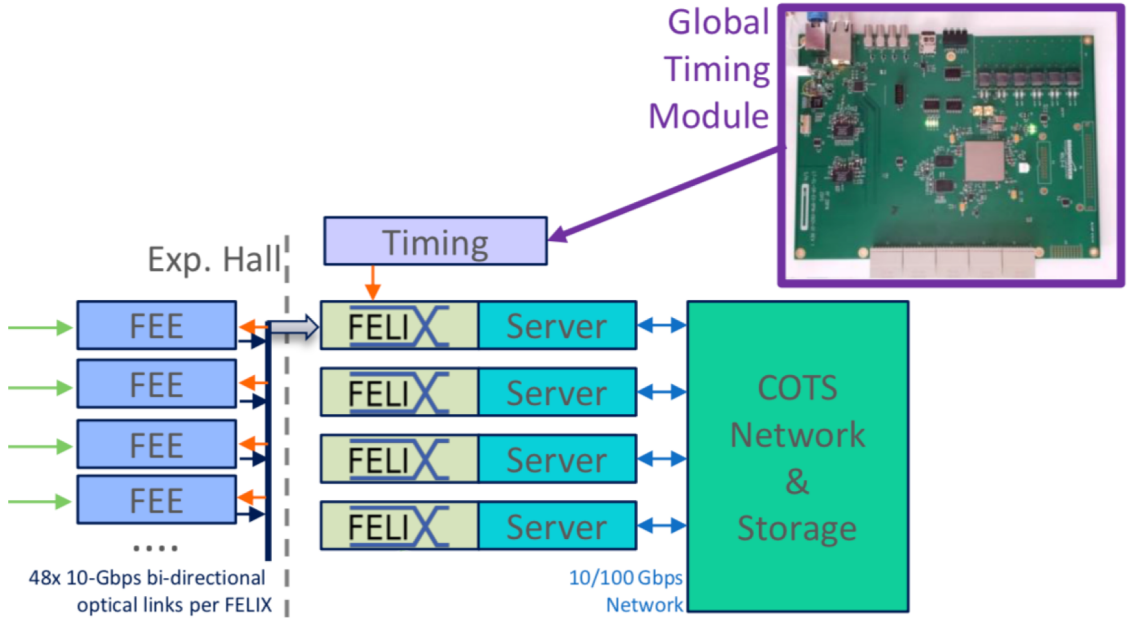


We are not so different, you and I…

JLAB



sPHENIX



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Summary

- From the very beginning JLAB has focused on hardware and software DAQ support flexible enough for use in all the experimental halls.
- The next generation of DAQ development at JLAB is clearly focused on Streaming readout, but we cannot abandon what we have now.
- Primary attention has to be toward the 12GeV program, but close collaboration with BNL and the EIC community can bring useful advances.
  - Integration of hardware like FELIX at JLAB
  - Standardizing on well supported software tools on the back end
  - Attention to flexible User configurable front-end electronics firmware where possible.