Lattice QCD, Programming Models and Porting LQCD codes to Exascale

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HPC Roundtable
LQCD as an application

- Replace Spacetime with a 4-Dimensional Lattice
LQCD as an application

- Replace Spacetime with a 4-Dimensional Lattice
- Quark fields on the lattice sites: spinors (either complex 3-vectors, or 4x3 “vectors”)
LQCD as an application

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- Strong Force Gauge fields on links: 3x3 complex matrices
• Replace Spacetime with a 4-Dimensional Lattice
• Quark fields on the lattice sites: spinors (either complex 3-vectors, or 4x3 “vectors”)
• Strong Force Gauge fields on links: 3x3 complex matrices
• Interactions are typically local
  - closed loops (3-matrix x 3-matrix)
  - covariant stencils (3-matrix x 3-vector)
• Also lattice wide summations:
  - global sums, inner products etc.
• Extremely well suited to data-parallel approaches
  - complex numbers and factors of 3 are often unfriendly to automatic vectorization - we need to usually build that in.
Typical LQCD Workflow

Configuration Generation
- Hybrid Molecular Dynamics Monte Carlo
- Linear Solves for Fermion Forces
- Data parallel code for non-solver parts
- Strong Scaling Limited
- ‘Large’ long running jobs

Propagators, graph nodes & edges eigenvectors etc.
- Linear Solves for quark propagators on sources
- e.g. \( O(1M) \) solves/config for spectroscopy
- Solver: same matrix, many right hand sides
- Throughput limited
- Ensemble: Many small jobs

Graph Contractions
- \( O(10K) - O(100K) \) diagrams
- sub-diagram reuse challenge
- main operation is batched ZGEMM
- Potential large scale I/O challenge
- Ensemble: Many single node jobs

Correlation Function
Fitting and Analysis
- workstations
• Level structure worked out over last 4 iterations of the SciDAC program
• Data Parallel Layer (QDP) over a communications abstraction layer, presents programmer with a ‘virtual grid machine’
• Applications can be written on top of the Data Parallel Layer, calling out to Highly Optimized Libraries as needed.
• Grid is a new code, also providing a data parallel layer, and similar layering internally (but not broken out into separate packages)
General Software Organization

Key Goals:
- Port Data Parallel Layer,
- Port Libraries,
- Aim for Performance
- Portability

- Apps
- Libraries
- Data Parallel
- Comms

Thomas Jefferson National Accelerator Facility
Exascale & Pre-Exascale Systems

- Perlmutter (formerly NERSC-9)
  - AMD CPUs, NVIDIA Next Gen GPUs.
  - Slingshot fabric from Cray

- Aurora
  - Xeon CPUs + Intel Xe Accelerators
  - Slingshot fabric from Cray

- Frontier
  - AMD CPUs + AMD Radeon GPUs
  - Slingshot fabric from Cray

- MPI + X programming model
- Horsepower for all the systems will come from accelerators
- But the accelerators are different between the 3 systems
## Node Programming Model Options

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<td>Supported</td>
<td>Supported</td>
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<td>Supported</td>
</tr>
<tr>
<td>AMD GPU</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
<td>In development</td>
<td>Supported</td>
</tr>
<tr>
<td>Intel Xe</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
<td>In development</td>
<td>Supported</td>
</tr>
<tr>
<td>CPUs</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
<td>In development</td>
<td>Supported</td>
</tr>
<tr>
<td>Fortran</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
<td>In development</td>
<td>Supported</td>
</tr>
<tr>
<td>FPGAs</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
<td>Supported</td>
<td>In development</td>
<td>Supported</td>
</tr>
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### Comments
- Compilers Maturing, some C++ issues
- DPC++ and HIP back ends in development
- NVIDIA via POCL or Codeplay Backend, AMD via hipSYCL for now, well supported for Intel
- Fortran via cross calling, well supported for AMD GPUs
- The way of the future? parallelism in the base language. Tech previews just now
- Fortran via PGI CUDA Fortran, well supported for NVIDIA GPUs

Disclaimer: this is my current view, products and support levels can change. This picture may become out of date very soon
OpenMP Offload

- Offloaded axpy in OpenMP

```c
#pragma omp target teams distribute parallel for simd
map(to:z[:N]) map(a,x[:N],y[:N])
for(int i=0; i < N; i++) // N is large
{
    z[i] = a*x[i] + b[i];
}
```

- Collapses:
  - omp target - target the accelerator,
  - omp teams - create a league of teams
  - omp distribute - distribute the works amongst the teams
  - omp parallel for simd - perform a SIMD-ized parallel for
  - map a, x and y to the accelerator and map resulting z back out (data movement).
HIP

- HIP is AMD’s “C++ Heterogeneous-Compute Interface for Portability”
- Take your CUDA API and replace ‘cuda’ with ‘hip’:
  - `cudaMemcpy()` -> `hipMemcpy()`
  - `kernel<<<>>>( )` -> `hipLaunchKernelGGL(kernel,...)`
  - and other slight changes.
  - You can use `hipify` tool to do first pass of conversion automatically
- Open Source
- Portability between NVIDIA and AMD GPUs only.
**Kokkos**

Kokkos::View<float[N],LayoutLeft,CudaSpace> x(“x”); // N is large
Kokkos::View<float[N],LayoutLeft,CudaSpace> y(“y”);
Kokkos::View<float[N],LayoutLeft,CudaSpace> z(“z”);

float a=0.5;

Kokkos::parallel_for(“zaxpy”, N, KOKKOS_LAMBDA (const int& i) {
    z(i) = a*x(i) + y(i);  // view provides indexing operator()
});

- View - multi-dimensional array, index order specified by Layout, location by MemorySpace policy. Layout allows appropriate memory access for CPU/GPU
- Parallel for dispatches a C++ lambda
- Kokkos developers on C++ standards committee - work to fold features into C++
Portability via Kokkos

- Kokkos provides portability via back-ends: e.g. OpenMP, CUDA, ...
- Most abstractions are provided in a C++ Header library
  - parallel_for, reduction, scans
- Kokkos provides the Kokkos View data-type
  - user can customize index order
  - explicit memory movement only
  - select memory space via policy
- Bind Execution to Execution Space
  - select back end via policy

Kokkos Abstractions

- CUDA Back-End
- OpenMP Back-End
- HIP Back-End
- SYCL/DPCPP Back-End
- OpenMP target Back-End

Stable and Production ready

In Development
SYCL

- SYCL manages buffers
- Only access buffers via accessors
- Can track accessor use and build data dependency graph to automate data movement
- What does this mean for non SyCL Libraries with pointers? (e.g. MPI)

```cpp
sycl::queue myQueue;
sycl::buffer<float,1> x_buf(LARGE_N);
sycl::buffer<float,1> y_buf(LARGE_N);
sycl::buffer<float,1> z_buf(LARGE_N);

// ... fill buffers somehow ...
float a = 0.5;
{
  myQueue.submit([&](handler& cgh) {
    auto x=x_buf.getAccess<access::mode::read>(cgh);
    auto y=y_buf.getAccess<access::mode::read>(cgh);
    auto z=z_buf.getAccess<access::mode::write>(cgh);

    cgh.parallel_for<class zaxpy>(LARGE_N,[=](id<1> id){
      auto i = id[0];
      z[i]=a*x[i] + y[i];
    });
  });
}
```

SYCL runtime manages data in buffers
access buffer data via accessors in command group (cgh) scope or host accessor

Kernels must have a unique name in C++
Intel OneAPI DPC++ extensions

- USM extension allows management of arrays via pointers (more CUDA-like)
- Memcpy ops to move data between host and device (not shown here)
- Reductions !!
- Unnamed Lambda extension obviates need for a class name for parallel for
- Libraries (e.g. MPI) can do intelligent things with USM pointers (e.g. direct device access)
- Subgroup Extension allows more explicit SIMD-ization

```c++
// Attempt to move data between host and device
sycl::queue myQueue;
sycl::device dev=myQueue.get_device();
sycl::context con=myQueue.get_context();

float* x=sycl::malloc_device(LARGE_N*sizeof(float),dev,con);
float* y=sycl::malloc_device(LARGE_N*sizeof(float),dev,con);
float* z=sycl::malloc_device(LARGE_N*sizeof(float),dev,con);

// ... fill aarrays somehow somehow ...
float a = 0.5;
{
    myQueue.submit([&](handler& cgh) {
        cgh.parallel_for(LARGE_N,[=](id<1> id){
            auto i = id[0];
            z[i]=a*x[i] + y[i];
        });
    });

    // free pointers etc..
```

**USM gives host/device pointers and**

- **Unnamed lambda extension**
  - obviates need for a class name for parallel for
  - Libraries (e.g. MPI) can do intelligent things with USM pointers (e.g. direct device access)
  - Subgroup Extension allows more explicit SIMD-ization
Portability via SYCL

Consistency in implementing standard (?)

Intel LLVM
OneAPI/DPCPP

Codeplay ComputeCPP

SPIR/SPIRV

SPIR/SPIRV

NEW!

Manufacturers all have favorite standards

Intel OpenCL Drivers

POCL Driver

NVIDIA GPU

CUDA driver

AMD GPU

ROCm driver

HD Graphics

FPGA

Xeon Server

Other CPU

HIP

Jefferson Lab
NERSC
NVIDIA
intel
Sandia National Laboratories

ECP

JSA
US LQCD Codes are C++/C

- For C/C++ codes, OpenMP offload, Kokkos/Raja, or DPC++ and SYCL are the most obvious candidates currently. pSTL may become interesting in the near future.

- Performance Portability Experiments:
  - OpenMP Offload: P. Steinbrecher and HotQCD - OpenMP implementation for Intel Gen9
  - Kokkos and SYCL: B. Joo, P3HPC @ SC19
  - Early pSTL experiments by K. Clark

- The lattice developer community is paying attention to DPC++/SYCL, HIP, and OpenMP offload as the porting work to the new machines becomes more urgent.

- I will focus on our local work with the Chroma code and Kokkos and SYCL.
Wilson Dslash in Kokkos and SYCL

- When looking at a new programming model, it helps to have a “simple” mini-app to evaluate whether the model is viable
- We chose the Wilson-Dslash operator as it is
  - sufficiently nontrivial.
  - well understood in terms of performance
  - has many hand optimized implementations, e.g. QPhiX on KNL, QUDA on NVIDIA GPUs
- Initial work in Kokkos looked at vectorization
- More recently we looked at porting to SYCL, and seeing how portable SYCL is

\[
D_{x,y} = \sum_{\mu} \left[ (1 - \gamma_{\mu}) U_{x,\mu} \delta_{x+\mu,y} + (1 + \gamma_{\mu}) U^\dagger_{x-\mu,\mu} \delta_{x-\mu,y} \right]
\]
Basic Performance Bound for Dslash

- \( R \): no of reused input spinors
- \( Br \): read bandwidth
- \( Bw \): write bandwidth
- \( G \): size of Gauge Link matrix (bytes)
- \( S \): size of Spinor (bytes)
- \( r \): 1 (read-for-write), 0 (no read-for-write)
- Simplify: Assume \( Br = Bw = B \)

\[
F = \frac{1320}{8G/Br + (8 - R + r)S/Br + S/Bw}
\]

\[
AI = \frac{1320}{8G + (9 - R + r)S}
\]

Wilson Dslash Arithmetic Intensities (F/B) for 32-bit floating point numbers (G=72B, S=96B)

<table>
<thead>
<tr>
<th>( R )</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>( r=0 )</td>
<td>0.92</td>
<td>0.98</td>
<td>1.06</td>
<td>1.15</td>
<td>1.25</td>
<td>1.38</td>
<td>1.53</td>
<td>1.72</td>
</tr>
<tr>
<td>( r=1 )</td>
<td>0.86</td>
<td>0.92</td>
<td>0.98</td>
<td>1.06</td>
<td>1.15</td>
<td>1.25</td>
<td>1.38</td>
<td>1.53</td>
</tr>
</tbody>
</table>
Vectorizing Dslash for Single RHS

Virtual Node Vectorization (P. Boyle, e.g. in Grid, BFM)

- Treat SIMD lanes like a grid of virtual computing elements (virtual nodes, VNs)
- Lay-out lattice onto VN grid
  - original site -> (‘outer’ site, lane)
- All arithmetic changes to straightforward SIMD arithmetic
- Accessing nearest neighbors
  - on edge of ‘outer lattice’ communicate between ‘virtual nodes’ (lanes).
  - this is a shuffle operations (e.g. _mm512_shuffle_ps in AVX512)
- On GPUs
  - use N=1 (no vectorization) => trivial shuffles.
  - Or use warp/subgroup level SIMD (less portable)
Kokkos Implementation: Kernel

```
template<
type name VN, type name GT, type name ST, type name TGT, type name TST, const int isign, const int target_cb>
struct VDslashFunctor {

VSpinorView<ST,VN> s_in;
VGaugeView<GT,VN> g_in;
VSpinorView<ST,VN> s_out;
SiteTable<VN> neigh_table;

KOKKOS_FORCEINLINE_FUNCTION
void operator() (const int& xcb, const int& y, const int& z, const int& t) const
{
    int site = neigh_table.coords_to_idx(xcb,y,z,t);
    int n_idx;

typename VN::MaskType mask;
SpinorSiteView<TST> res_sum;
HalfSpinorSiteView<TST> proj_res, mult_proj_res;

for(int spin=0; spin < 4; ++spin)
    for(int color=0; color < 3; ++color)
        ComplexZero(res_sum(color,spin));

neigh_table.NeighborTMinus(xcb,y,z,t,n_idx,mask);
KokkosProjectDir3Perm<ST,VN,TST,isign>(s_in, proj_res,n_idx,mask);
mult_adj_u_halfsinor<GT,VN,TST,0>(g_in, proj_res,mult_proj_res,site);
KokkosRecons23Dir3<TST,VN,isign>(mult_proj_res,res_sum);

// Other dirs. (Z-, Y-, X-, X+, Y+, Z+, T+)
#pragma unroll
for(int spin=0; spin < 4; ++spin)
    for(int color=0; color < 3; ++color) {
        Stream(s_out(site,spin,color),res_sum(color,spin));
    }
};
```

operator() gets 4 indices from the multi dimensional range policy

Neighbouring site

Vectorisation Permutation mask: for edges
Kokkos Implementation: Dispatch

template<
typename VN,
typename GT,
typename ST,
typename TGT,
typename TST>
class KokkosVDslash {
public:
        const LatticeInfo& _info;
    SiteTable<VN> _neigh_table;

    KokkosVDslash(const LatticeInfo& info) : _info(info),
        _neigh_table(info.GetCBLatticeDimensions()[0], info.GetCBLatticeDimensions()[1], info.GetCBLatticeDimensions()[2], info.GetCBLatticeDimensions()[3]) {}

    void operator()(const KokkosCBFineVSpinor<ST,VN,4>& fine_in,
        KokkosCBGoldenVSpinor<ST,VN,4>& fine_out,
        int plus_minus,
        const IndexArray& blocks) const
    {
        int source_cb = fine_in.GetCB();
        int target_cb = (source_cb == EVEN) ? ODD : EVEN;

        const VSpinorView<ST,VN>& s_in = fine_in.GetData();
        const VGaugeView<GT,VN>& g_in = gauge_in.GetData();
        VSpinorView<ST,VN>& s_out = fine_out.GetData();

        IndexArray cb_latdims = _info.GetCBLatticeDimensions();

        MDPolicy policy({0,0,0,0}, {cb_latdims[0], cb_latdims[1], cb_latdims[2], cb_latdims[3]}, {blocks[0], blocks[1], blocks[2], blocks[3]});

        if( plus_minus == 1 ) {
            if (target_cb == 0 ) {
                VDslashFunctor<VN,GT,ST,TGT,TST,1,0> f = {s_in, g_in, s_out, _neigh_table}; // Instantiate functor: set fields
                Kokkos::parallel_for(policy, f); // Dispatch
            } else {
            } //Dispatch
        } else {
        }
    }
};

4D Blocked Lattice Traversal Dispatch
template<typename VN, typename GT, typename ST, int dir, int cb>

class dslash_loop;  // Just to give SyCL Kernel a name; Yuck!

template<typename VN, typename GT, typename ST>

class SyCLVDslash {
    const LatticeInfo& _info;
    SiteTable _neigh_table;

    public:
        SyCLVDslash(const LatticeInfo& info) : _info(info),
        _neigh_table(info.GetCBLatticeDimensions()[0],info.GetCBLatticeDimensions()[1],info.GetCBLatticeDimensions()[2],info.GetCBLatticeDimensions()[3]) {} 

        void operator() (const SyCLBFineVSpinor<ST, VN, 4>& fine_in,
        const SyCLCBFineVGaugeFieldDoubleCopy<GT, VN>& gauge_in,
        SyCLBFineVSpinor<ST, VN, 4>& fine_out,
        int plus_minus) {

            int source_cb = fine_in.GetCB();
            int target_cb = (source_cb == EVEN) ? ODD : EVEN;
            SyCLVSpinorView<ST, VN> s_in = fine_in.GetData();
            SyCLVGaugeView<GT, VN> g_in = gauge_in.GetData();
            SyCLVSpinorView<ST, VN> s_out = fine_out.GetData();
            IndexArray cb_latdims = _info.GetCBLatticeDimensions();
            int num_sites = fine_in.GetInfo().GetNumCBSites();

            cl::sycl::queue q;
            if (plus_minus == 1) {   
                q.submit([&](cl::sycl::handler& cgh) {
                    V D s l a s h F u n c t o r < V N , G T , S T ,
                    1, 0> f{
                        s_in.template get_access<cl::sycl::access::mode::read>(cgh),
                        g_in.template get_access<cl::sycl::access::mode::read>(cgh),
                        s_out.template get_access<cl::sycl::access::mode::write>(cgh),
                        _neigh_table.template get_access<cl::sycl::access::mode::read>(cgh)
                    };
                    cgh.parallel_for<dslash_loop<VN, GT, ST, 1, 0>>(cl::sycl::range<1>(num_sites), f);
                });
            } else {
            }
        }
    }
};
template<typename VN, typename GT, typename ST, int dir, int cb> class dslash_loop;   // Just to give SyCL Kernel a name; Yuck!

class SyCLVDslash{
    const LatticeInfo& _info;
    SiteTable _neigh_table;

public:
    SyCLVDslash(const LatticeInfo& info) : _info(info), _neigh_table(info.GetCBLatticeDimensions()[0], info.GetCBLatticeDimensions()[1], info.GetCBLatticeDimensions()[2], info.GetCBLatticeDimensions()[3]) {}  

    void operator() (const SyCLCBFineVSpinor<ST,VN,4>& fine_in, const SyCLCBFineVGaugeFieldDoubleCopy<GT,VN>& gauge_in, SyCLCBFineVSpinor<ST,VN,4>& fine_out, int plus_minus) {

        int source_cb = fine_in.GetCB(); int target_cb = (source_cb == EVEN) ? ODD : EVEN;

        SyCLVSpinorView<ST,VN> s_in = fine_in.GetData();
        SyCLVGaugeView<GT,VN> g_in = gauge_in.GetData();
        SyCLVSpinorView<ST,VN> s_out = fine_out.GetData();

        int num_sites = fine_in.GetInfo().GetNumCBSites();
        cl::sycl::queue q;

        if (plus_minus == 1) {
            if (target_cb == 0) {
                q.submit([&](cl::sycl::handler& cgh) {
                    V D s l a s h F u n c t o r < V N , G T , S T , 1 , 0 > f{
                        s_in.template get_access<cl::sycl::access::mode::read>(cgh),
                        g_in.template get_access<cl::sycl::access::mode::read>(cgh),
                        s_out.template get_access<cl::sycl::access::mode::write>(cgh),
                        _neigh_table.template get_access<cl::sycl::access::mode::read>(cgh)
                    };  
                    cgh.parallel_for<dslash_loop<VN,GT,ST,1,0>>(cl::sycl::range<1>(num_sites), f);
                });
            } else {

            }
        } else {

        }
    }
};
We measured the performance of Kokkos & SYCL Dslash kernels on:

- Volta V100 GPUs using Cori GPU system at NERSC
- Skylake CPUs (single socket) using the CPUs on Cori GPU system at NERSC
- KNL Systems using Jefferson Lab 18p cluster nodes
- Gen9 GPU using an Intel NUC System

Performance ‘Standard Candles’

- On GPU: Dslash from QUDA Library, with equivalent compression/precision options
- On CPU/KNL: Dslash from QPhiX Library with equivalent compression/precision options

To use SYCL on KNL and GPUs we used POCL v1.8: http://portablecl.org/
• Gen-9 GPU in a NUC (max DRAM bandwidth ~ 38 GB/sec, lattice had $32^4$ sites

• Used Codeplay Community Edition (1.0.4 Ubuntu) and Intel Public LLVM-based SYCL Compiler (version in the paper).

• Fortran like complex: (RIRIRI...), Vector Like complex: (RRRR...III...).
  - since V=1 these are the same layout but different operations

• Best performance: sustain 32-36 GB/sec, ~45 GFLOPS => AI ~ 1.25 => R=4-5.
Combined Single RHS Results

- Kokkos using the virtual node SIMD with a ‘Vector Type’ seems to work well
  - ‘Vectype’ is AVX512 or our complex type based on float2
  - Kokkos::complex with ‘alignas’ keyword works as well as float2
- SYCL + POCL did well on GPUs (had linear lattice traversal, if we implemented 4D it may be on par with Kokkos & QUDA - future work)
- Kokkos without Vectype did not do well on KNL - we anticipate the compiler doesn’t do well with SIMD-izing complex operations(?)

![Performance / GFLOPS graph]

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<tr>
<th>Platform</th>
<th>Method</th>
<th>Performance / GFLOPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V100</td>
<td>QUDA</td>
<td>1216</td>
</tr>
<tr>
<td></td>
<td>SYCL + POCL</td>
<td>1114</td>
</tr>
<tr>
<td></td>
<td>Kokkos + Virt. Node + Vectype</td>
<td>1189</td>
</tr>
<tr>
<td>K80</td>
<td>QUDA</td>
<td>222</td>
</tr>
<tr>
<td></td>
<td>SYCL + POCL</td>
<td>179</td>
</tr>
<tr>
<td></td>
<td>Kokkos + Virt. Node + Vectype</td>
<td>211</td>
</tr>
<tr>
<td>KNL</td>
<td>QPhiX</td>
<td>435</td>
</tr>
<tr>
<td></td>
<td>SYCL (V=16) + POCL</td>
<td>56</td>
</tr>
<tr>
<td></td>
<td>Kokkos + Virt. Node + Vectype</td>
<td>416</td>
</tr>
<tr>
<td></td>
<td>Kokkos + Virt. Node</td>
<td>49</td>
</tr>
<tr>
<td>SKX</td>
<td>QPhiX</td>
<td>170</td>
</tr>
<tr>
<td></td>
<td>SYCL (V=16) + Intel Experimental OCL</td>
<td>136</td>
</tr>
<tr>
<td></td>
<td>SYCL (V=1) + Intel Experimental OCL</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>Kokkos + Virt Node + Vectype</td>
<td>160</td>
</tr>
</tbody>
</table>
LLVM: The Swiss Army Knife

- LLVM is compiler technology which underlies the implementations of current programming models:
  - Intel DPC++, HIPCC/HCC, NVCC, …
- Key concepts are
  - a front end: e.g. Clang for C++
  - an intermediate representation (IR)
  - back ends: NVPTX, AMDGPU, X86, Power, Arm etc.
- LLVM also includes Just-In-Time Compilers
  - compile functions/kernels at run-time
  - powering high level languages like Julia
- LLVM can be used to write portable and efficient Domain Specific Languages (DSLs).
QDP-JIT, QDP++ as a DSL

- QDP-JIT developed by F. Winter at JLab allowed us to move all of the QDP++ data parallel layer to GPUs.
  - Expression Templates (ET) generated CUDA PTX kernels
  - PTX Kernels were launched by CUDA driver
  - Automated Memory movement between host/device (via software cache)
  - Provided data layout flexibility
- Later, PTX generation moved to LLVM libraries
  - Turns QDP-JIT into a DSL for QCD
- CPU version was developed to target x86/KNL
  - No ‘driver’, LLVM JIT-ed to objects (LLVM Modules)
  - Vector friendly layout was supported (including matching QPhiX)
- Reduced Amdahl’s law by accelerating the whole application, rather than just a library

QDP-JIT via LLVM for AMD & Intel Xe?

NVIDIA GPU Approach

\[ \text{tmp3} = u[nu] \times \text{tmp}; \]

**Build Function:**
LLVM IR Builder

- **libdevice.bc**
  - NVVM
  - Math functions

- **CUfunction**

- **CUDA DriverAPI**
  - cuLaunchKernel()

- **Execute!**

AMD GPU Approach

\[ \text{tmp3} = u[nu] \times \text{tmp}; \]

**Build Function:**
LLVM IR Builder

- **libocml.bc**
  - OCML
  - Math functions

- **LLVM IR/Module?/SPIRV?**

- **ROCk/HIP kernel launch?/OpenCL driver, dlopen()?**

- **Execute!**

Preliminary discussions about this with Frontier COE

Intel Xe approach?

\[ \text{tmp3} = u[nu] \times \text{tmp}; \]

**Build Function:**
LLVM IR Builder

- **LLVM IR \rightarrow SPIRV**

- **Intel Graphics driver (OpenCL?)**

- **Execute!**

We need to work with Intel more on this

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Conclusions & Future Work

- Both Kokkos and SYCL were sufficiently expressive for Dslash (parallel_for)
- Kokkos Dslash performed on par with QUDA on NVIDIA GPUs, and QPhiX on KNL (with SIMD type)
- SYCL performance depends a lot on the combination of compiler and driver
- LLVM is universal and allows constructing DSLs such as QDP-JIT
  - Ports of QDP-JIT will likely have different branches for each architecture (different dispatch, etc)
- Libraries are also being ported (not discussed here)
- Ongoing / Future work with Kokkos and SYCL
  - Warp/Subgroup level SIMD - in progress using Intel’s SYCL Subgroup-ND range extension
  - Targeting AMD - in progress using new Kokkos HIP Back End, now looking at performance
  - Trying out the Kokkos SYCL/DPC++ back end and OpenMP offload back-ends as they develop
  - Evaluate using Kokkos to implement QDP++
  - Considering multi-node device aspects (communication)
- Lots of ongoing work by the LQCD Software Community on porting codes to ECP systems
References

- KokkosDslash MiniApp:
  - Repo: https://github.com/bjoo/KokkosDslash.git
  - Workspace repo (with dependencies): https://github.com/bjoo/KokkosDslashWorkspace.git

- SyCLDslash MiniApp:
  - Repo: https://github.com/bjoo/SyCLDslash.git
  - Workspace repo (with dependencies): https://github.com/bjoo/SyCLDslashWorkspace.git

- Remember to clone with ‘—recursive’ !!!

- Intel Publicly available SyCL Compiler: https://github.com/intel/llvm
  - sycl branch

- Kokkos: https://github.com/kokkos

- SyCL: https://www.khronos.org/sycl/

- CodePlay Compiler: https://www.codeplay.com/products/computesuite/computecpp


- Subgroup SIMD extension: https://github.com/intel/llvm/blob/sycl/sycl/doc/extensions/SubGroupNDRange/SubGroupNDRange.md


- QPhiX: https://github.com/jeffersonlab/qphix
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