SBS Collaboration Meeting

TDIS Streaming Readout Prototype

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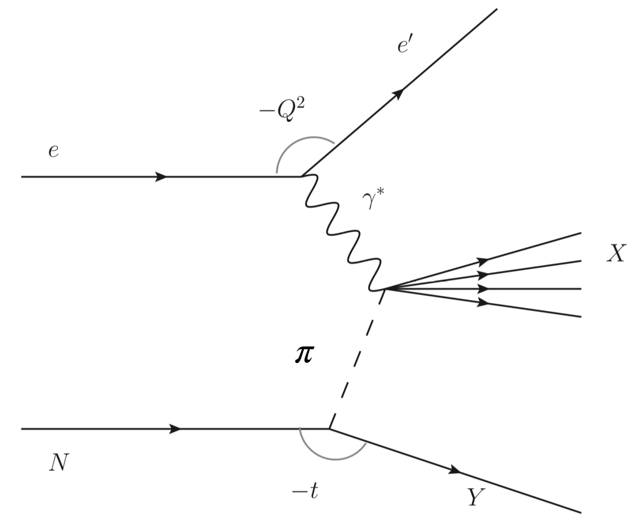
On Behalf of the TDIS SRO Working Group

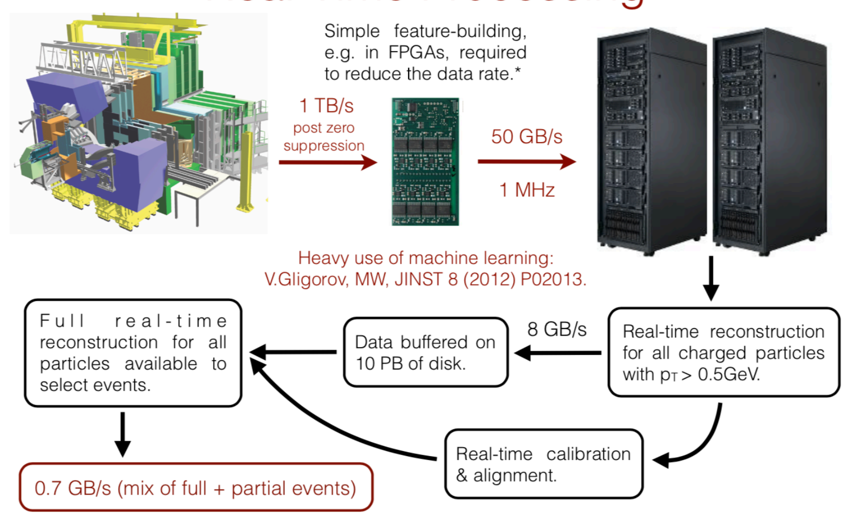
TDIS Streaming Readout Prototype

- TDIS ≡ Tagged Deep Inelastic Scattering
  - Hall-A, Super Big-Bite (SBS)
  - Measure high W^2, Q^2 electron-meson scattering events
  - A GEM based radial time projection chamber (TPC) will facilitate the detection of low momentum spectators
- ALICE collaboration (CERN) is currently upgrading their TPC with a GEM based detection system that is read out continuously
  - Streaming readout (SRO)
  - Continuous time ordered sequences of detector system readout
  - ~1 TB/s post zero-suppression
- Novel front-end ASIC was developed specifically for this purpose ➢ SAMPA
- We are interested in exploring how experiments at JLab can take advantage of this technology as well as the SRO concept
  - SRO Grand Challenge



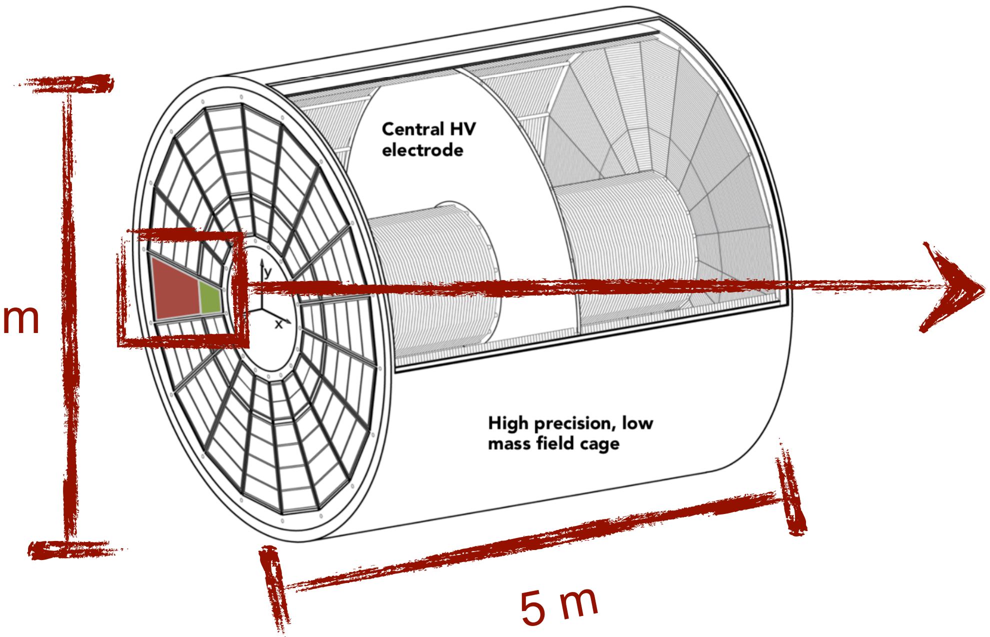
JINST 8 (2013) P04022

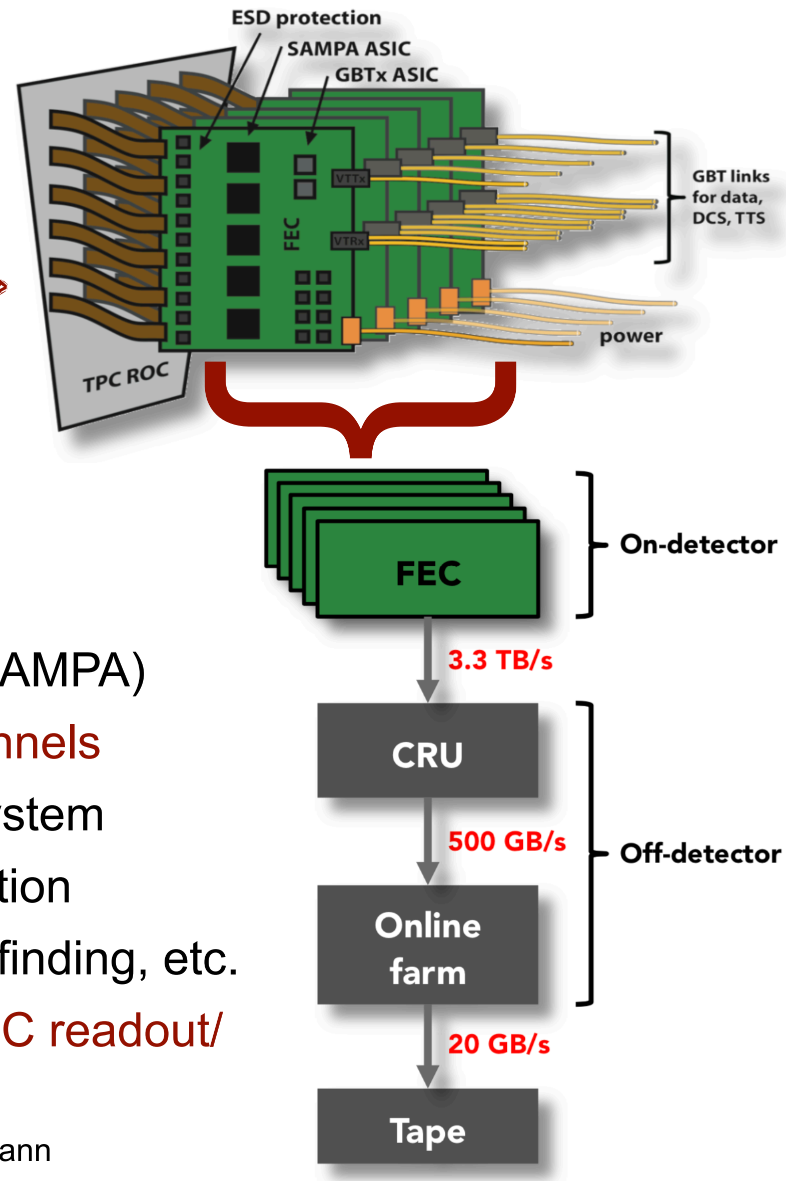
Real-Time Processing



*LHCb will move to a triggerless-readout system for LHC Run 3 (2021-2023), and process 5 TB/s in real time on the CPU farm.

ALICE TPC SRO Strategy



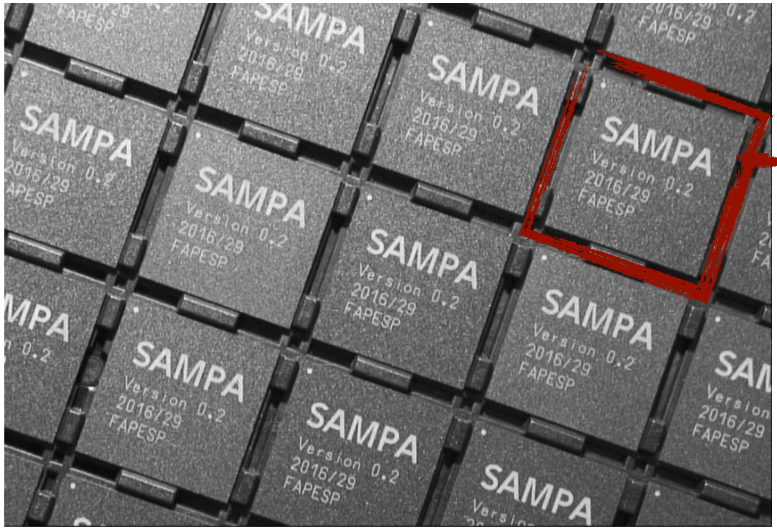


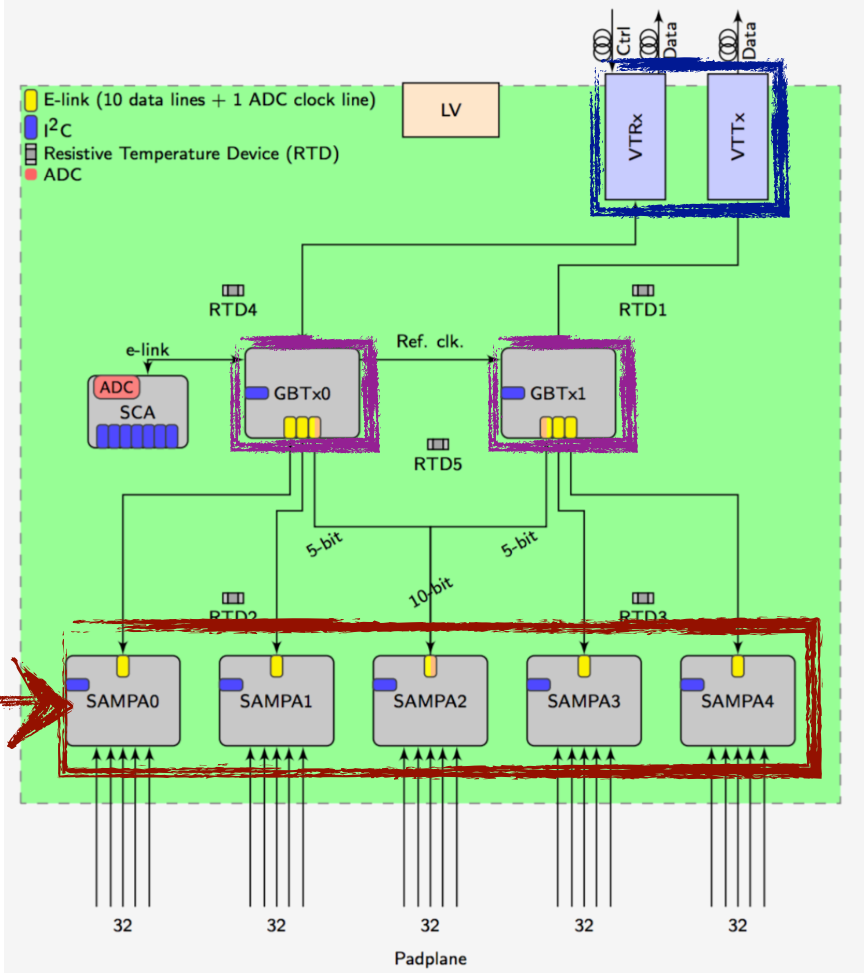
- Continuously readout all TPC ADC channels (via SAMPA)
  - ALICE : 10k FEC’s ➛ 50k chips ➛ ~1.6M channels
- Radiation hard CERN Gigabit transceiver (GBT) system
- Common readout unit (CRU) ➛ Online data correction
  - PCIe platform ➛ Baseline corrections, cluster finding, etc.
- TDIS SRO prototype is utilizing as many ALICE TPC readout/ control chain components as possible

Slide Adapted From C. Lippmann

ALICE SRO Electronics

- SAMPA : University of São Paulo, Brazil
- Supports both continuous and triggered readout modes
- Digital signal processor (can be bypassed)
- Single ALICE front end card (FEC) supports 5 SAMPA chips (160 channels)
- Serialized data are routed via e-links into 2 GBTx chips which drive fiber transmitters (VTTx & VTRx) at 3.2 Gb/s each

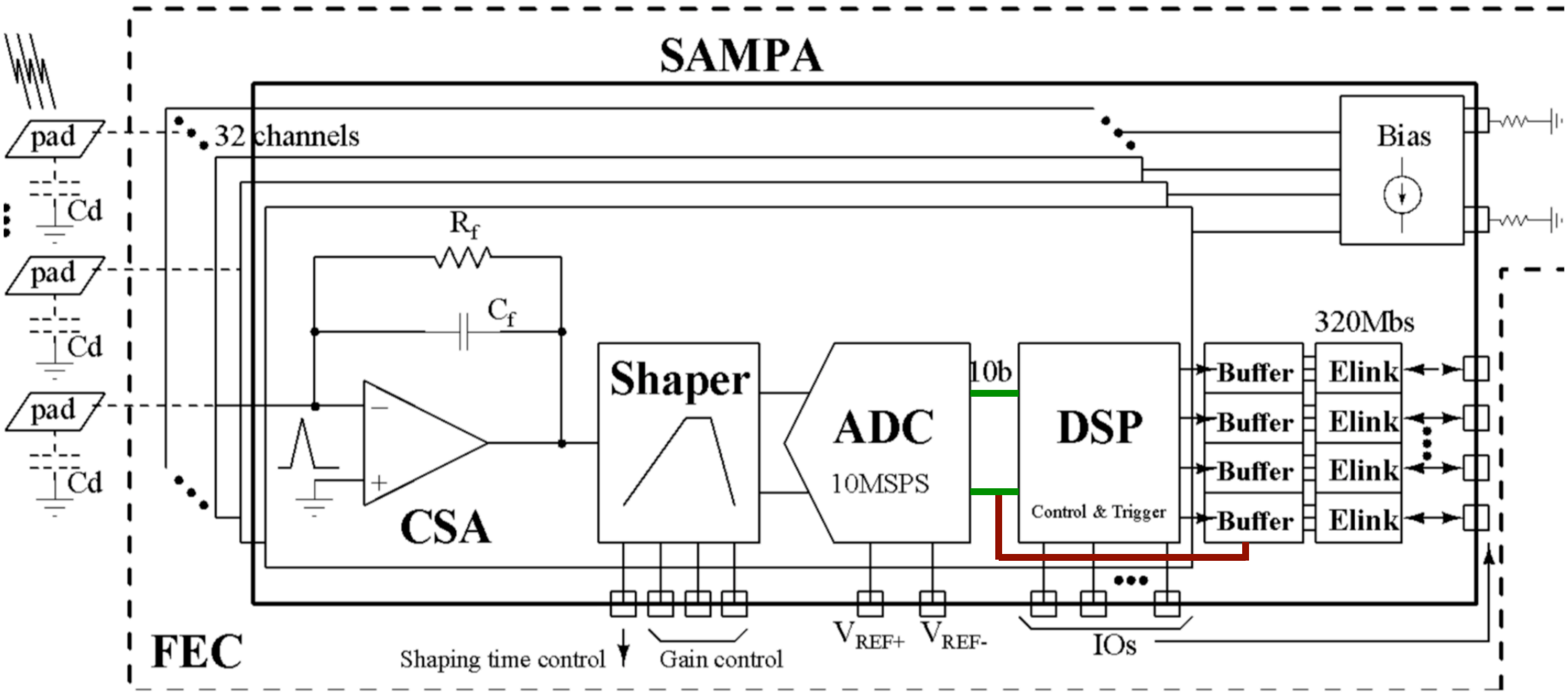




Slide Adapted From C. Lippmann

SAMPA Operational Modes

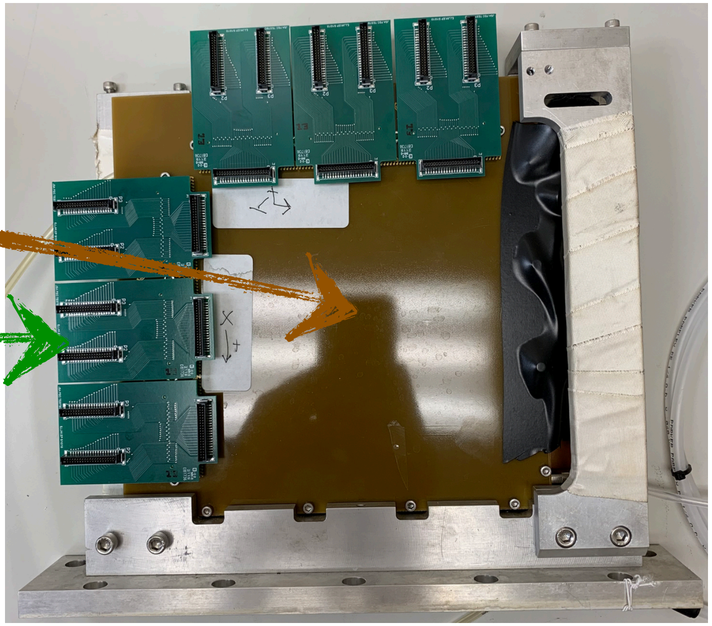
- Direct ADC serialization (DAS) mode ➛ bypass digital signal processor (DSP)
  - ALICE FEC design limits ADC rate to 5 MHz in DAS mode ➛ 10 e-links (max 3.2 Gb/s)
- DSP mode ➛ pedestal subtraction, baseline corrections, zero-suppression, compression
  - Sampling rates of 10 or 20 MHz ➛ 11 e-links (max 3.2 Gb/s or 6.4 Gb/s)



Slide Courtesy of E. Jastrzembski

TDIS SRO Prototype

- INDRA-ASTRA Facility (CC F110)
- Variety of hardware present so that it is "streaming capable"
  - User programmable network switch with 100 Gb/s data link
  - Fast multi-core server machine with 100 Gb/s data link
  - Fast PC's with several PCIe slots for testing high speed data links, FPGAs, GPU's, etc.
- Triple-GEM detector provides 768 channels of analog data
- Custom transition card fabricated to facilitate ALICE FEC inputs
- 800 channels of SAMPA readout (5 FEC's, 25 SAMPA chips) via ALICE SRO system



TDIS SRO Prototype

- We are able to stream trigger-less GEM data (768 channels) in DAS mode at 45 Gb/s via 5 ALICE FEC's
  - GEM ➛ FEC ➛ TRORC (30 Gb/s) ➛ PC Memory ➛ Disk
- We are able to stream triggered GEM data in DSP mode where a global readout threshold is applied and a programmable window of streamed data is captured by the T-RORC
  - Keeps the data volume to memory (and to disk) at a manageable level
- Will modify the T-RORC firmware to suppress the transmission of unnecessary sync packet data to memory and disk
  - Sync packets keep the serial links from the SAMPAs active when there is no hit data to send
- Then we can acquire data in a truly continuous fashion

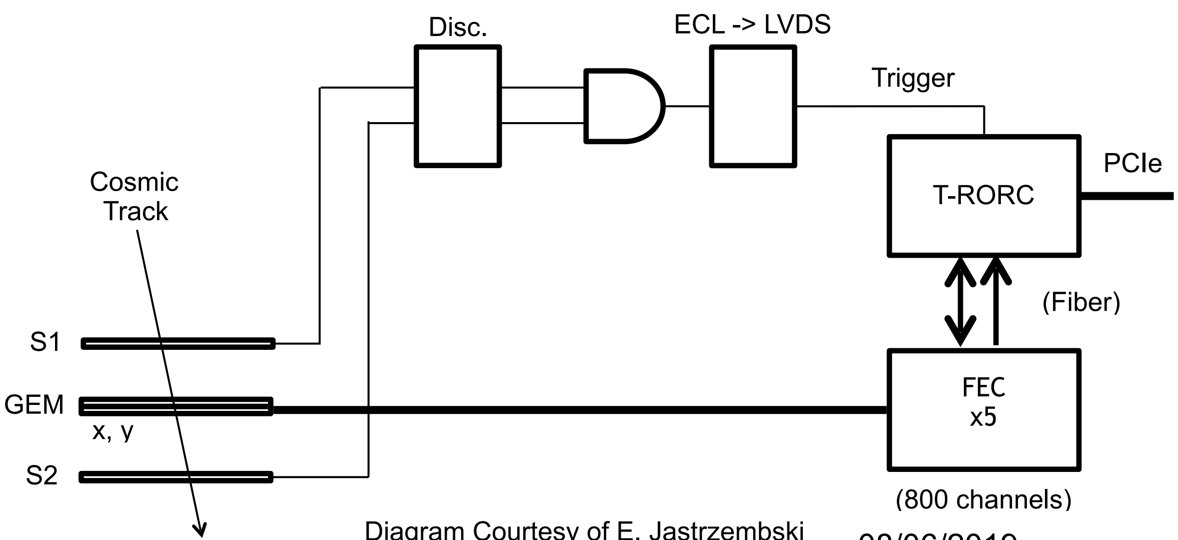
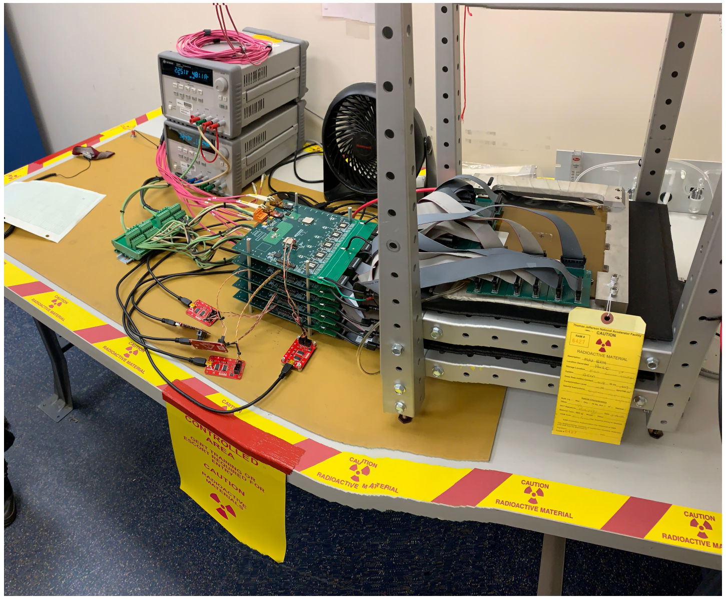
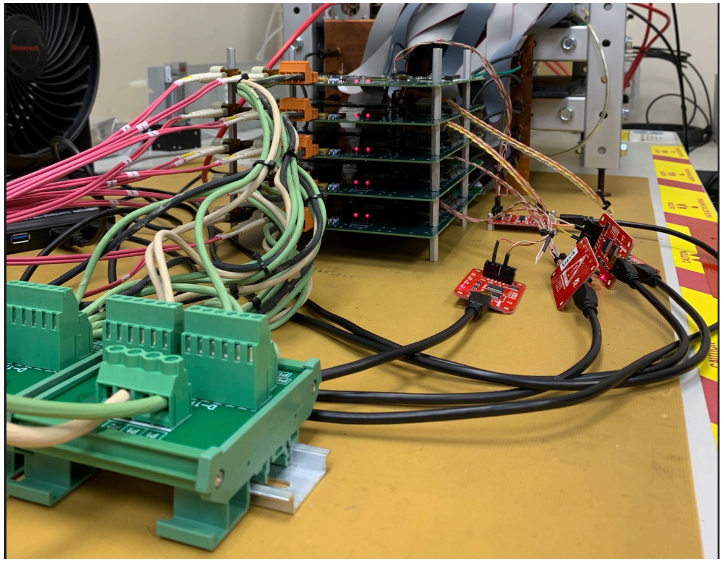


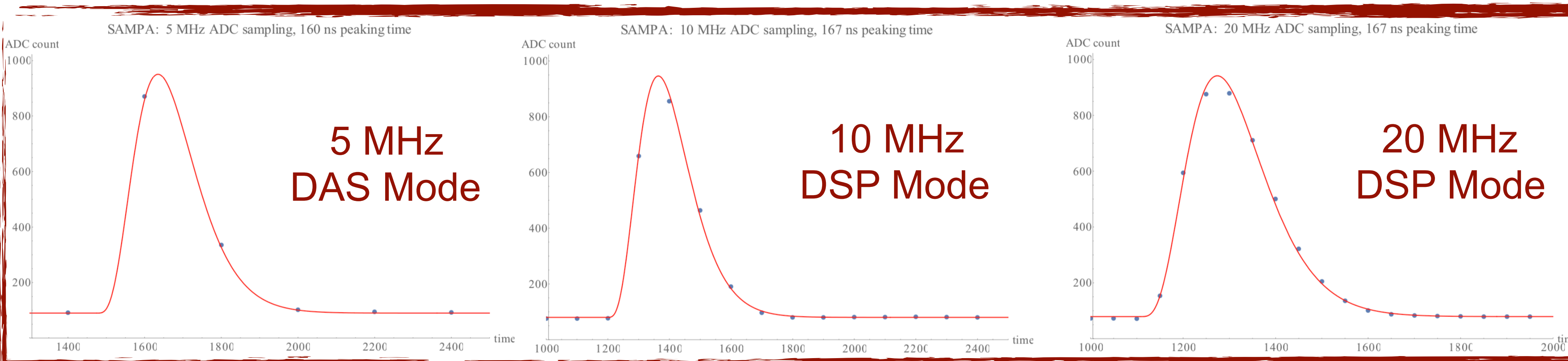
Diagram Courtesy of E. Jastrzembski

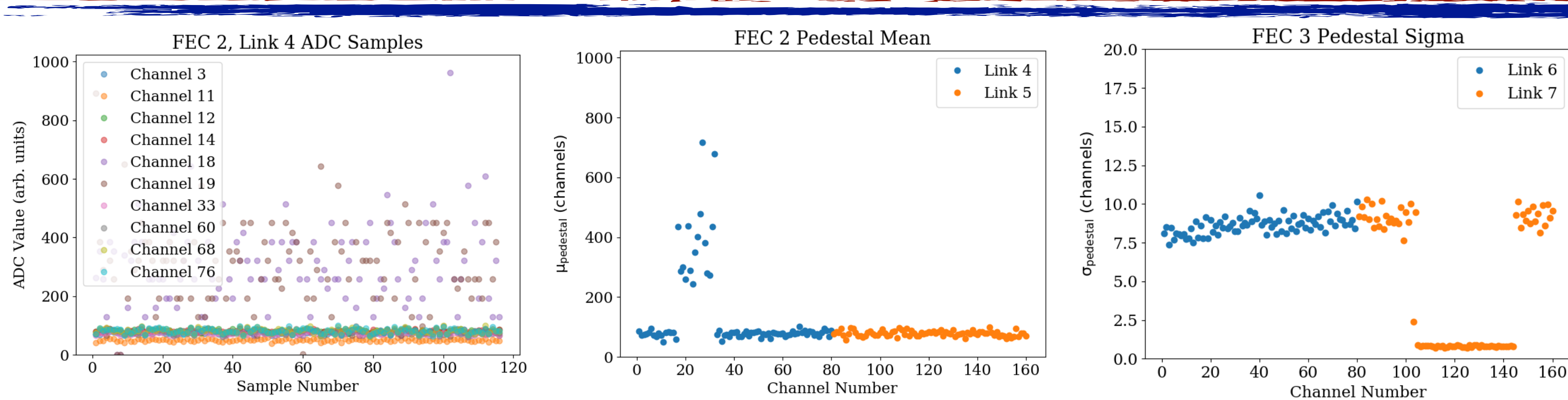




TDIS SRO SAMPA Data

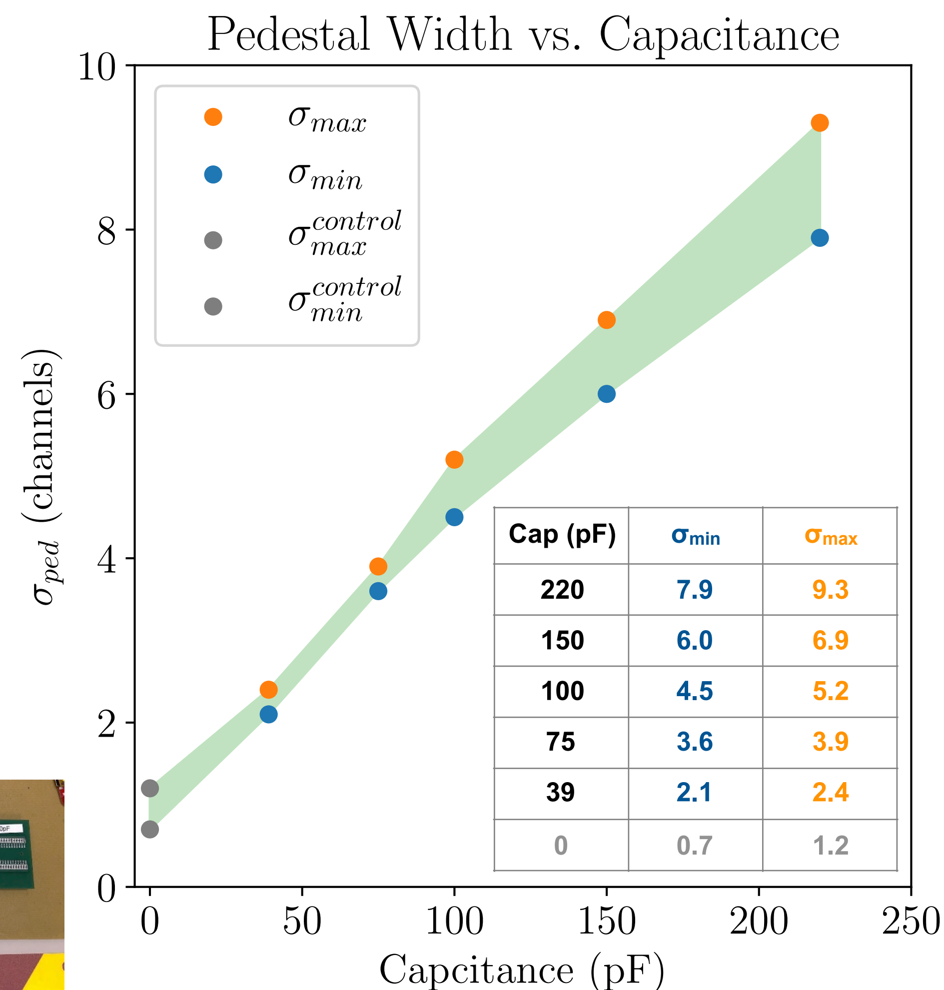
- Variety of ways to analyze/monitor the data are actively being developed
- SAMPA response to test pulse ➛ 5 MHz, 10 MHz, and 20 MHz
- TDIS SRO GEM data ➛ 5 MHz DAS mode ➛ sample, μ_{ped}, and σ_{ped} data



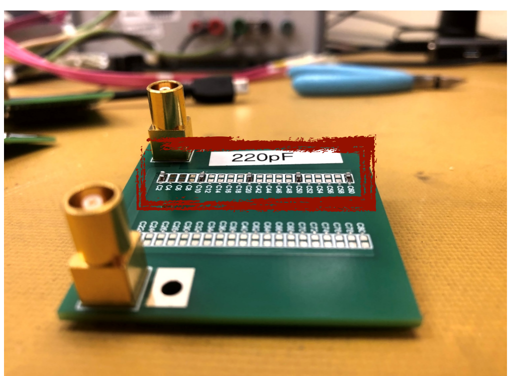


SAMPA Capacitance Study

- Capacitance studies were performed to measure the noise of the SAMPA type front end architecture (CSA + shaper)
- The aim of the study was to quantify the noise vs. capacitance curve and illustrate that the noise does in fact increases linearly with detector capacitance
- Five input channels were configured with varying capacitances (0 - 220 pF) while the remaining 35 channels were not modified
- The min and max sigmas of the pedestal distributions of the five channels configured with "detector capacitance" are shown
- A clear linear dependence was observed

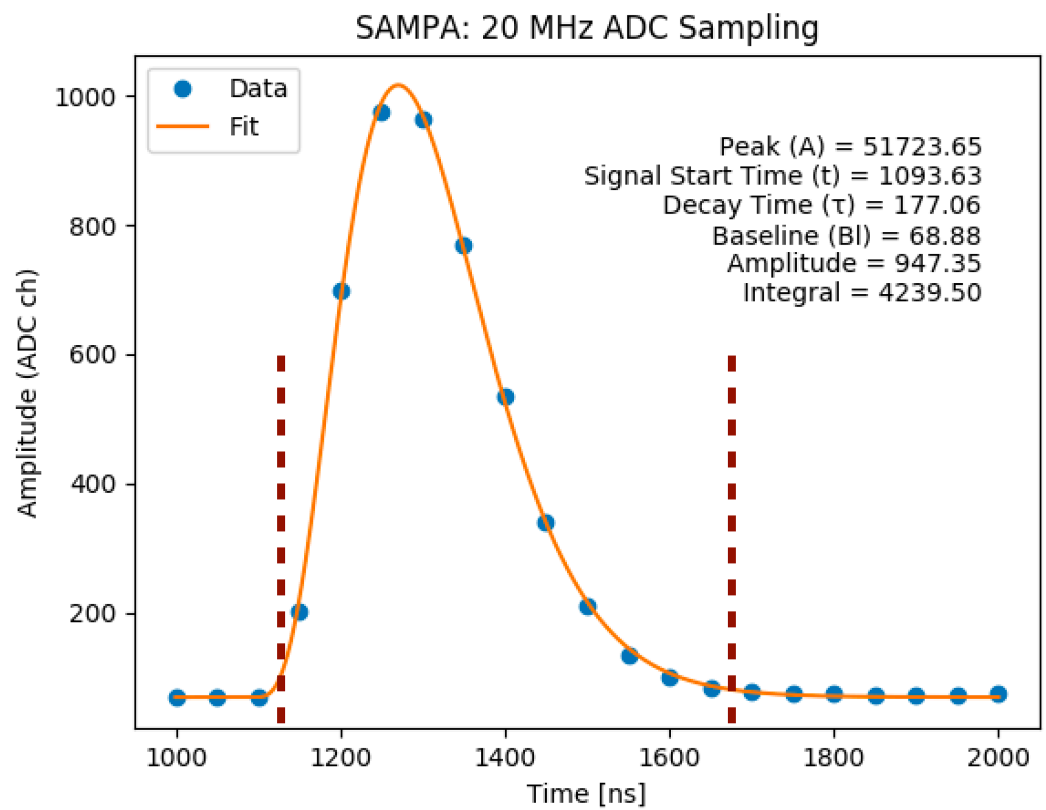


Cap (pF)	σ_{min}	σ_{max}
220	7.9	9.3
150	6.0	6.9
100	4.5	5.2
75	3.6	3.9
39	2.1	2.4
0	0.7	1.2



SAMPA Response & Pulse Fitting

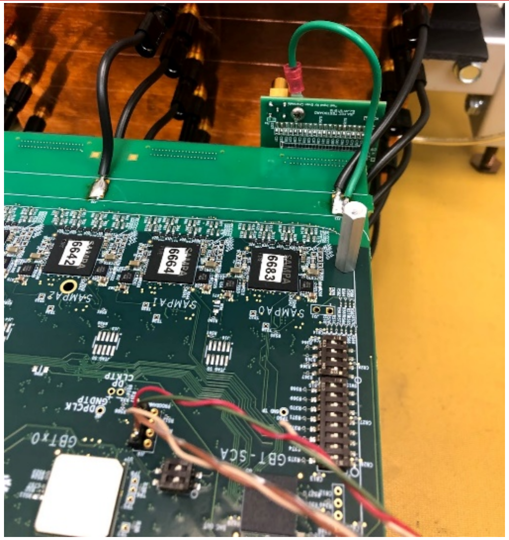
- A charge of 80 fC was injected into the SAMPA input via an injector card over a 2.5 ns period via a pulse generator ➣ fast negative 80 mV step on a 1 pF capacitor connected to the input
- Data was continuously streamed (no trigger required) and sampled at 20 MHz with the DSP configured to zero-suppression mode with a threshold set slightly above the base line
- The packetized data includes 3 pre-samples and 7 post-samples relative to the threshold crossing
- Feature extractions are obtained via fitting the sample data with a semi-Gaussian of $\mathcal{O}(4)$ ➣ start-time, decay time, baseline, amplitude
- The integral is extracted from summing the samples above threshold and subtracting an averaged base line from pre and post samples



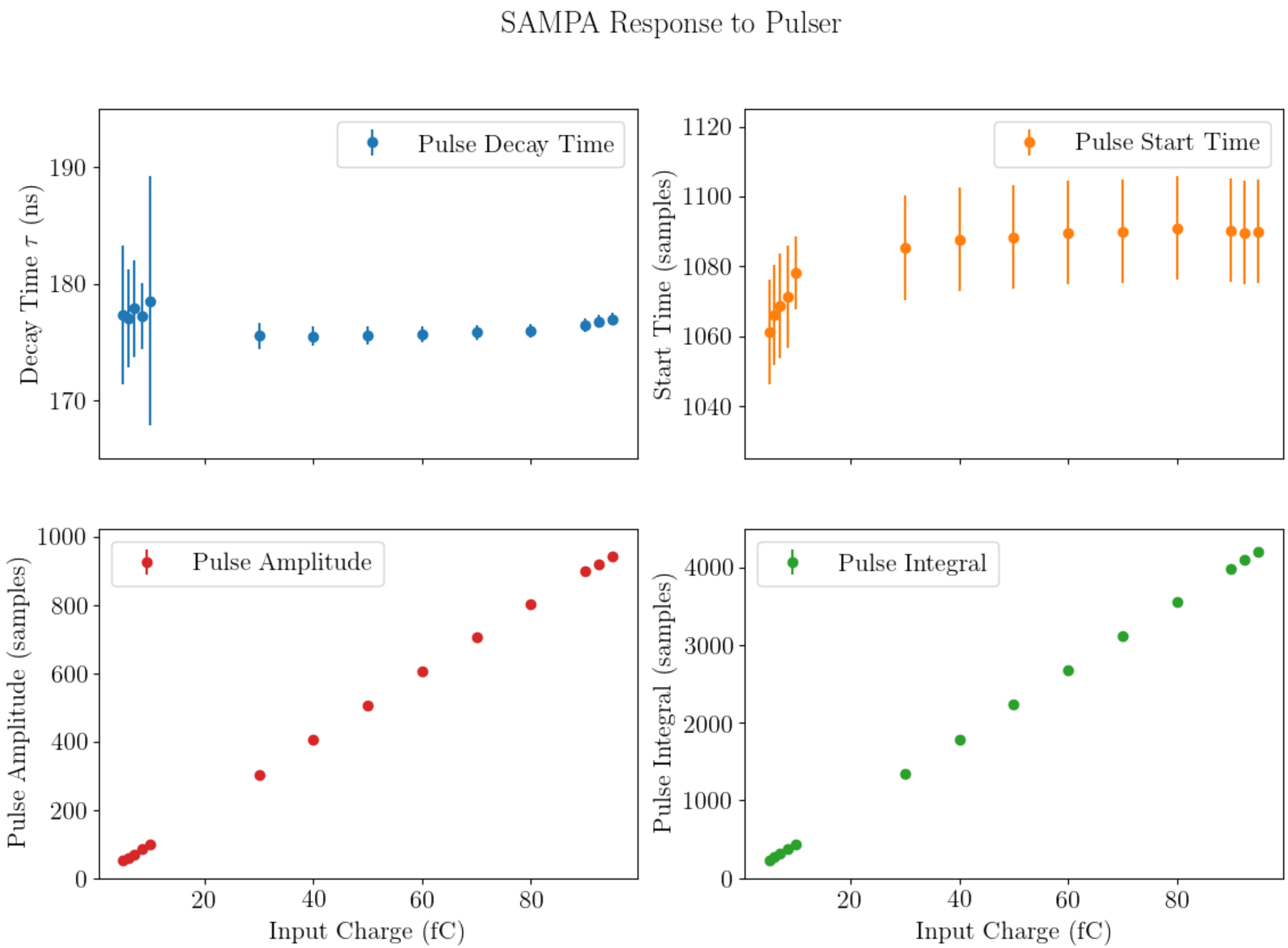
$$f(x) = A\left(\frac{x-t}{\tau}\right)^4 e^{-4\left(\frac{x-t}{\tau}\right)} + B_l$$

SAMPA Linearity Test

- Pulses of constant amplitude were injected into a single FEC input (40 SAMPA channels)
- 20 kHz step signal AC coupled to a 1 pF cap over a 2.5 ns period ➛ ≈ 167 ns decay time
- 5 ms of DSP zero-suppressed data (20 MHz sampling) were streamed from one FEC (2 optical links) and written to directly disk
- 100 pulses of known charge were captured within 50 μs (1000 samples) windows
- The ADC samples were analyzed and fits were applied to the data
- Pulse features were extracted and averaged for each input charge setting (14 settings in total)
- The aim was to verify the linearity of the SAMPA response to pulses populating the full dynamic range of the 10-bit ADCs (1024 samples)

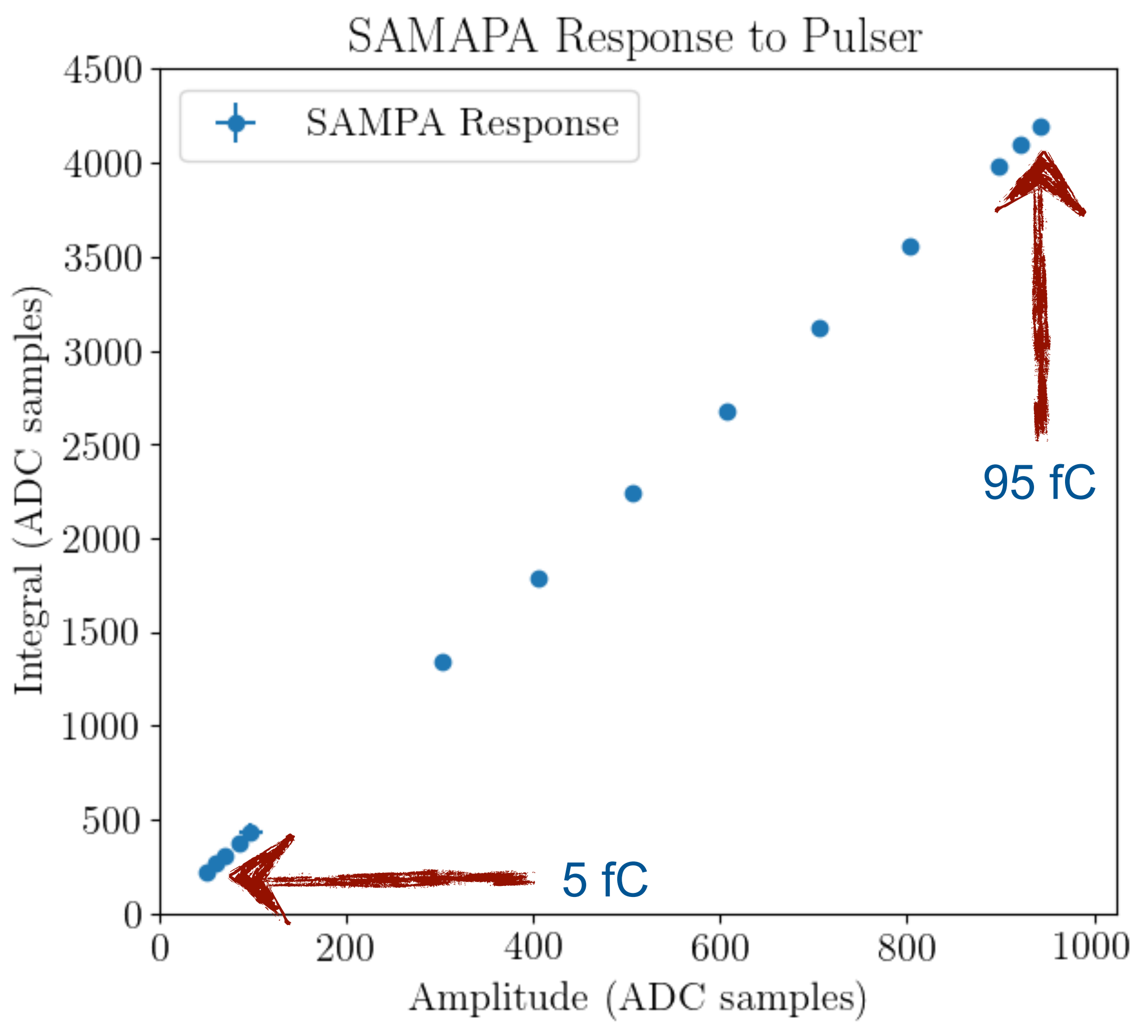


SAMPA Linearity Test



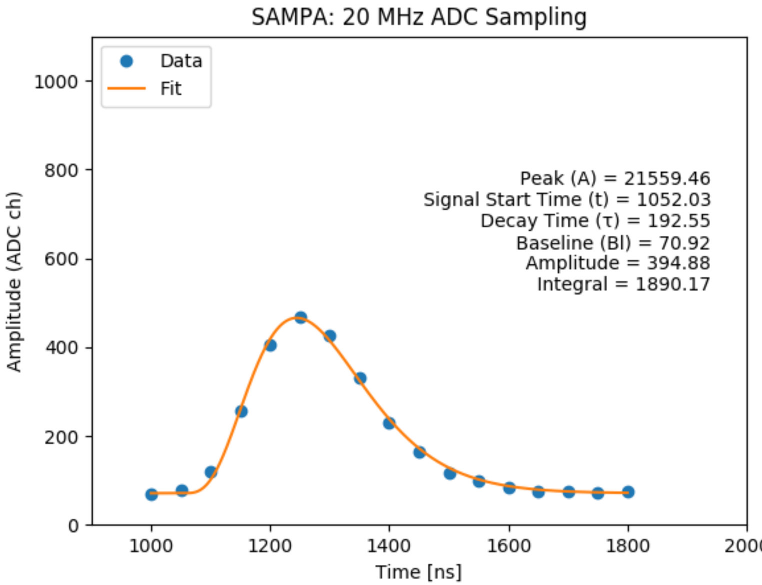
SAMPA Linearity Test

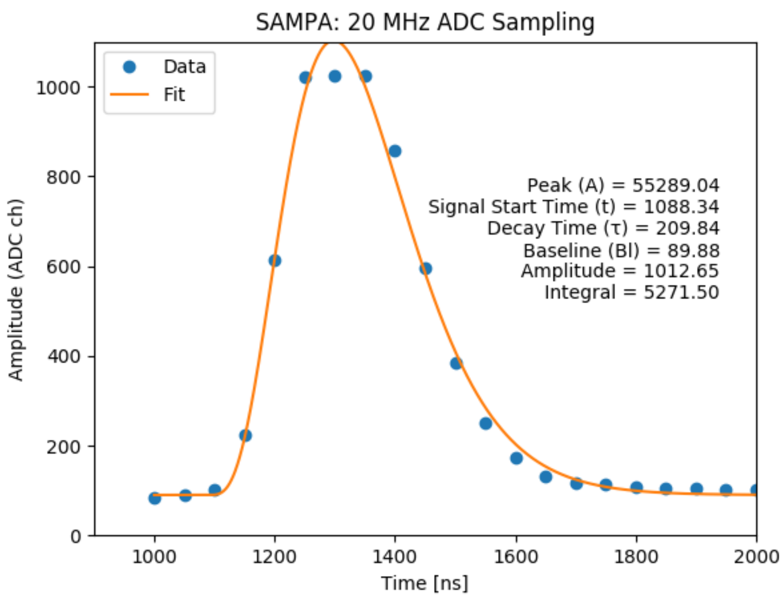
- The waveform amplitude and integral of samples vary linearly with input charge

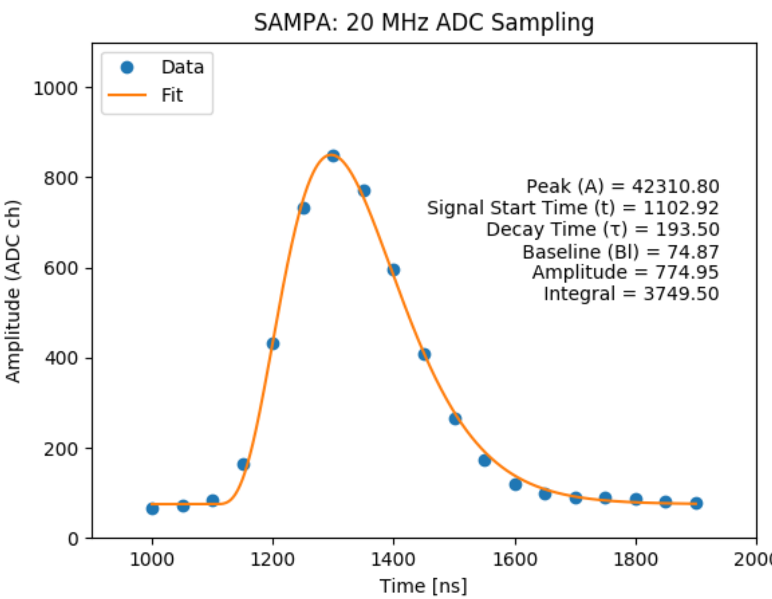


SAMPA Response to Cosmic GEM Data

- Cosmic NIM triggers from two scintillator paddles above and below the GEM are converted to LVDS
- The SAMPA chips are configured to operate in DSP zero-suppression mode with a common threshold applied to all channels ➛ 125 ADC channels
- The LVDS signal triggers the TRORC to capture 50 μs of data streaming from 5 ALICE FECs at 45 Gb/s and write it to disk
- 100 cosmic triggers (≈ 5 min) were collected illustrating that we can continuously stream data from all 768 GEM strips and obtain feature extraction on real pulses

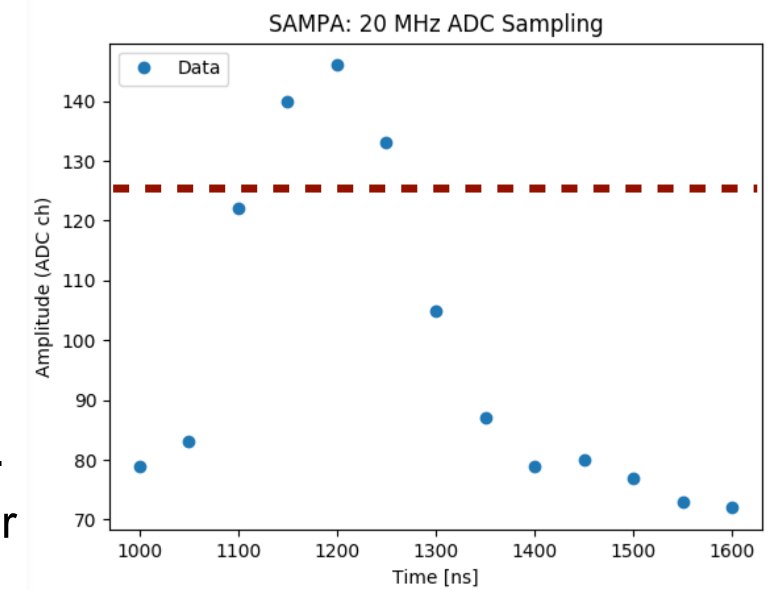


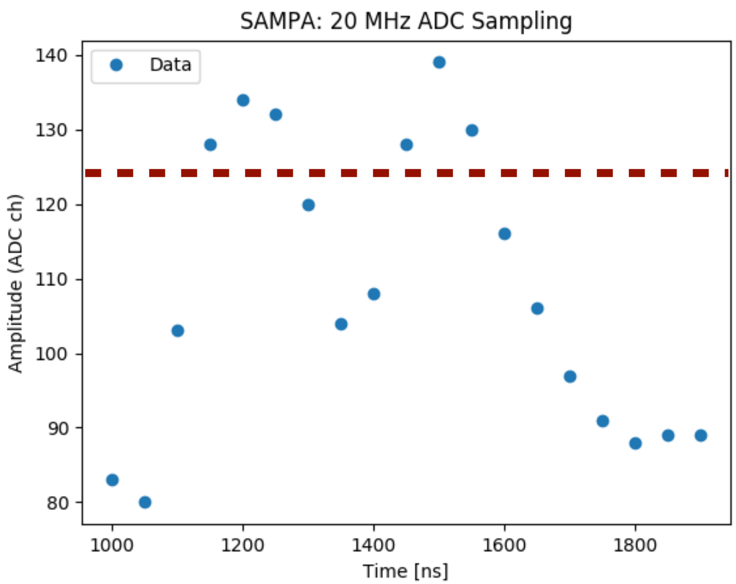


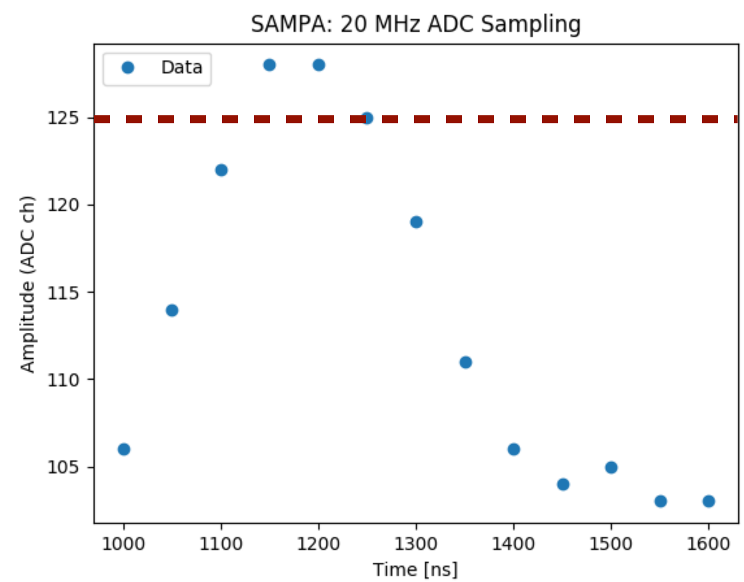


SAMPA Response to Cosmic GEM Data

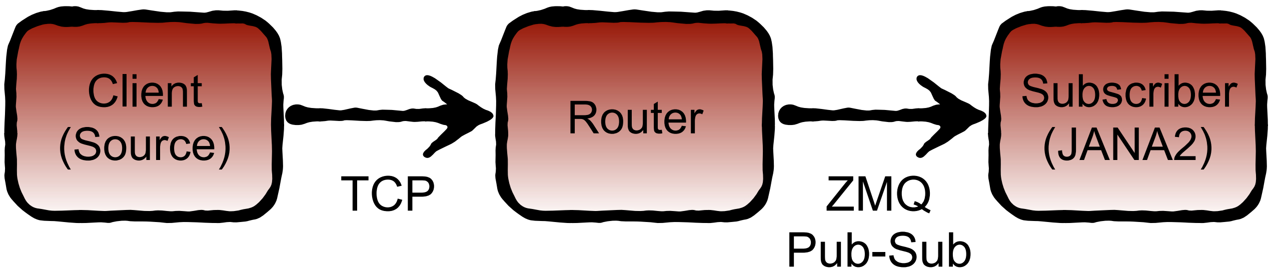
- Our current pulse fitting algorithm is only optimized for pulser inputs
- More development is required to handle real pulses emanating from a real detector
- Infrastructure to apply per channel thresholds is required in order to analyze GEM cluster data
- Handing corner cases will require a sizable amount of attention ➢ double pulsing, window edge hits, etc.
- Utilizing the integral as quantifying the pulse is easier



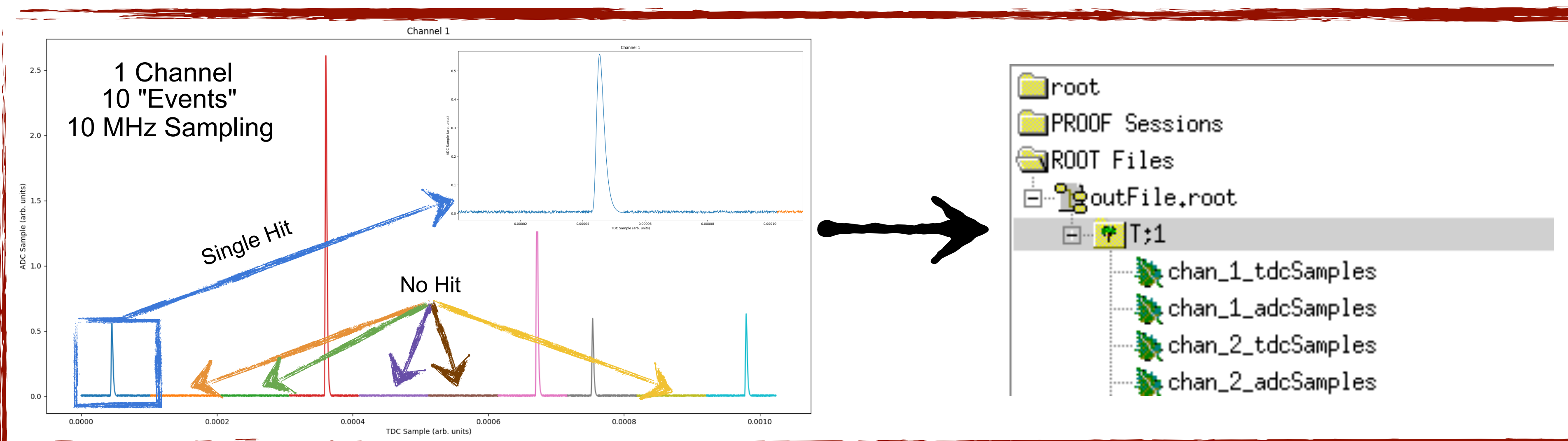




TDIS SRO Data Transfer Protocol



- Router receives data from emulator or hardware sources and publishes data to subscribers (analyzers) ➛ SAMPA SRO emulator and JANA2 plugin have been developed
- Open source ZeroMQ library was chosen as the publish-subscribe data transport between the router and the subscriber ➛ Mature library that is well maintained and is evolving
- INDRA-Streaming software exists and is actively being developed to interface with JANA2



Looking Forward

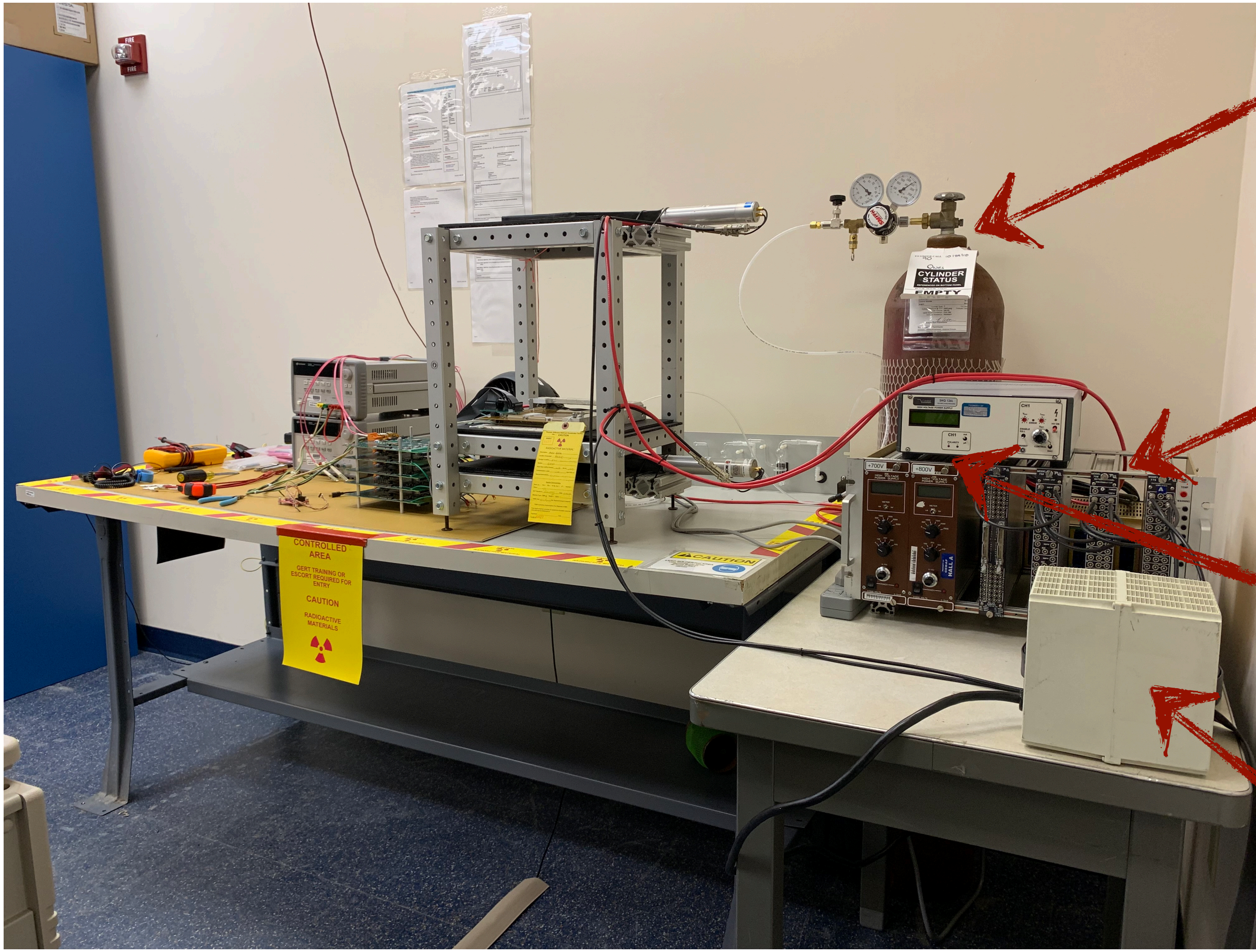
- Reduce observed noise as much as possible in TDIS SRO prototype
  - Improve ground connection between FEC and GEM, EM shielding
- Configure SRO DAQ for zero-suppression (DSP mode) operation
  - Establish pedestal/threshold database
  - Suppress non-data sync headers and reformat hit data
- Develop T-RORC firmware to stream only hit data to memory
- Integrate FELIX (100 Gb/s) readout hardware and software
  - Utilize FELIX software to configure FEC hardware
- Complete the chain of SRO
  - TIDIS SRO Prototype ➛ Router ➛ JANA2 Subscriber ➛ JupyterLab Real Time Online Analysis
- Special thanks to: E. Jastrzembski, J. Wilson, A. Hellman, et al.

SBS Collaboration Meeting

Questions?

Backup Slides

TDIS SRO Test Stand Setup



75/25 Ar/CO_2 Gas System

NIM Cosmic Trigger

HV Power Supplies

Isolation Transformer

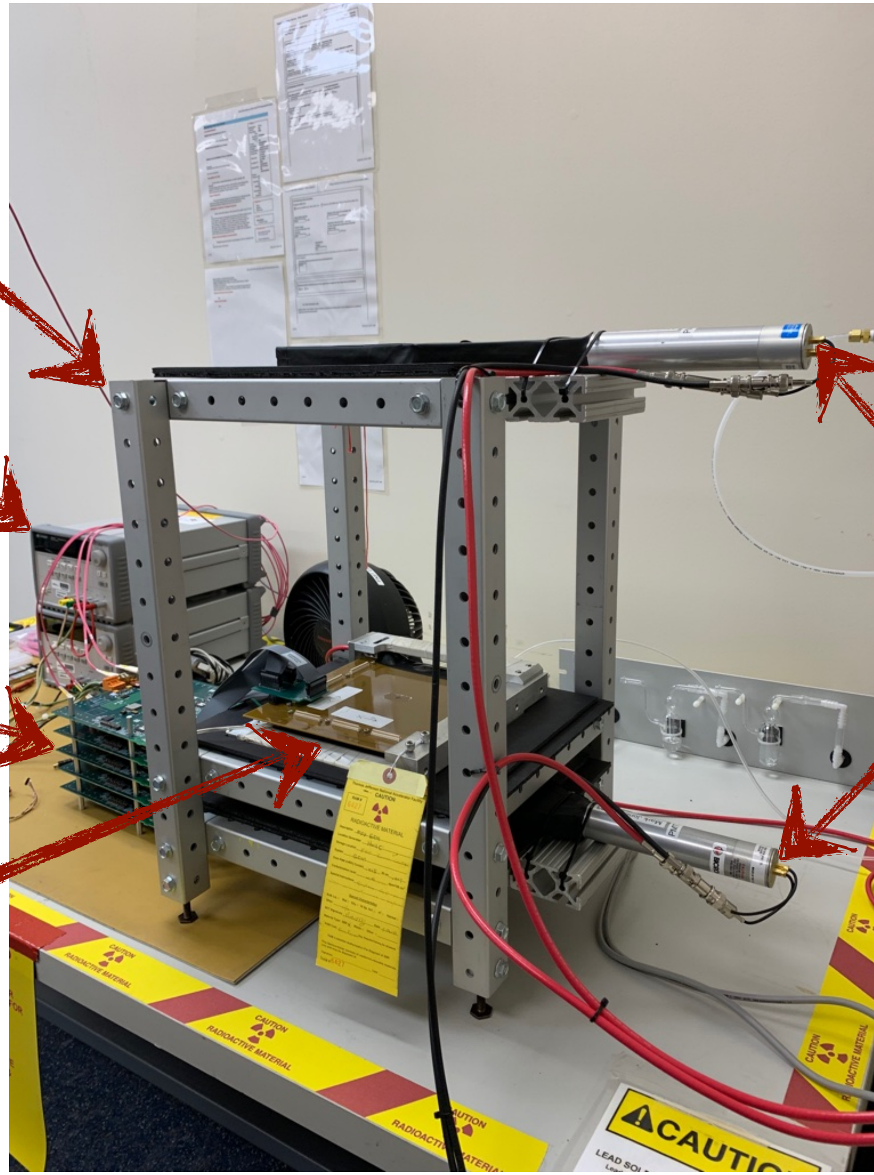
TIDIS SRO Test Stand Setup

Cosmic Test Stand

FEC LV Power Supply

ALICE FEC's (x5)

GEM Detector



Trigger PMTs

ALICE SAMPA Specifications

Specification	TPC	MCH
Voltage supply	1.25 V	1.25 V
Polarity	Negative	Positive
Detector capacitance (Cd)	18.5 pF	40 pF - 80 pF
Peaking time (ts)	160 ns	300 ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 600e@ts=160 ns*	< 950e @ Cd=40 pF* < 1600e @ Cd=80 pF*
Linear Range	100 fC or 67 fC	500 fC
Sensitivity	20 mV/fC or 30 mV/fC	4 mV/fC
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts=160 ns	< 0.2%@ts=300 ns
ADC effective input range	2 Vpp	2 Vpp
ADC resolution	10-bit	10-bit
Sampling Frequency	10 (20) Msamples/s	10 Msamples/s
INL (ADC)	<0.65 LSB	<0.65 LSB
DNL (ADC)	<0.6 LSB	<0.6 LSB
ENOB (ADC)**	> 9.2-bit	> 9.2-bit
Power consumption (per channel) CSA + Shaper + ADC	< 15 mW	< 15 mW
Channels per chip	32	32

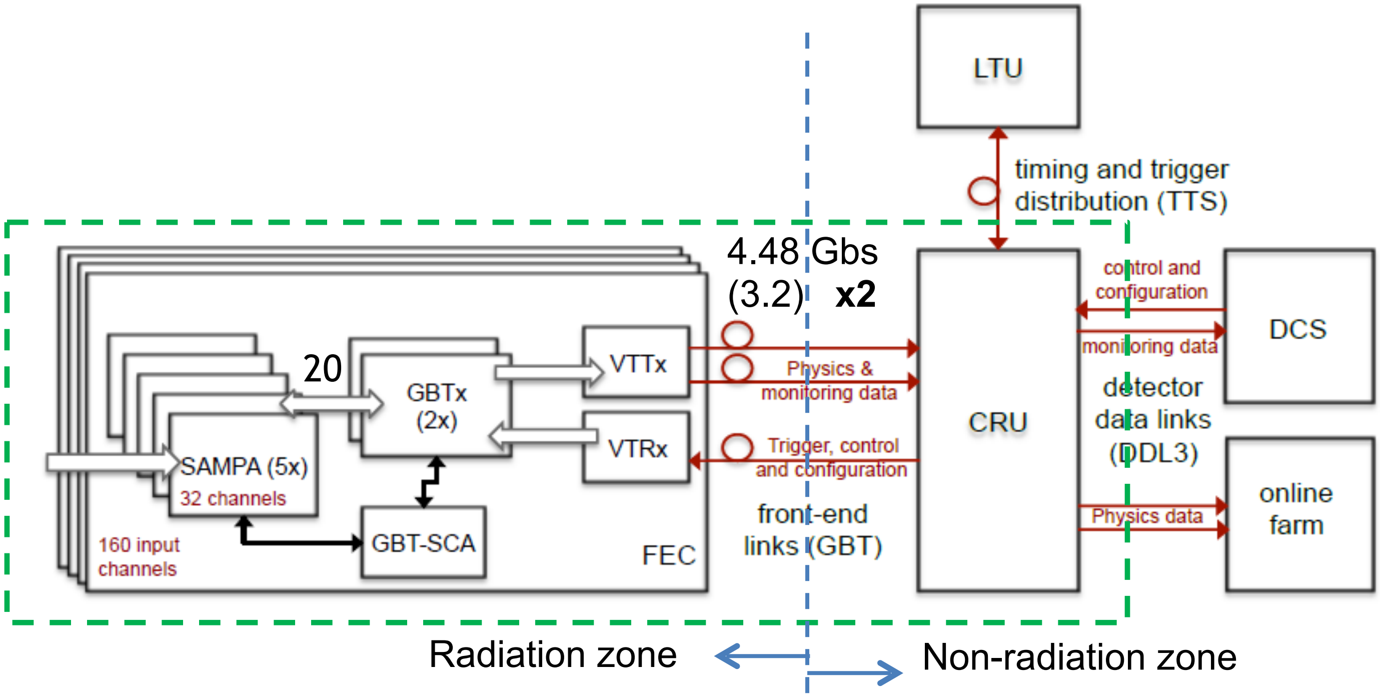
*$R_{esd} = 70\Omega$

** @ 0.5MHz, 10Msamples/s

Slide Courtesy of E. Jastrzembski

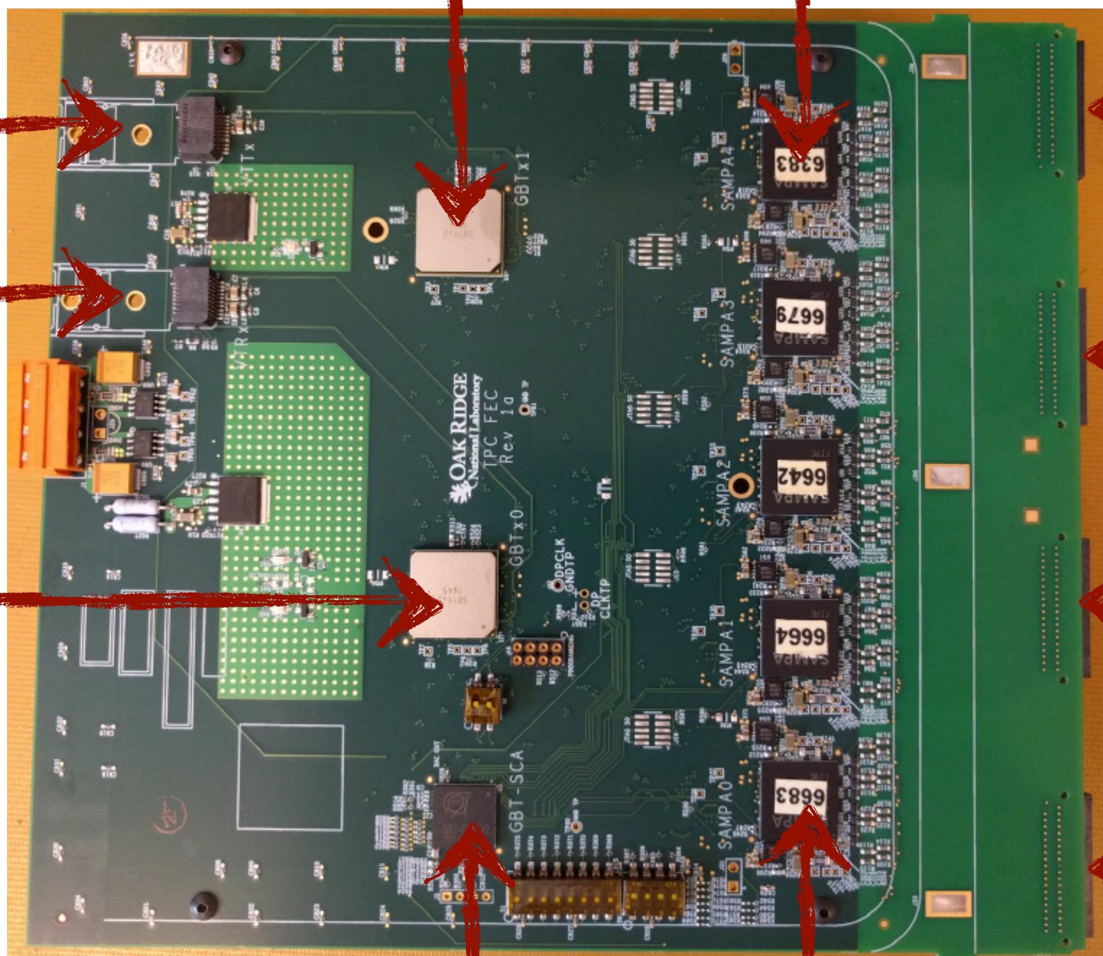
ALICE System

- FEC – Front End Card (160 ch / FEC)
- CRU – Common Readout Unit ~12 FECs / CRU = ~1920 ch / CRU
- DCS – Detector Control System
- LTU – Local Trigger Unit



Slide Courtesy of E. Jastrzembski

ALICE FEC (JLab Version)



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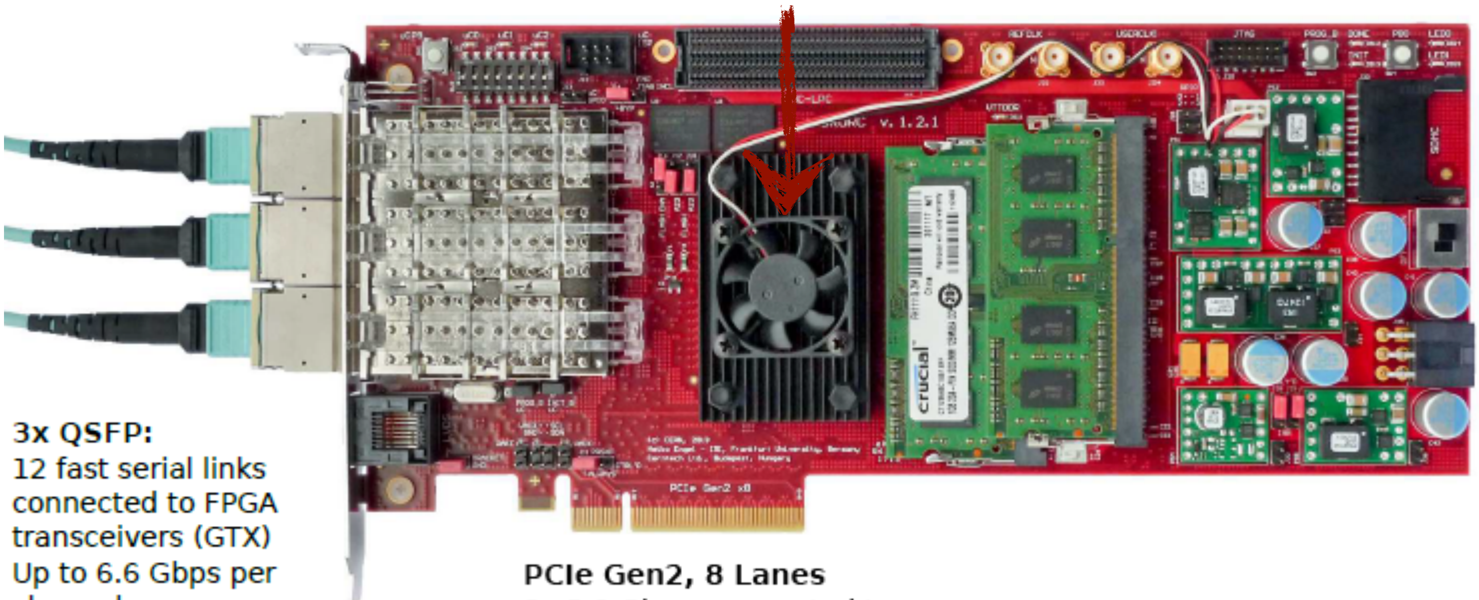
C-RORC (Common Readout Receiver Card)

Xilinx Virtex-6 FPGA



3x QSFP:
12 fast serial links connected to FPGA transceivers (GTX)
Up to 6.6 Gbps per channel

PCIe Gen2, 8 Lanes
8x 5.0 Gbps, connected to Xilinx PCIe Hard Block

(~ 30 Gb/s)

Slide Courtesy of E. Jastrzembski

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