Streaming Readout Grand Challenge

TDIS Streaming Readout Prototype

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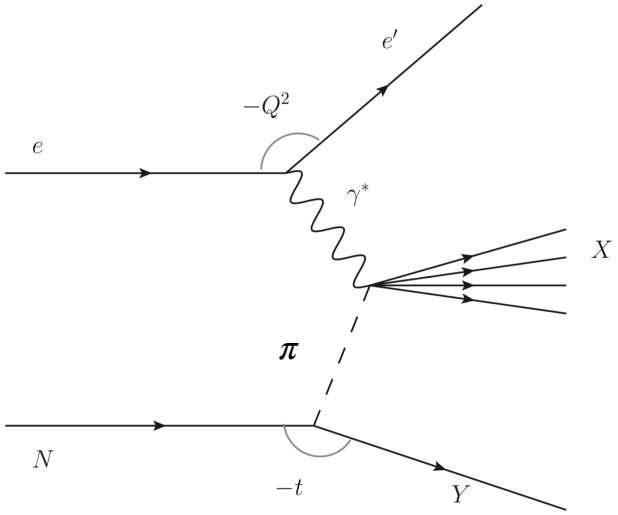
On Behalf of the TDIS SRO Working Group

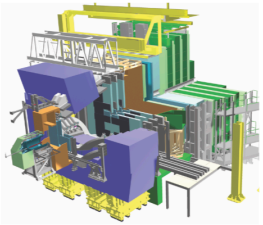
TDIS Streaming Readout Prototype

- TDIS ≡ Tagged Deep Inelastic Scattering
  - Hall-A, Super Big-Bite (SBS)
  - Measure high W², Q² electron-meson scattering events
  - A GEM based radial time projection chamber (TPC) will facilitate the detection of low momentum spectators
- ALICE collaboration (CERN) is currently upgrading their TPC with a GEM based detection system that is read out continuously
  - Streaming readout (SRO)
  - Continuous time ordered sequences of detector system readout
  - ~1 TB/s post zero-suppression
- Novel front-end ASIC was developed specifically for this purpose ➛ SAMPA
- We are interested in exploring how experiments at JLab can take advantage of this technology as well as the SRO concept
  - SRO Grand Challenge



JINST 8 (2013) P04022

Real-Time Processing



Simple feature-building, e.g. in FPGAs, required to reduce the data rate.*

1 TB/s post zero suppression

50 GB/s

1 MHz

Heavy use of machine learning: V.Gligorov, MW, JINST 8 (2012) P02013.

Full real-time reconstruction for all particles available to select events.

Data buffered on 10 PB of disk.

8 GB/s

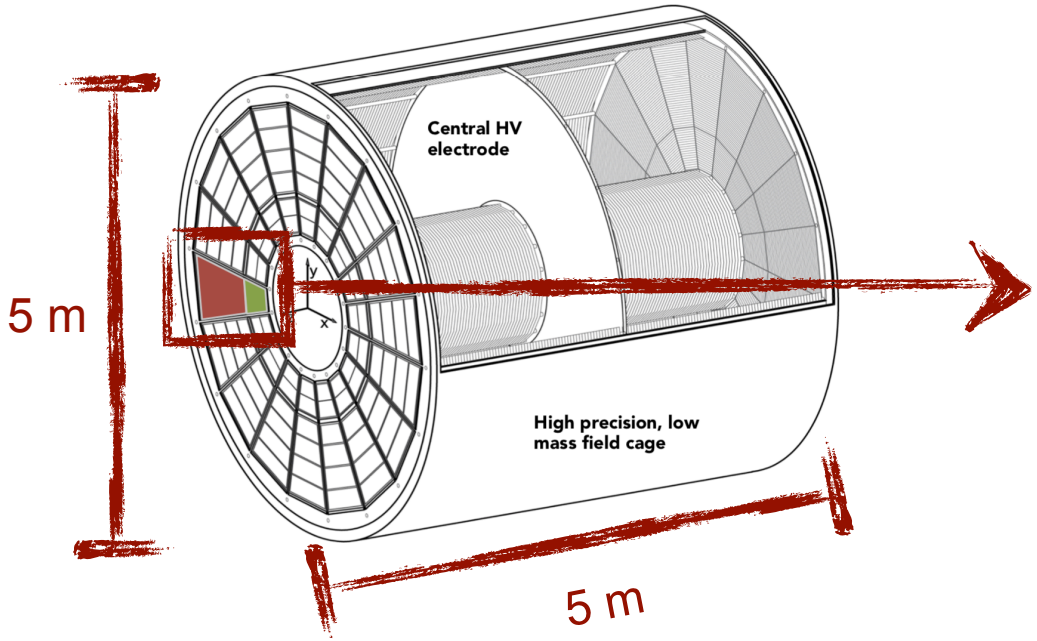
Real-time reconstruction for all charged particles with $p_T > 0.5$GeV.

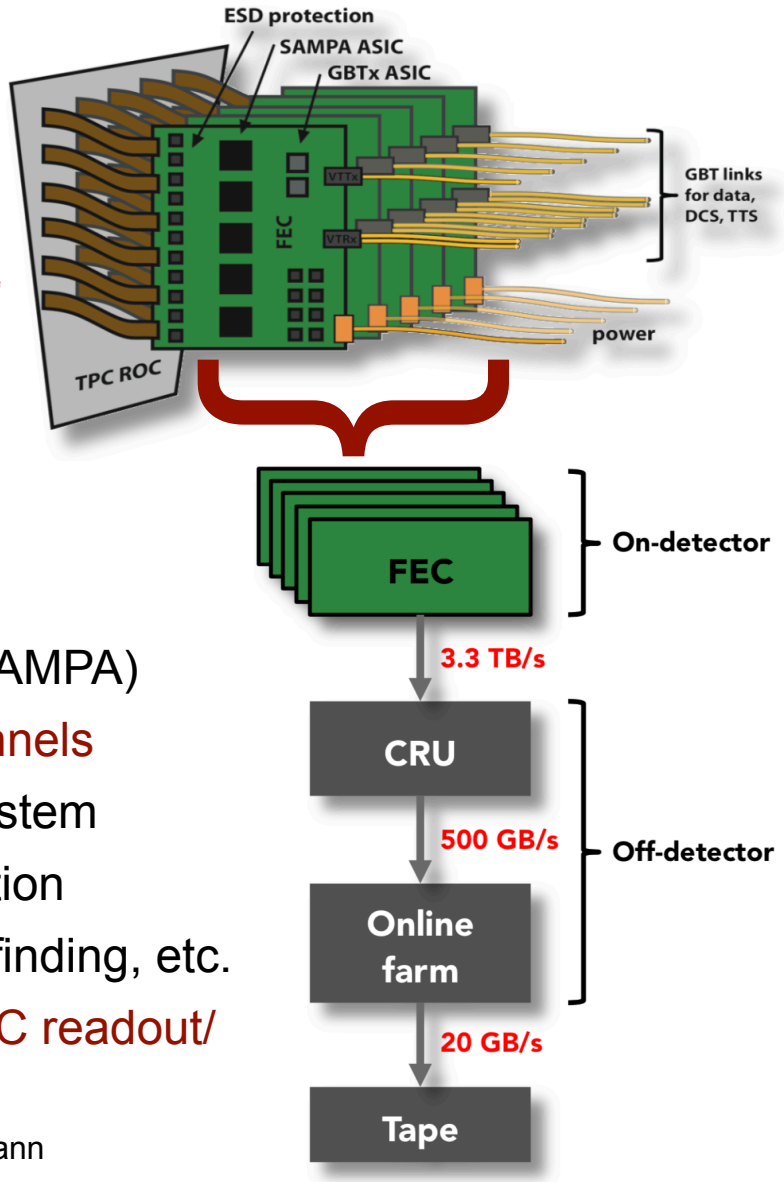
Real-time calibration & alignment.

0.7 GB/s (mix of full + partial events)

*LHCb will move to a triggerless-readout system for LHC Run 3 (2021-2023), and process 5 TB/s in real time on the CPU farm.

ALICE TPC SRO Strategy



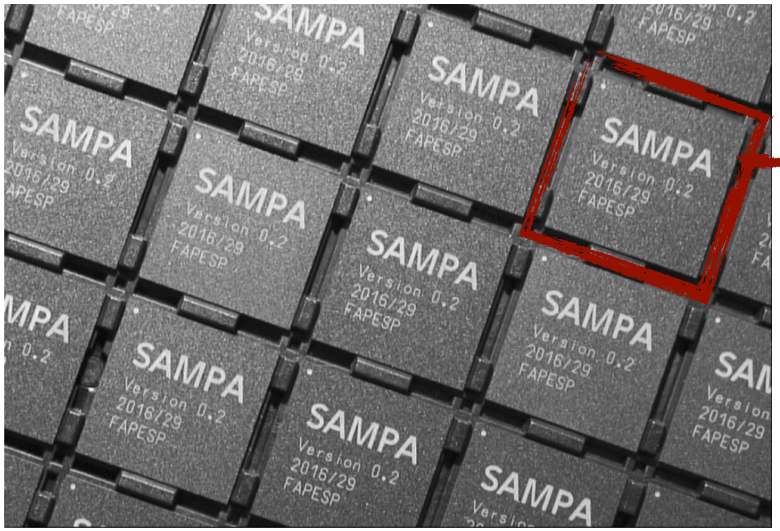


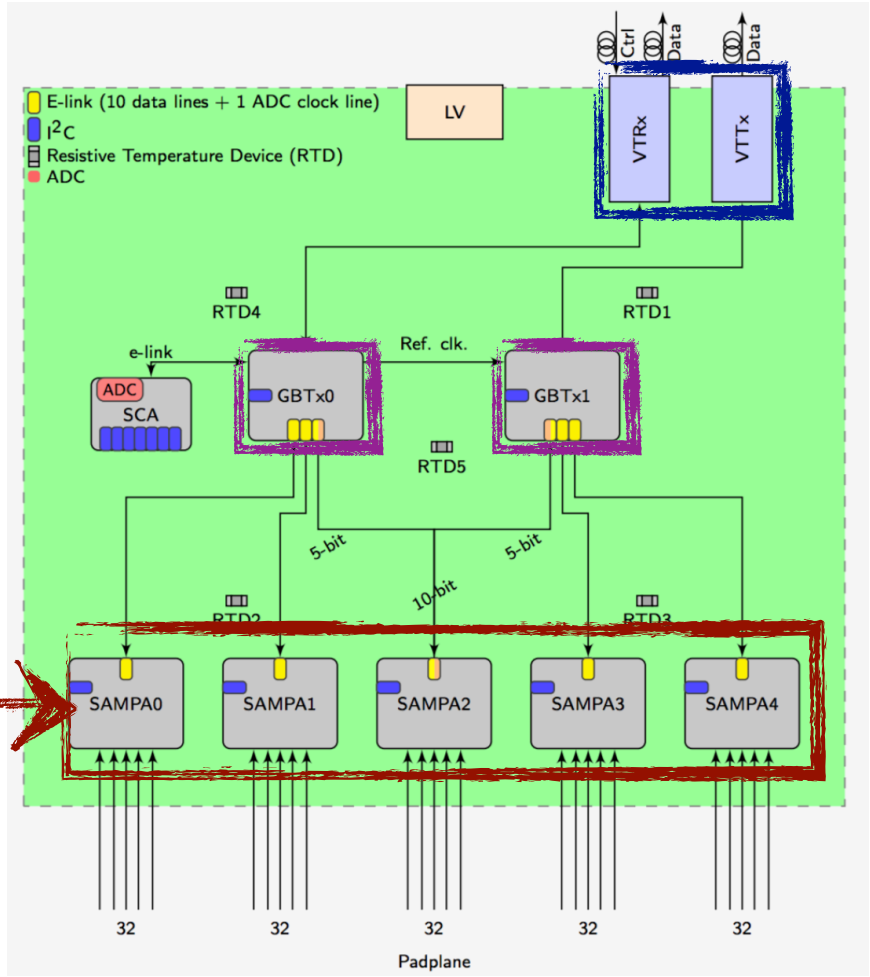
- Continuously readout all TPC ADC channels (via SAMPA)
  - ALICE : 10k FEC's ➛ 50k chips ➛ ~1.6M channels
- Radiation hard CERN Gigabit transceiver (GBT) system
- Common readout unit (CRU) ➛ Online data correction
  - PCIe platform ➛ Baseline corrections, cluster finding, etc.
- TDIS SRO prototype is utilizing as many ALICE TPC readout/ control chain components as possible

Slide Adapted From C. Lippmann

ALICE SRO Electronics

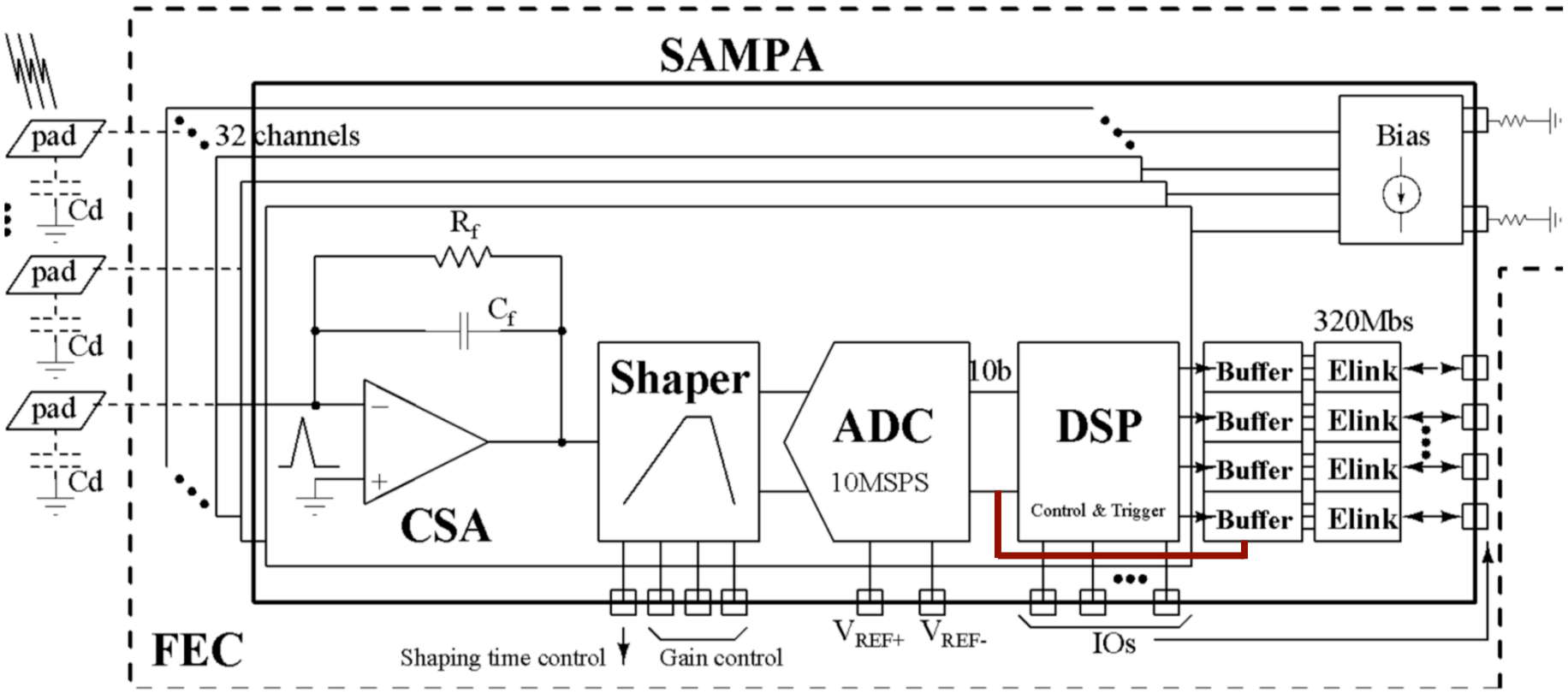
- SAMPA : University of São Paulo, Brazil
- Supports both continuous and triggered readout modes
- Digital signal processor (can be bypassed)
- Single ALICE front end card (FEC) supports 5 SAMPA chips (160 channels)
- Serialized data are routed via e-links into 2 GBTx chips which drive fiber transmitters (VTTx) at 3.2 Gb/s each





SAMPA Operational Modes

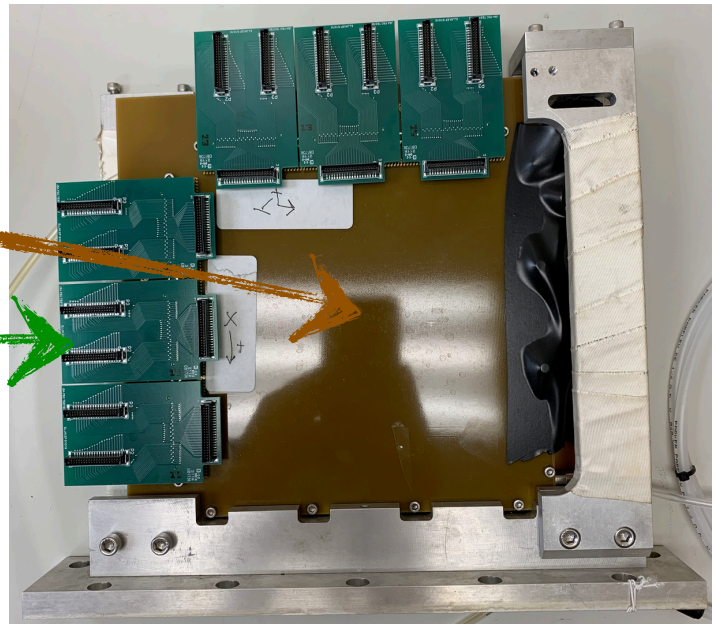
- Direct ADC serialization (DAS) mode ➛ bypass digital signal processor (DSP)
  - ALICE FEC design limits ADC rate to 5 MHz in DAS mode ➛ 10 e-links (max 3.2 Gb/s)
- DSP mode ➛ pedestal subtraction, baseline corrections, zero-suppression, compression
  - Sampling rates of 10 or 20 MHz ➛ 11 e-links (max 3.2 Gb/s or 6.4 Gb/s)



Slide Courtesy of E. Jastrzembski

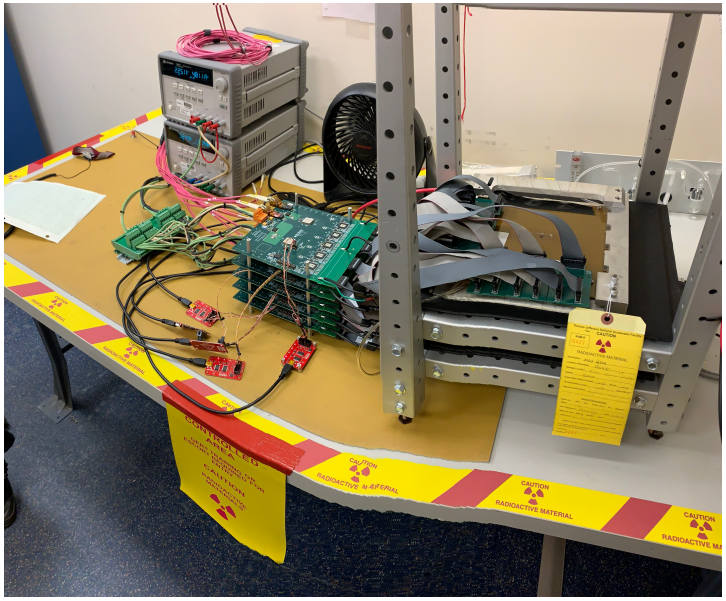
TDIS SRO Prototype

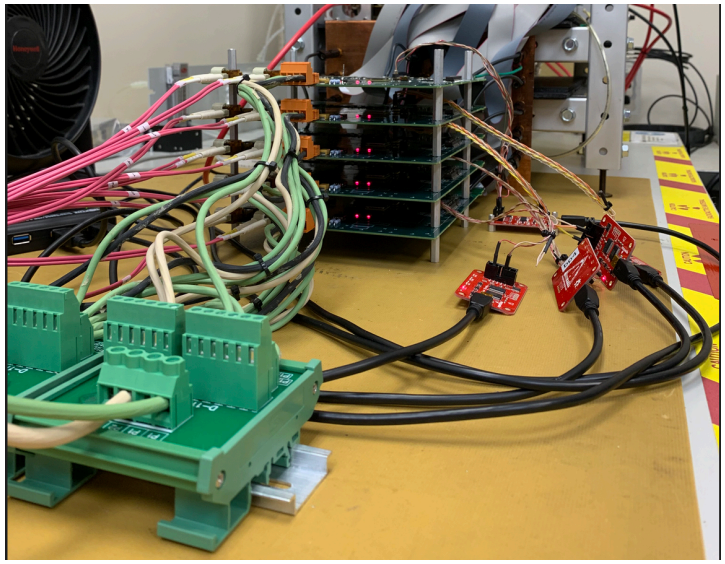
- INDRA-ASTRA Facility (CC F110)
- Variety of hardware present so that it is "streaming capable"
  - User programmable network switch with 100 Gb/s data link
  - Fast multi-core server machine with 100 Gb/s data link
  - Fast PC's with several PCIe slots for testing high speed data links, FPGAs, GPU's, etc.
- Triple-GEM detector provides 768 channels of analog data
- Custom transition card fabricated to facilitate ALICE FEC inputs
- 800 channels of SAMPA readout (5 FEC's, 25 SAMPA chips) via ALICE SRO system



TDIS SRO Prototype

- Currently we are streaming trigger-less GEM data (768 channels) in DAS mode at 45 Gb/s via 5 ALICE FEC's
  - GEM ➛ FEC ➛ TRORC (30 Gb/s) ➛ PC Memory ➛ Disk
- By implementing the receipt of a trigger, a programmable window of streamed data can be captured by the T-RORC
  - Keeps the data volume to memory (and to disk) at a manageable level
- Will modify the T-RORC firmware to suppress the transmission of unnecessary sync packet data to memory and disk
  - Sync packets keep the serial links from the SAMPAs active when there is no hit data to send
- Then we can acquire data in a truly continuous fashion





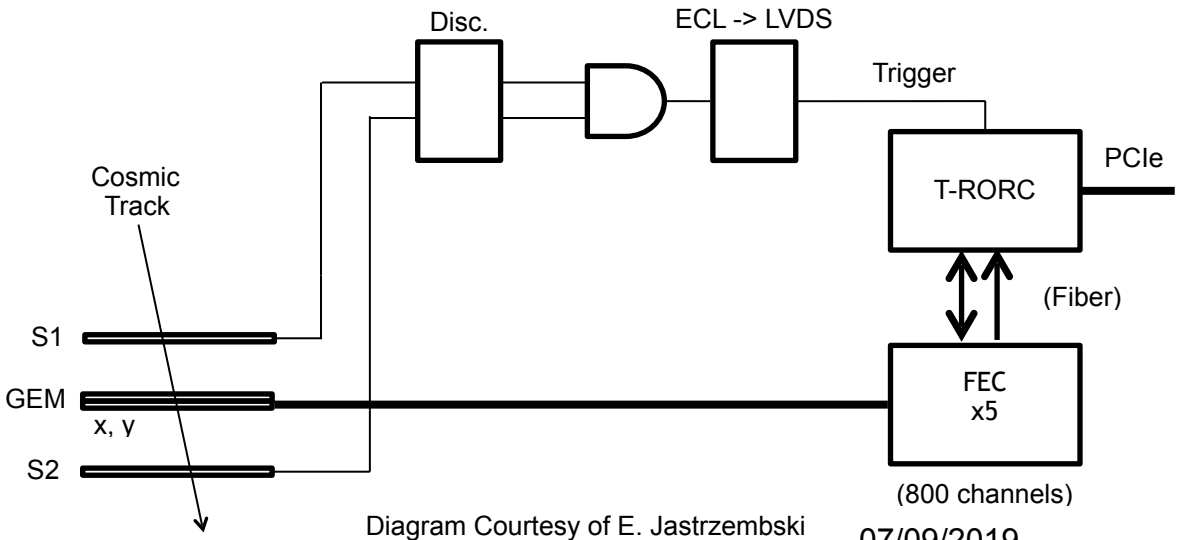
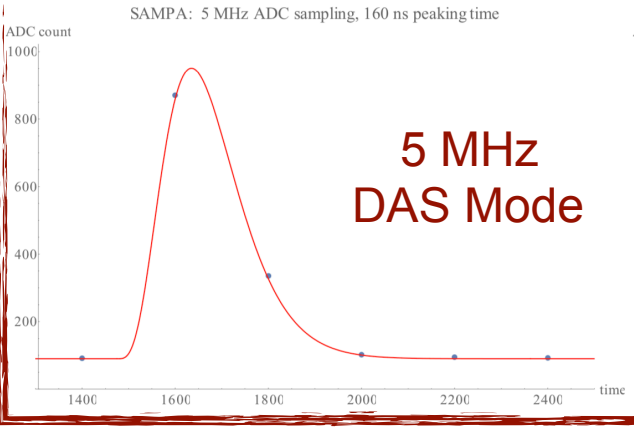


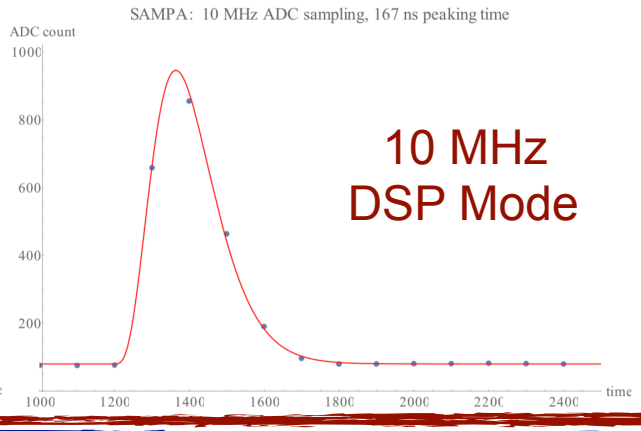
Diagram Courtesy of E. Jastrzembski

TDIS SRO SAMPA Data

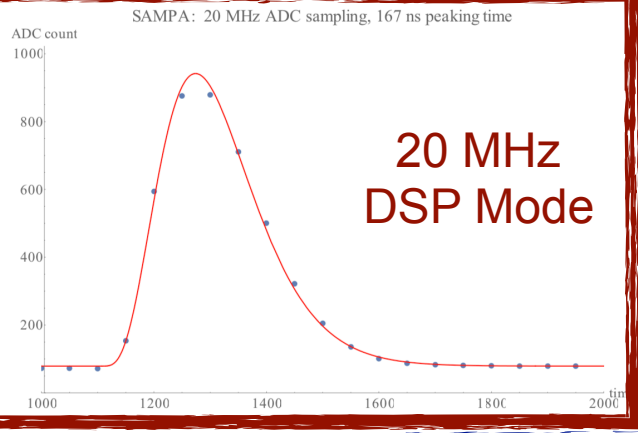
- Variety of ways to analyze/monitor the data are actively being developed
- SAMPA response to test pulse ➛ 5 MHz, 10 MHz, and 20 MHz
- TDIS SRO GEM data ➛ 5 MHz DAS mode ➛ sample, μ_{ped}, and σ_{ped} data



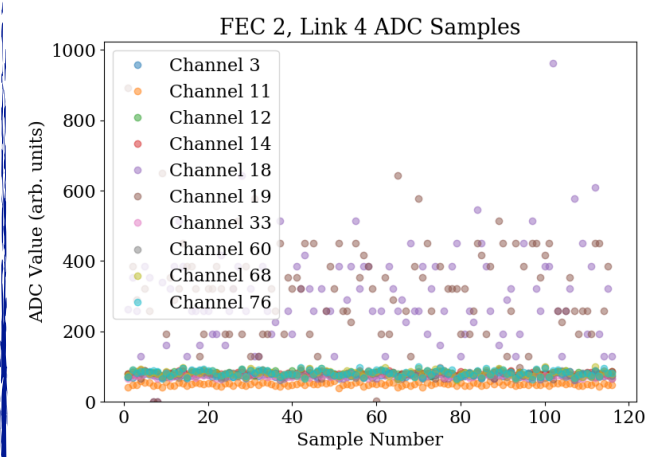
5 MHz
DAS Mode

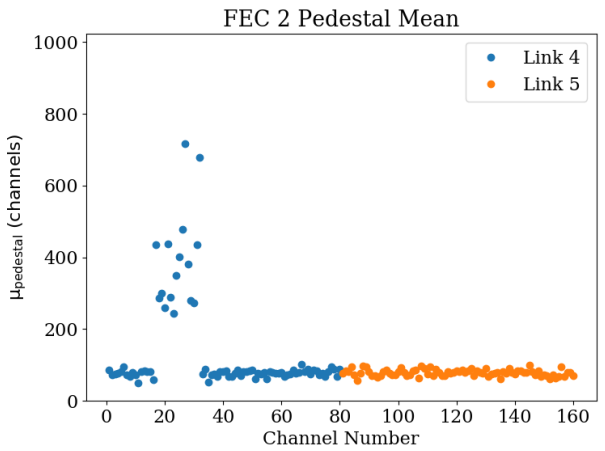


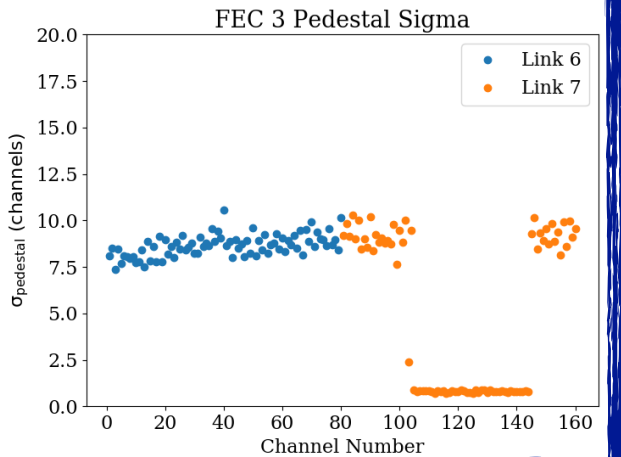
10 MHz
DSP Mode



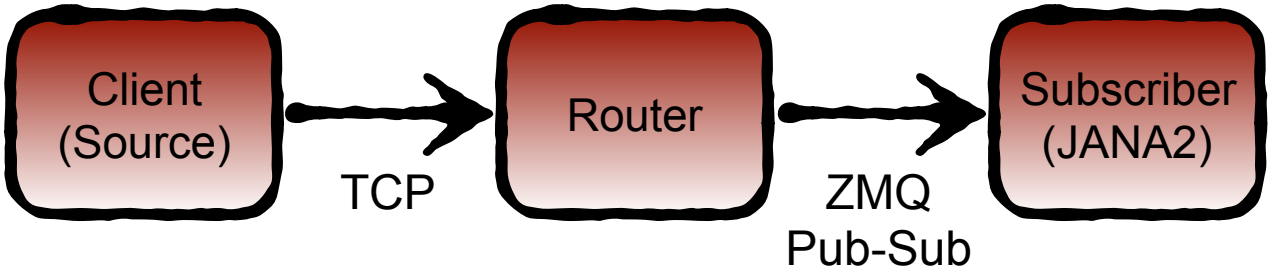
20 MHz
DSP Mode



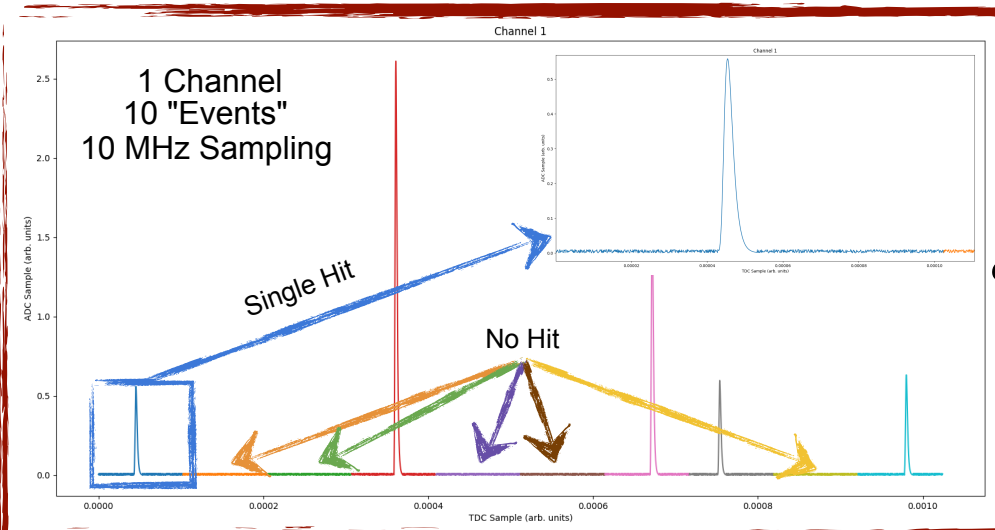


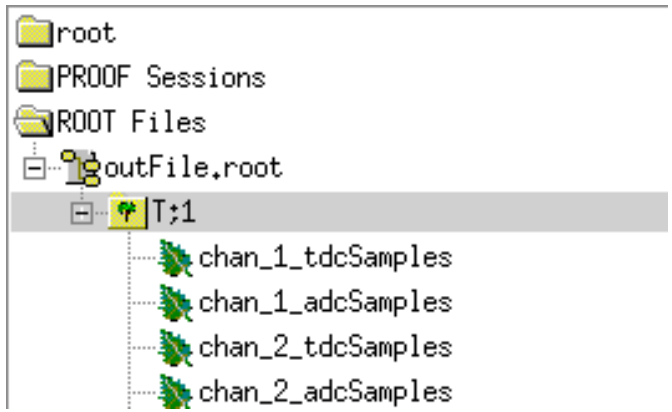


TDIS SRO Data Transfer Protocol



- Router receives data from emulator or hardware sources and publishes data to subscribers (analyzers) ➛ SAMPA SRO emulator and JANA2 plugin have been developed
- Open source ZeroMQ library was chosen as the publish-subscribe data transport between the router and the subscriber ➛ Mature library that is well maintained and is evolving
- INDRA-Streaming software exists and is actively being developed to interface with JANA2





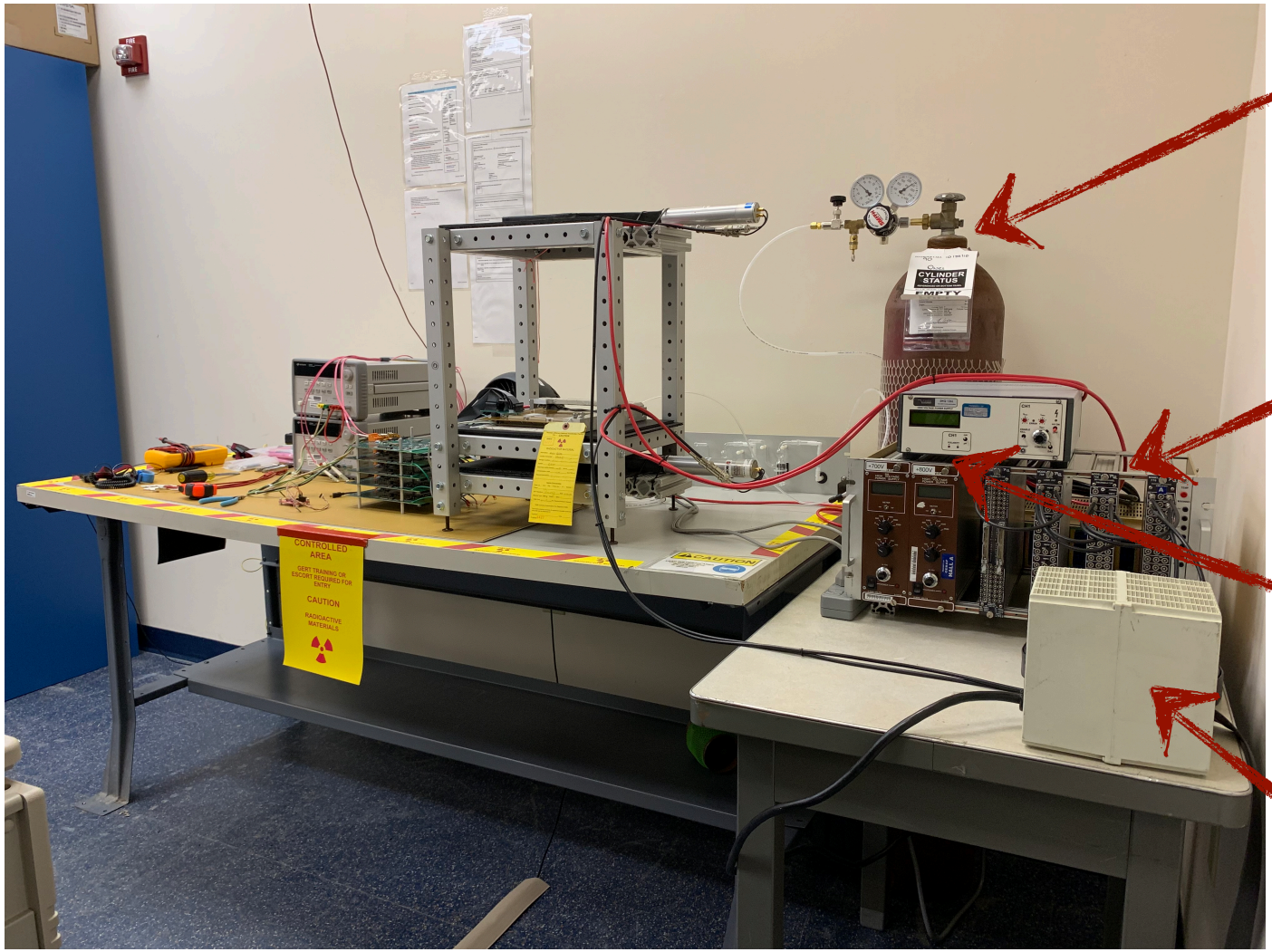
Looking Forward

- Reduce observed noise as much as possible in TDIS SRO prototype
  - Improve ground connection between FEC and GEM, EM shielding
- Integrate cosmic trigger into SRO DAQ
  - NIM ➛ LVDS conversion, configure SAMPA trigger latency
- Configure SRO DAQ for zero-suppression (DSP mode) operation
  - Create pedestal/threshold database
  - Suppress non-data sync headers and reformat hit data
- Develop T-RORC firmware to stream only hit data to memory
- Integrate FELIX readout hardware and software
  - Utilize FELIX software to configure FEC hardware
- Complete the chain of SRO
  - TIDIS SRO Prototype ➛ Router ➛ JANA2 Subscriber ➛ JupyterLab
- Special thanks to: E. Jastrzembski, J. Wilson, A. Hellman, C. Long, et al.

Streaming Readout Grand Challenge

Backup Slides

TDIS SRO Test Stand Setup



75/25 Ar/CO_2 Gas System

NIM Cosmic Trigger

HV Power Supplies

Isolation Transformer

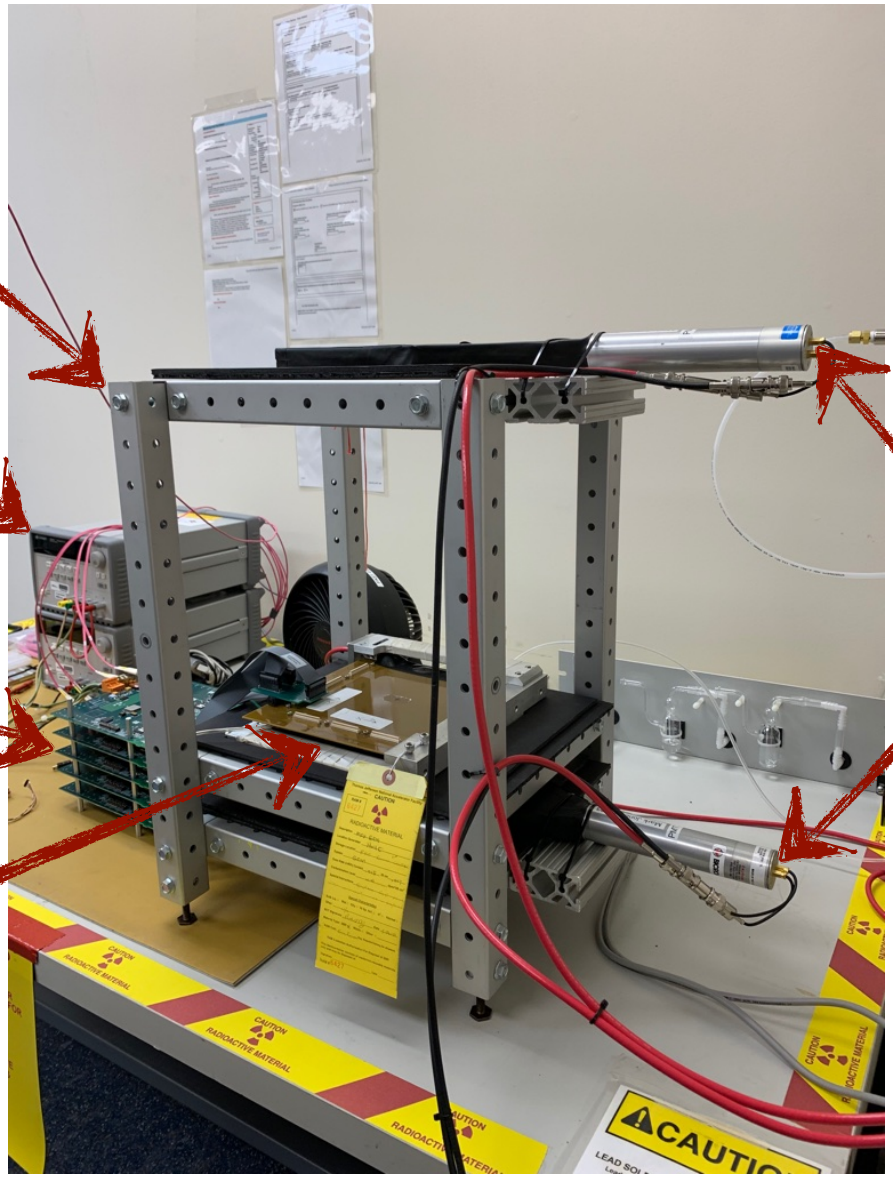
TIDIS SRO Test Stand Setup

Cosmic Test Stand

FEC LV Power Supply

ALICE FEC's (x5)

GEM Detector



Trigger PMTs

TDIS Streaming Readout Prototype

Traditional triggered readout

- data is digitized into buffers and a trigger, per event, starts readout
- parts of events are transported through the DAQ to an event builder where they are assembled into events
- **event selection** based on fast detectors with coarse resolution

default at JLab experiments

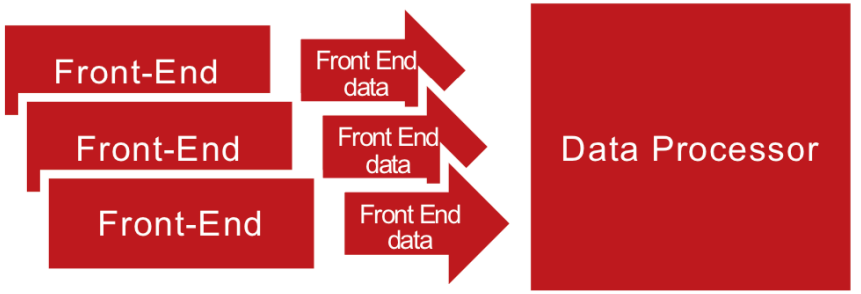
Streaming readout

- data is read continuously from all channels
- data then flows unimpeded in parallel channels to storage or a local compute resource
- **event selection** based on full detector information

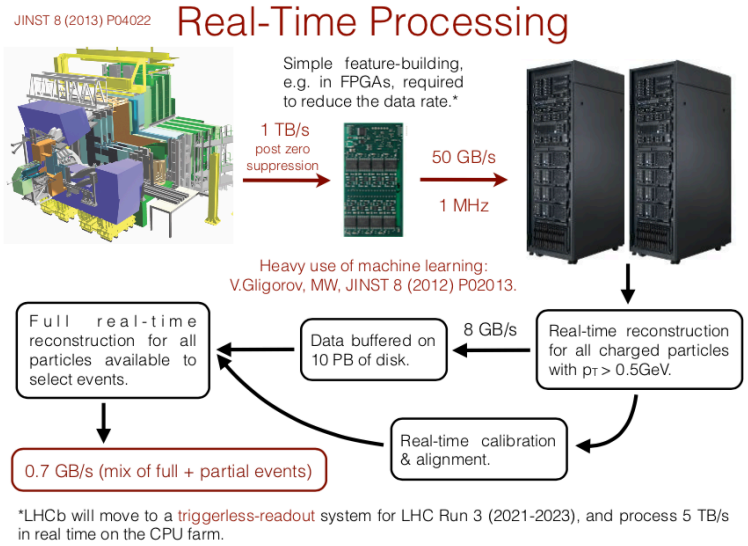
intended for TDIS, SoLid, EIC

Slide Courtesy of M. Diefenthaler

TDIS Streaming Readout Prototype



LHCb Example



Data Processor

- assembles the data into events
- outputs data suitable for final analysis (**Analysis data**)

Features (among others)

- ideal for machine learning
- automated calibration and alignment
- partial or full event reconstruction
- event selection and/or labeling into analysis streams
- automated anomaly detection
- responsive detectors (conscious experiment)

Slide Courtesy of M. Diefenthaler

ALICE SAMPA Specifications

Specification	TPC	MCH
Voltage supply	1.25 V	1.25 V
Polarity	Negative	Positive
Detector capacitance (Cd)	18.5 pF	40 pF - 80 pF
Peaking time (ts)	160 ns	300 ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 600e@ts=160 ns*	< 950e @ Cd=40 pF* < 1600e @ Cd=80 pF*
Linear Range	100 fC or 67 fC	500 fC
Sensitivity	20 mV/fC or 30 mV/fC	4 mV/fC
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts=160 ns	< 0.2%@ts=300 ns
ADC effective input range	2 Vpp	2 Vpp
ADC resolution	10-bit	10-bit
Sampling Frequency	10 (20) Msamples/s	10 Msamples/s
INL (ADC)	<0.65 LSB	<0.65 LSB
DNL (ADC)	<0.6 LSB	<0.6 LSB
ENOB (ADC)**	> 9.2-bit	> 9.2-bit
Power consumption (per channel) CSA + Shaper + ADC	< 15 mW	< 15 mW
Channels per chip	32	32

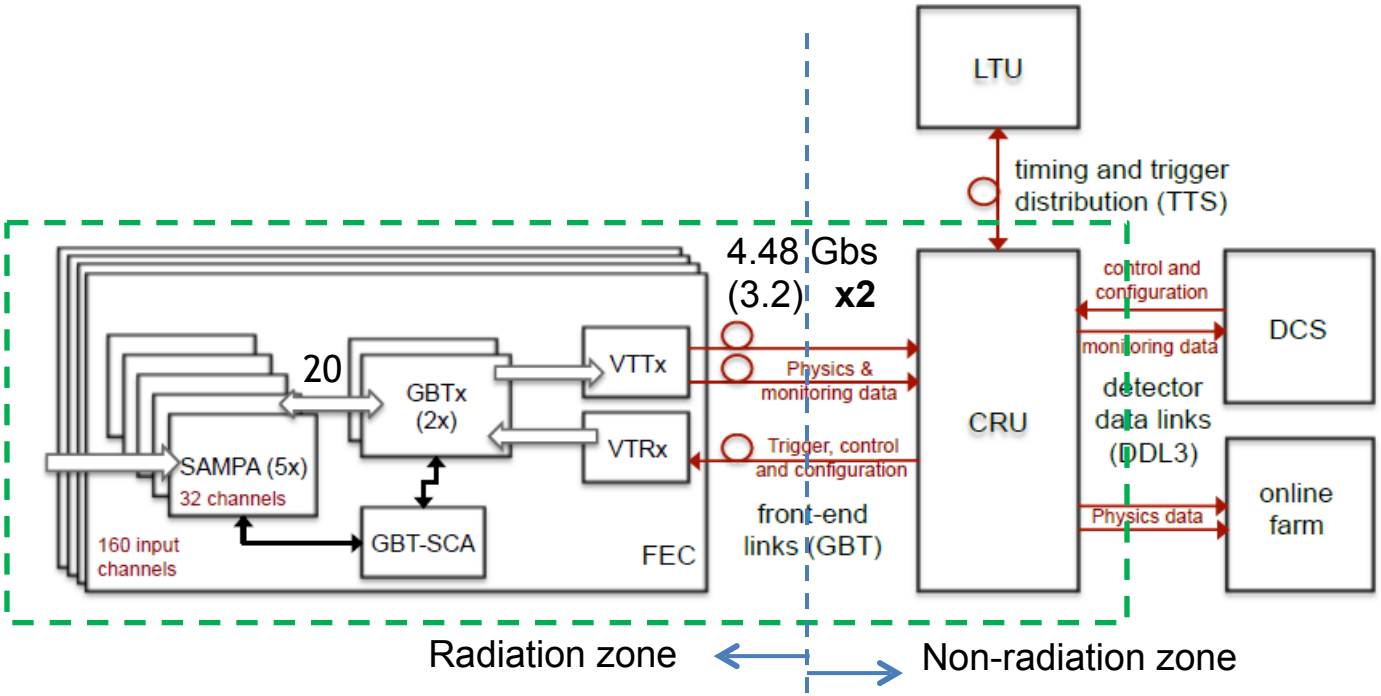
*R_{esd} = 70Ω

** @ 0.5MHz, 10Msamples/s

Slide Courtesy of E. Jastrzembski

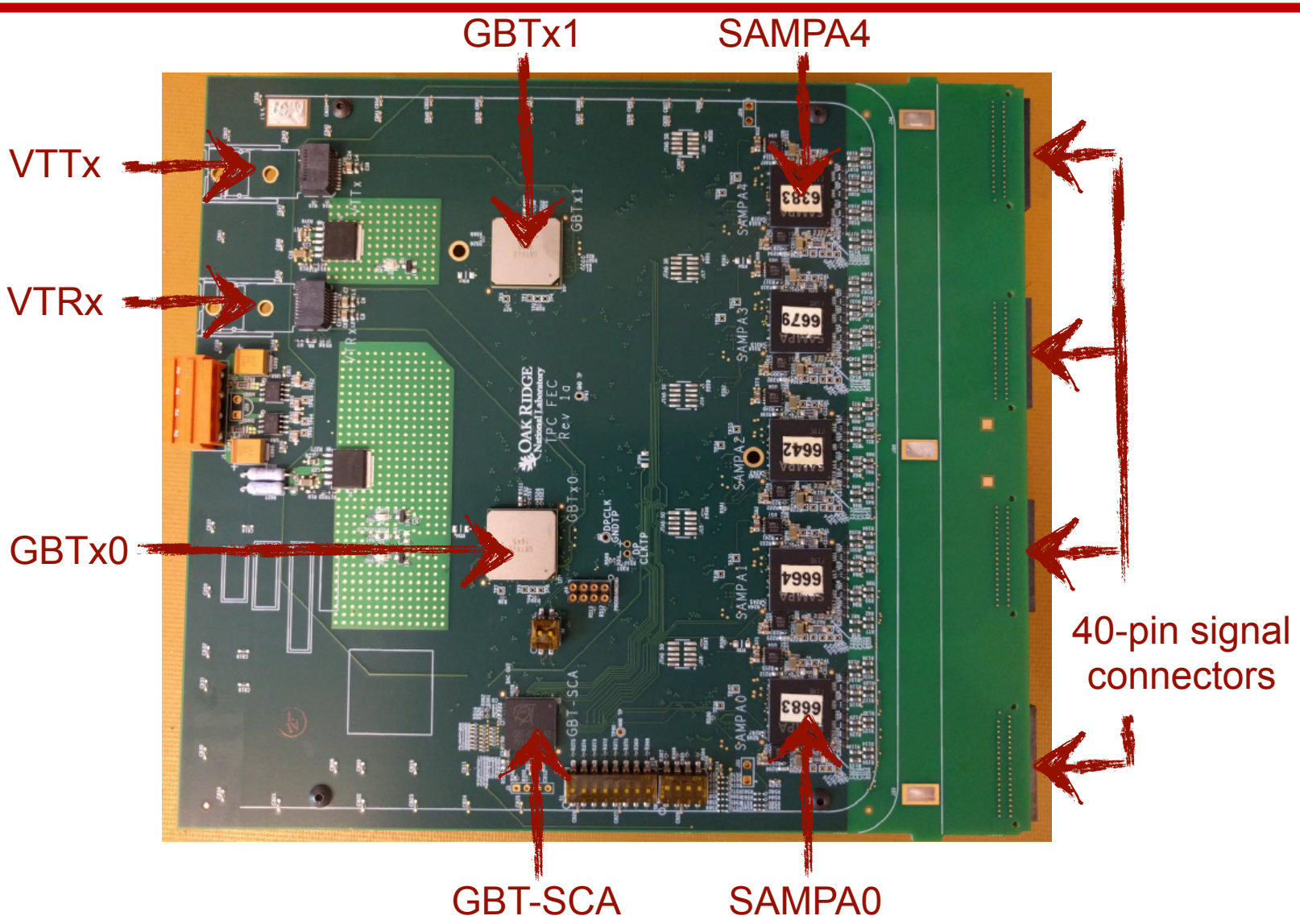
ALICE System

- FEC – Front End Card (160 ch / FEC)
- CRU – Common Readout Unit ~12 FECs / CRU = ~1920 ch / CRU
- DCS – Detector Control System
- LTU – Local Trigger Unit



Slide Courtesy of E. Jastrzembski

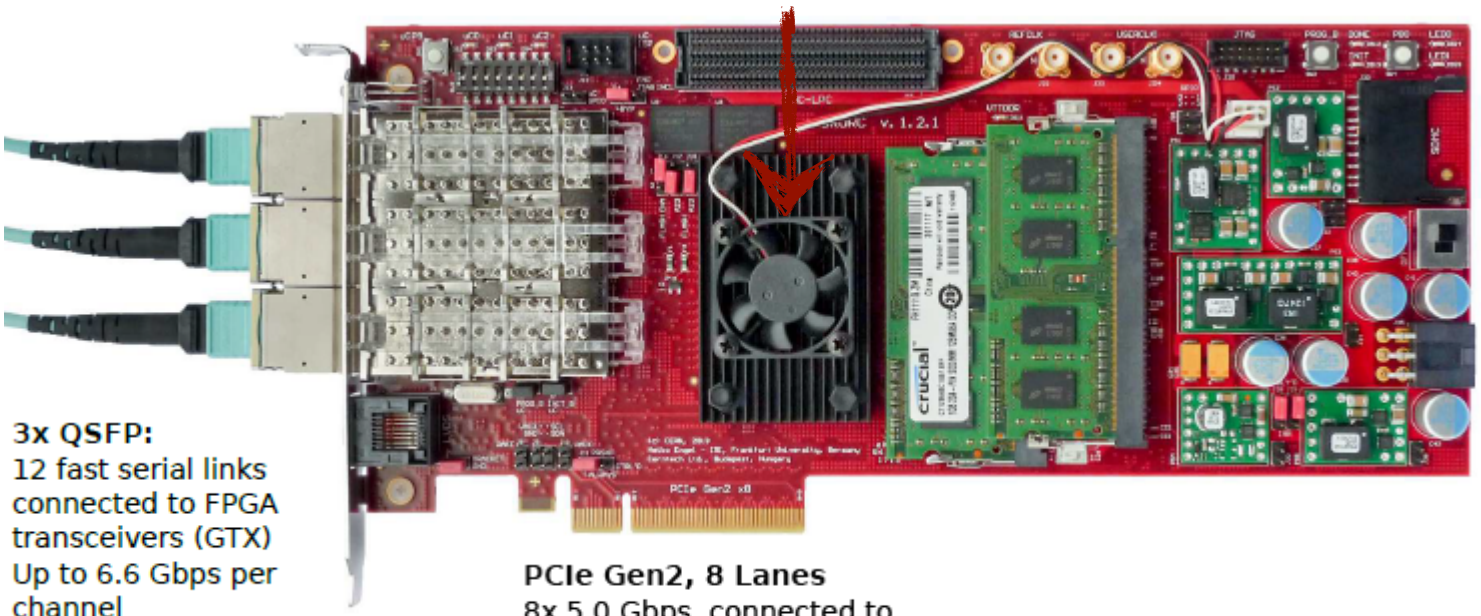
ALICE FEC (JLab Version)



Slide Courtesy of E. Jastrzembski

C-RORC (Common Readout Receiver Card)

Xilinx Virtex-6 FPGA



3x QSFP:
12 fast serial links connected to FPGA transceivers (GTX)
Up to 6.6 Gbps per channel

PCIe Gen2, 8 Lanes
8x 5.0 Gbps, connected to Xilinx PCIe Hard Block

(~ 30 Gb/s)

Slide Courtesy of E. Jastrzembski