Streaming Readout Grand Challenge

TDIS Streaming Readout Prototype

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Jefferson Lab
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On Behalf of the TDIS SRO Working Group
· TDIS ≡ Tagged Deep Inelastic Scattering
  · Hall-A, Super Big-Bite (SBS)
  · Measure high $W^2$, $Q^2$ electron-meson scattering events
  · A GEM based radial time projection chamber (TPC) will facilitate the detection of low momentum spectators
· ALICE collaboration (CERN) is currently upgrading their TPC with a GEM based detection system that is read out continuously
  · Streaming readout (SRO)
  · Continuous time ordered sequences of detector system readout
  · ~1 TB/s post zero-suppression
· Novel front-end ASIC was developed specifically for this purpose ➔ SAMPA
· We are interested in exploring how experiments at JLab can take advantage of this technology as well as the SRO concept
  · SRO Grand Challenge
ALICE TPC SRO Strategy

- Continuously readout all TPC ADC channels (via SAMPA)
  - ALICE: 10k FEC’s $\rightarrow$ 50k chips $\rightarrow$ $\sim$1.6M channels
- Radiation hard CERN Gigabit transceiver (GBT) system
- Common readout unit (CRU) $\rightarrow$ Online data correction
  - PCIe platform $\rightarrow$ Baseline corrections, cluster finding, etc.
- TDIS SRO prototype is utilizing as many ALICE TPC readout/control chain components as possible

Slide Adapted From C. Lippmann
07/09/2019
ALICE SRO Electronics

- **SAMPA**: University of São Paulo, Brazil
- Supports both continuous and triggered readout modes
- Digital signal processor (can be bypassed)
- Single ALICE front end card (FEC) supports 5 SAMPA chips (160 channels)
- Serialized data are routed via e-links into 2 GBTx chips which drive fiber transmitters (VTTx) at 3.2 Gb/s each
SAMPA Operational Modes

- Direct ADC serialization (DAS) mode ➔ bypass digital signal processor (DSP)
  - ALICE FEC design limits ADC rate to 5 MHz in DAS mode ➔ 10 e-links (max 3.2 Gb/s)
- DSP mode ➔ pedestal subtraction, baseline corrections, zero-suppression, compression
  - Sampling rates of 10 or 20 MHz ➔ 11 e-links (max 3.2 Gb/s or 6.4 Gb/s)
TDIS SRO Prototype

- INDRA-ASTRA Facility (CC F110)
- Variety of hardware present so that it is "streaming capable"
  - User programmable network switch with 100 Gb/s data link
  - Fast multi-core server machine with 100 Gb/s data link
  - Fast PC’s with several PCIe slots for testing high speed data links, FPGAs, GPU’s, etc.
- Triple-GEM detector provides 768 channels of analog data
- Custom transition card fabricated to facilitate ALICE FEC inputs
- 800 channels of SAMPA readout (5 FEC’s, 25 SAMPA chips) via ALICE SRO system
Currently we are streaming trigger-less GEM data (768 channels) in DAS mode at 45 Gb/s via 5 ALICE FEC’s

- GEM ➔ FEC ➔ TRORC (30 Gb/s) ➔ PC Memory ➔ Disk
- By implementing the receipt of a trigger, a programmable window of streamed data can be captured by the T-RORC
  - Keeps the data volume to memory (and to disk) at a manageable level
- Will modify the T-RORC firmware to suppress the transmission of unnecessary sync packet data to memory and disk
  - Sync packets keep the serial links from the SAMPAs active when there is no hit data to send
- Then we can acquire data in a truly continuous fashion

Diagram Courtesy of E. Jastrzembski

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Streaming Readout Grand Challenge
TDIS SRO SAMPA Data

- Variety of ways to analyze/monitor the data are actively being developed
- SAMPA response to test pulse ➔ 5 MHz, 10 MHz, and 20 MHz
- TDIS SRO GEM data ➔ 5 MHz DAS mode ➔ sample, $\mu_{\text{ped}}$, and $\sigma_{\text{ped}}$ data

5 MHz DAS Mode

10 MHz DSP Mode

20 MHz DSP Mode

FEC 2, Link 4 ADC Samples

FEC 2 Pedestal Mean

FEC 3 Pedestal Sigma
TDIS SRO Data Transfer Protocol

- Router receives data from emulator or hardware sources and publishes data to subscribers (analyzers) ➔ SAMPA SRO emulator and JANA2 plugin have been developed
- Open source ZeroMQ library was chosen as the publish-subscribe data transport between the router and the subscriber ➔ Mature library that is well maintained and is evolving
- INDRA-Streaming software exists and is actively being developed to interface with JANA2

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Looking Forward

- Reduce observed noise as much as possible in TDIS SRO prototype
  - Improve ground connection between FEC and GEM, EM shielding
- Integrate cosmic trigger into SRO DAQ
  - NIM ➔ LVDS conversion, configure SAMPA trigger latency
- Configure SRO DAQ for zero-suppression (DSP mode) operation
  - Create pedestal/threshold database
  - Suppress non-data sync headers and reformat hit data
- Develop T-RORC firmware to stream only hit data to memory
- Integrate FELIX readout hardware and software
  - Utilize FELIX software to configure FEC hardware
- Complete the chain of SRO
  - TIDIS SRO Prototype ➔ Router ➔ JANA2 Subscriber ➔ JupyterLab
- Special thanks to: E. Jastrzembski, J. Wilson, A. Hellman, C. Long, et al.
Streaming Readout Grand Challenge

Questions?
Backup Slides
TDIS SRO Test Stand Setup

75/25 Ar/CO₂ Gas System

NIM Cosmic Trigger

HV Power Supplies

Isolation Transformer
TIDIS SRO Test Stand Setup

Cosmic Test Stand

FEC LV Power Supply

ALICE FEC’s (x5)

GEM Detector

Trigger PMTs
Traditional triggered readout

- data is digitized into buffers and a trigger, per event, starts readout
- parts of events are transported through the DAQ to an event builder where they are assembled into events
- **event selection** based on fast detectors with coarse resolution

*default at JLab experiments*

Streaming readout

- data is read continuously from all channels
- data then flows unimpeded in parallel channels to storage or a local compute resource
- **event selection** based on full detector information

*intended for TDIS, SoLid, EIC*
TDIS Streaming Readout Prototype

Data Processor
- assembles the data into events
- outputs data suitable for final analysis (Analysis data)

Features (among others)
- ideal for machine learning
- automated calibration and alignment
- partial or full event reconstruction
- event selection and/or labeling into analysis streams
- automated anomaly detection
- responsive detectors (conscious experiment)

Real-Time Processing
Simple feature-building, e.g. in FPGAs, required to reduce the data rate.


Full real-time reconstruction for all particles available to select events.

Data buffered on 10 PB of disk.

Real-time reconstruction for all charged particles with pT > 0.5 GeV.

0.7 GB/s (mix of full + partial events)

Real-time calibration & alignment.

1 TB/s post zero suppression
50 GB/s
1 MHz

JINST 8 (2013) P04022

LHCb Example

Slide Courtesy of M. Diefenthaler
07/09/2019

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## ALICE SAMPA Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>TPC</th>
<th>MCH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage supply</td>
<td>1.25 V</td>
<td>1.25 V</td>
</tr>
<tr>
<td>Polarity</td>
<td>Negative</td>
<td>Positive</td>
</tr>
<tr>
<td>Detector capacitance (Cd)</td>
<td>18.5 pF</td>
<td>40 pF - 80 pF</td>
</tr>
<tr>
<td>Peaking time (ts)</td>
<td>160 ns</td>
<td>300 ns</td>
</tr>
<tr>
<td>Shaping order</td>
<td>4th</td>
<td>4th</td>
</tr>
<tr>
<td>Equivalent Noise Charge (ENC)</td>
<td>&lt; 600e@ts=160 ns*</td>
<td>&lt; 950e @ Cd=40 pF* &lt; 1600e @ Cd=80 pF*</td>
</tr>
<tr>
<td>Linear Range</td>
<td>100 fC or 67 fC</td>
<td>500 fC</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>20 mV/fC or 30 mV/fC</td>
<td>4 mV/fC</td>
</tr>
<tr>
<td>Non-Linearity (CSA + Shaper)</td>
<td>&lt; 1%</td>
<td>&lt; 1%</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>&lt; 0.3%@ts=160 ns</td>
<td>&lt; 0.2%@ts=300 ns</td>
</tr>
<tr>
<td>ADC effective input range</td>
<td>2 Vpp</td>
<td>2 Vpp</td>
</tr>
<tr>
<td>ADC resolution</td>
<td>10-bit</td>
<td>10-bit</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>10 (20) Msamples/s</td>
<td>10 Msamples/s</td>
</tr>
<tr>
<td>INL (ADC)</td>
<td>&lt;0.65 LSB</td>
<td>&lt;0.65 LSB</td>
</tr>
<tr>
<td>DNL (ADC)</td>
<td>&lt;0.6 LSB</td>
<td>&lt;0.6 LSB</td>
</tr>
<tr>
<td>ENOB (ADC)**</td>
<td>&gt; 9.2-bit</td>
<td>&gt; 9.2-bit</td>
</tr>
<tr>
<td>Power consumption (per channel)</td>
<td>&lt; 15 mW</td>
<td>&lt; 15 mW</td>
</tr>
<tr>
<td>CSA + Shaper + ADC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channels per chip</td>
<td>32</td>
<td>32</td>
</tr>
</tbody>
</table>

\*R_{esd} = 70Ω
\**@ 0.5MHz, 10Msamples/s

Slide Courtesy of E. Jastrzembski
ALICE System

- FEC – Front End Card (160 ch / FEC)
- CRU – Common Readout Unit ~12 FECs / CRU = ~1920 ch / CRU
- DCS – Detector Control System
- LTU – Local Trigger Unit

Slide Courtesy of E. Jastrzembski
ALICE FEC (JLab Version)

GBTx0

GBTx1

SAMPA0

SAMPA4

VTRx

VTTx

40-pin signal connectors

GBT-SCA

Slide Courtesy of E. Jastrzembiski
C-RORC (Common Readout Receiver Card)

3x QSFP:
12 fast serial links connected to FPGA transceivers (GTX)
Up to 6.6 Gbps per channel

PCIe Gen2, 8 Lanes
8x 5.0 Gbps, connected to Xilinx PCIe Hard Block

(~ 30 Gb/s)

Xilinx Virtex-6 FPGA

Slide Courtesy of E. Jastrzembski