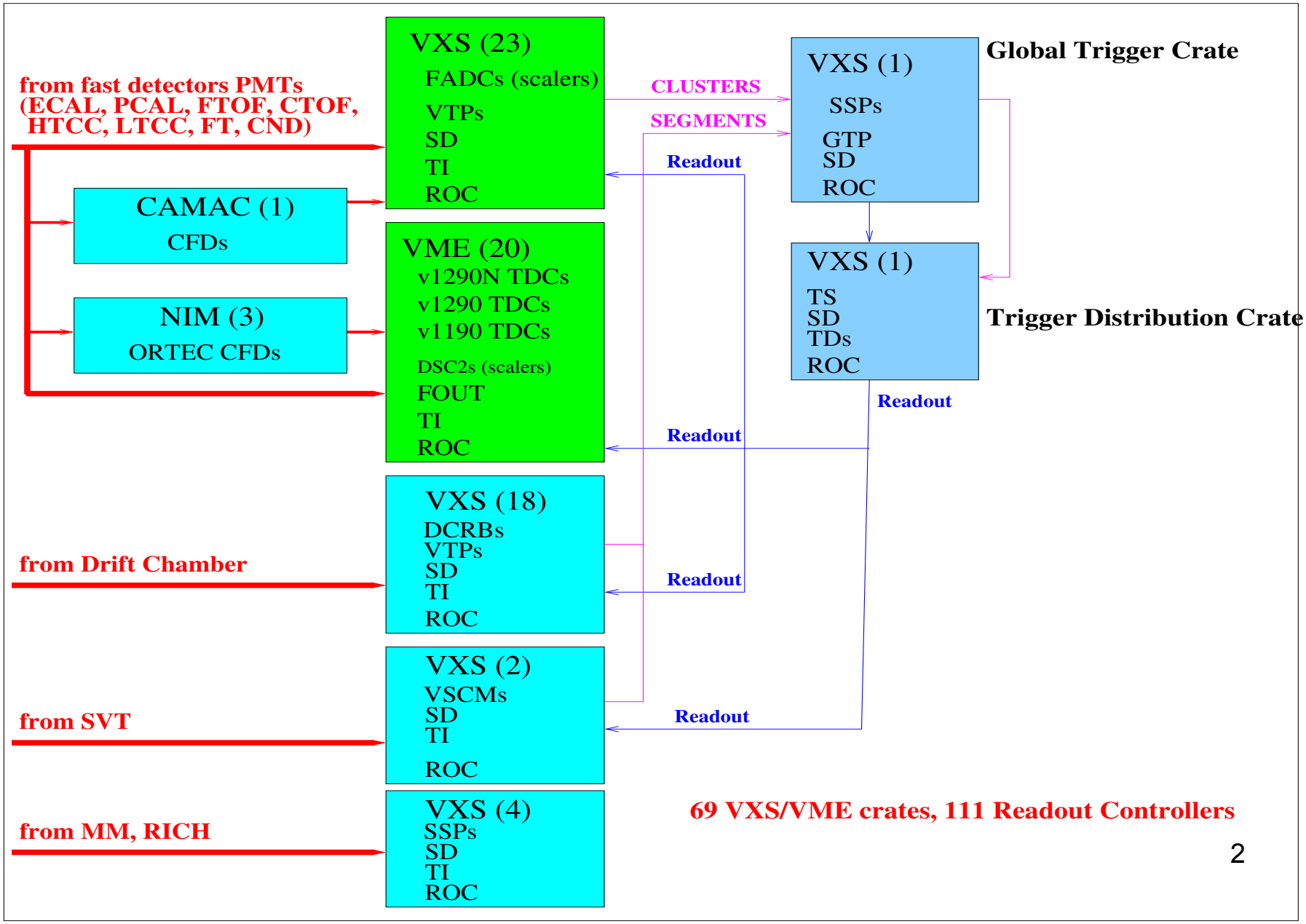
DAQ/Trigger Status

1. DAQ/Trigger systems overview
2. Performance and development since spring run

Sergey Boyarinov

Nov 14, 2018

DAQ/Trigger Hardware



Readout channels count

Detectors with dual outputs (FADCs and Discriminators/TDCs):

ECAL: 1296
PCAL: 1152
FTOF: 1080
CTOF: 96
CND: 144
HTCC: 48
LTCC: 144
=== 3,960 x 2 = 7,920

Detectors with single output:

Drift chamber:	24,192
SVT:	21,504
MM:	24,576
RICH:	25,024
FT:	564

=== 95,860

====== Total in CLAS12: 103,780

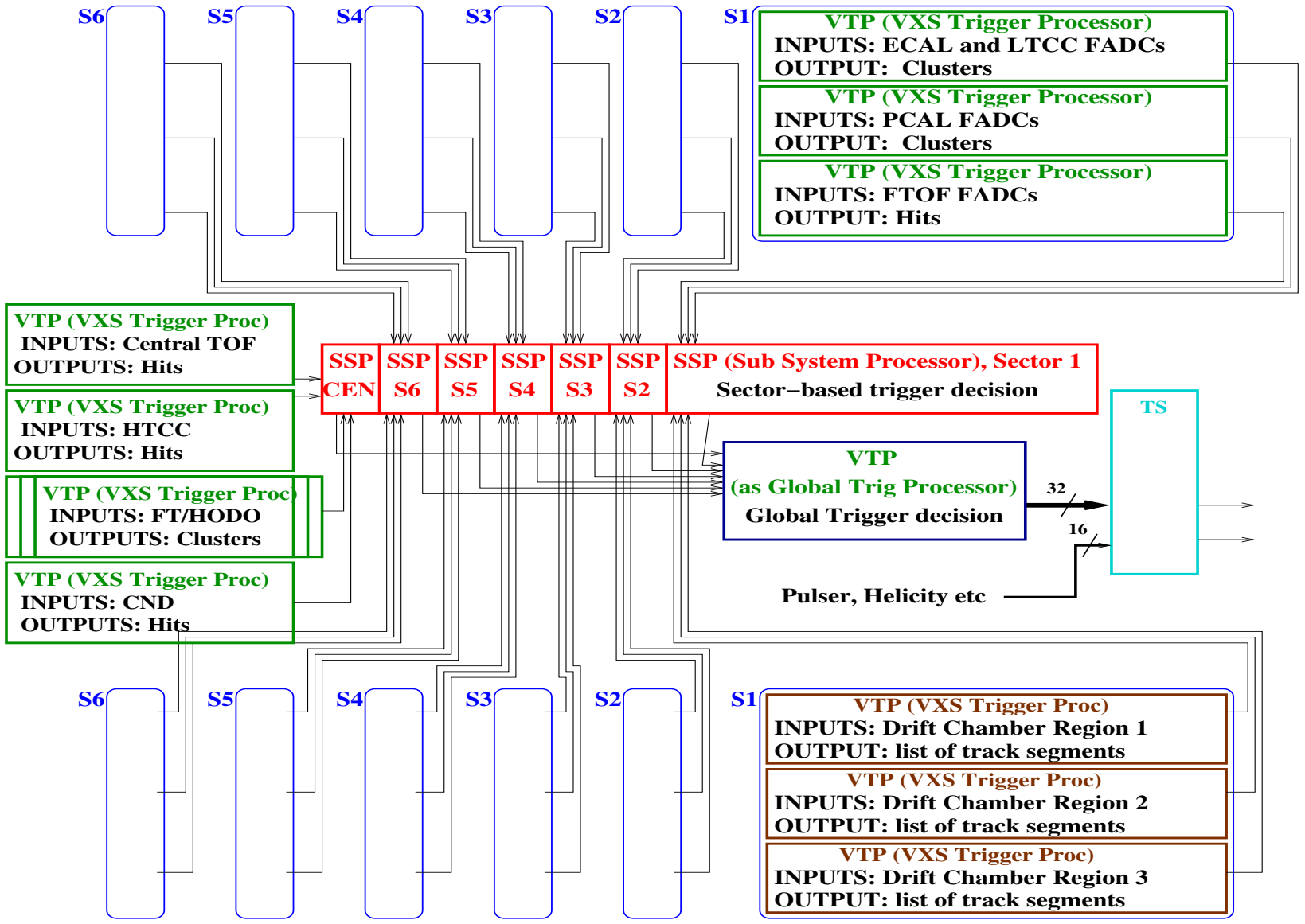
Most of channels have built-in scalers, they are reported to EPICS. Few channels are recorded into data stream (such as helicity-marked Faraday Cup)

In addition we have trigger system containing 42 VTP boards.
All but 2VTPs being read out.

CLAS12 DAQ Status

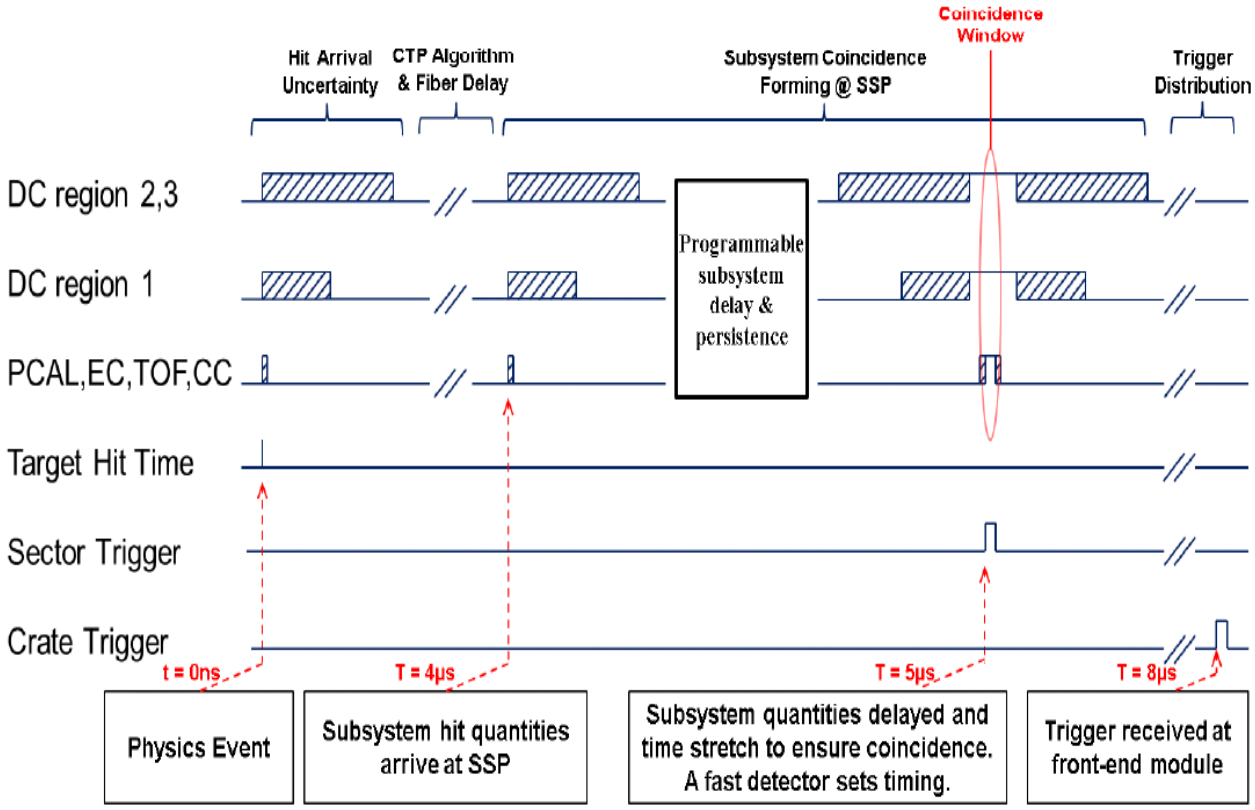
- Detectors supported: ECAL, PCAL, FTOF, LTCC, DC, HTCC, CTOF, CND, SVT, MM, FT/HODO, RICH, BAND in process of installation
- Online computer cluster: 30+ computers, 4 DAQ servers (2 in use and 2 hot swap)
- Networking: 1 router, 20+ switches, 40GBit to CC
- DAQ is operational, performance exceeded requirements, reliability is acceptable and improving

CLAS12 Trigger System Logic



CLAS12 Trigger Timing

- **~8us trigger Latency**
- **~10ns final trigger jitter (typical for HTCC & FTCAL timed triggers)**



CLAS12 Trigger Defintions (Sector/Central Stage 2)

8 Independent sector trigger bits can be defined:

- ECAL/PCAL Cluster Cuts
- FTOF1B, HTCC hit requirement
- PCAL-U x FTOF1B geometry matching
- DC superlayer hit multiplicity
- DC road requirement
- Coincidence width
- Detector skew (common to all sector trigger bits)

Configuration FIle:

```
#####################
#
# Sector Trigger bit 0
#
#   DC_INBEND x HTCC x (PCAL+ECAL)>300MeV x PCAL>60MeV x ECAL>10MeV
#####################
SSP_GT_STRG                         0
SSP_GT_STRG_EN                      1

# HTCC trigger logic
SSP_GT_STRG_HTCC_EN                 1
SSP_SLOT 3      # sector 1 SSP
SSP_GT_STRG_HTCC_MASK               0x0000000000FF
SSP_SLOT 4      # sector 2 SSP
SSP_GT_STRG_HTCC_MASK               0x00000000FF00
SSP_SLOT 5      # sector 3 SSP
SSP_GT_STRG_HTCC_MASK               0x000000FF0000
SSP_SLOT 6      # sector 4 SSP
SSP_GT_STRG_HTCC_MASK               0x0000FF000000
SSP_SLOT 7      # sector 5 SSP
SSP_GT_STRG_HTCC_MASK               0x00FF00000000
SSP_SLOT 8      # sector 6 SSP
SSP_GT_STRG_HTCC_MASK               0xFF0000000000
SSP_SLOT all
SSP_GT_STRG_HTCC_WIDTH              0

# PCAL cluster trigger logic
SSP_GT_STRG_PCAL_CLUSTER_EMIN_EN    1
SSP_GT_STRG_PCAL_CLUSTER_EMIN     600
```

8 Independent central trigger bits can be defined:

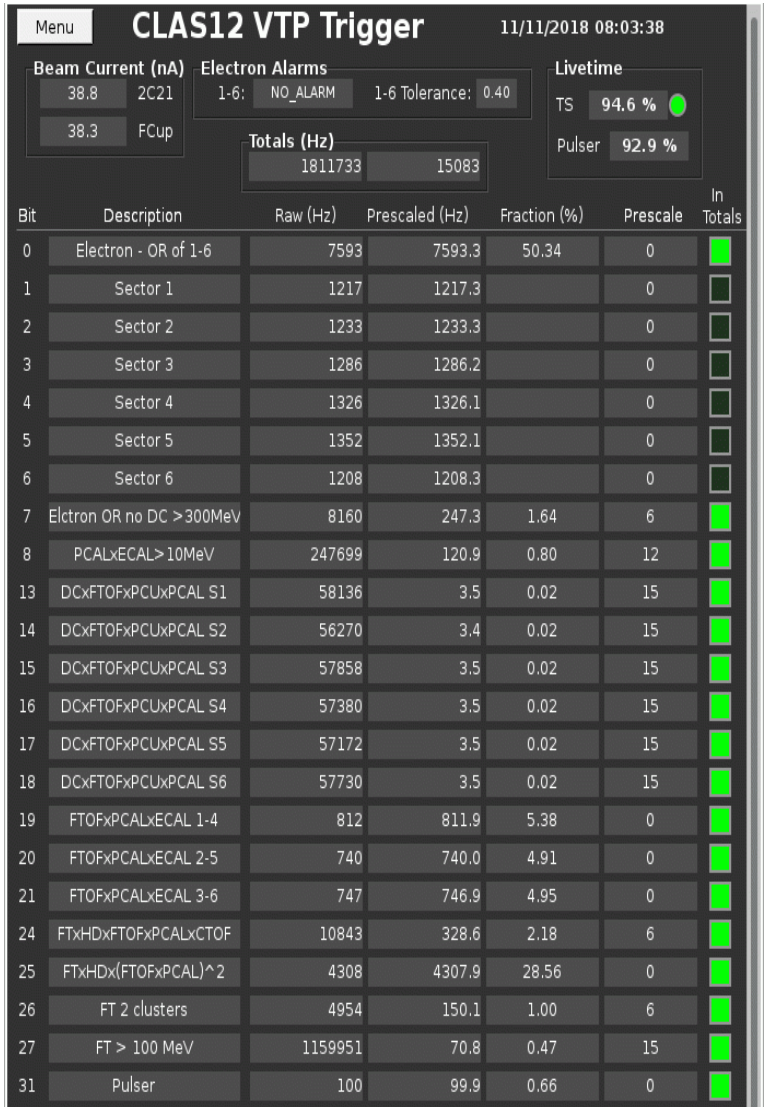
- Forward Tagger Cluster Cuts
- CND x CTOF geometry matching
- Coincidence width
- Detector skew (common to all central trigger bits)

Configuration FIle:

```
#####################
# Central Trigger bit 0    CTRG0:  FT(200-4000)xHD(2)
#####################
SSP_GTC_CTRG 0

SSP_GTC_CTRG_EN                     1
SSP_GTC_CTRG_FT_CLUSTER_EN          1
SSP_GTC_CTRG_FT_CLUSTER_EMIN        200
SSP_GTC_CTRG_FT_CLUSTER_EMAX        4000
SSP_GTC_CTRG_FT_CLUSTER_HODO_NMIN   2
SSP_GTC_CTRG_FT_CLUSTER_NMIN        1
SSP_GTC_CTRG_FT_CLUSTER_WIDTH       0
SSP_GTC_CTRG_FT_ESUM_EN             0
SSP_GTC_CTRG_FT_ESUM_EMIN           0
SSP_GTC_CTRG_FT_ESUM_WIDTH          0


#####################
# Central Trigger bit 1    CTRG1:  FT(500-8500) 2 clusters
#####################
SSP_GTC_CTRG                        1
SSP_GTC_CTRG_EN                     1

SSP_GTC_CTRG_FT_CLUSTER_MULT_EN            1
SSP_GTC_CTRG_FT_CLUSTER_MULT_COINCIDENCE   16
SSP_GTC_CTRG_FT_CLUSTER_MULT_MIN           2

SSP_GTC_CTRG_FT_CLUSTER_EMIN             500
SSP_GTC_CTRG_FT_CLUSTER_EMAX            8500
```

CLAS12 Trigger Definitions (Global – Stage 3)

ActiveMQ to EPICS:



Bit	Description	Raw (Hz)	Prescaled (Hz)	Fraction (%)	Prescale	In Totals
0	Electron - OR of 1-6	7593	7593.3	50.34	0	
1	Sector 1	1217	1217.3		0	
2	Sector 2	1233	1233.3		0	
3	Sector 3	1286	1286.2		0	
4	Sector 4	1326	1326.1		0	
5	Sector 5	1352	1352.1		0	
6	Sector 6	1208	1208.3		0	
7	Elctron OR no DC >300MeV	8160	247.3	1.64	6	
8	PCALxECAL>10MeV	247699	120.9	0.80	12	
13	DCxFTOFxPCUxPCAL S1	58136	3.5	0.02	15	
14	DCxFTOFxPCUxPCAL S2	56270	3.4	0.02	15	
15	DCxFTOFxPCUxPCAL S3	57858	3.5	0.02	15	
16	DCxFTOFxPCUxPCAL S4	57380	3.5	0.02	15	
17	DCxFTOFxPCUxPCAL S5	57172	3.5	0.02	15	
18	DCxFTOFxPCUxPCAL S6	57730	3.5	0.02	15	
19	FTOFxPCALxECAL 1-4	812	811.9	5.38	0	
20	FTOFxPCALxECAL 2-5	740	740.0	4.91	0	
21	FTOFxPCALxECAL 3-6	747	746.9	4.95	0	
24	FTxHDxFTOFxPCALxCTOF	10843	328.6	2.18	6	
25	FTxHDx(FTOFxPCAL)^2	4308	4307.9	28.56	0	
26	FT 2 clusters	4954	150.1	1.00	6	
27	FT > 100 MeV	1159951	70.8	0.47	15	
31	Pulser	100	99.9	0.66	0	

Electro-production (bits 0-6)

Muon (bits 19-21)

MesonX (bit 25)

32 Independent trigger bits can be defined:

- Sector Trigger Mask
- Sector Mask
- Sector Multiplicity
- Central Trigger Mask
- Multiplicity Coincidence Window
- Delay
- Prescale factor (done on Trigger Supervisor)

Configuration FIle:

```
# TRIGGER BITS:
#              trig number
#              |   ssp trig mask
#              |   |   ssp sector mask
#              |   |   |  multiplicity
#              |   |   |  |  coincidence=#extended_clock_cycles
#              |   |   |  |  |  ssp central trig mask
#              |   |   |  |  |  |  delay(in 4ns ticks)
#              |   |   |  |  |  |  |
#
# Electron, All Sectors with DC
VTP_GT_TRGBIT  0   3  63  1  1  0  0  # SSP STRG0|STRG1, SECTOR 1-6

# Electron, Individual Sectors with DC Roads
VTP_GT_TRGBIT  1   3   1  1  1  0  0  # SSP STRG0|STRG1, SECTOR 1
VTP_GT_TRGBIT  2   3   2  1  1  0  0  # SSP STRG0|STRG1, SECTOR 2
VTP_GT_TRGBIT  3   3   4  1  1  0  0  # SSP STRG0|STRG1, SECTOR 3
VTP_GT_TRGBIT  4   3   8  1  1  0  0  # SSP STRG0|STRG1, SECTOR 4
VTP_GT_TRGBIT  5   3  16  1  1  0  0  # SSP STRG0|STRG1, SECTOR 5
VTP_GT_TRGBIT  6   3  32  1  1  0  0  # SSP STRG0|STRG1, SECTOR 6

# Electron, All sectors without DC_INBEND
VTP_GT_TRGBIT  7  96  63  1  1  0  0  # SSP STRG5|STRG6, SECTOR 1-6

# PCAL(>10)xECAL(>10 MeV) All sectors without DC
VTP_GT_TRGBIT  8 128  63  1  1  0  0  # SSP STRG7, SECTOR 1-6
```

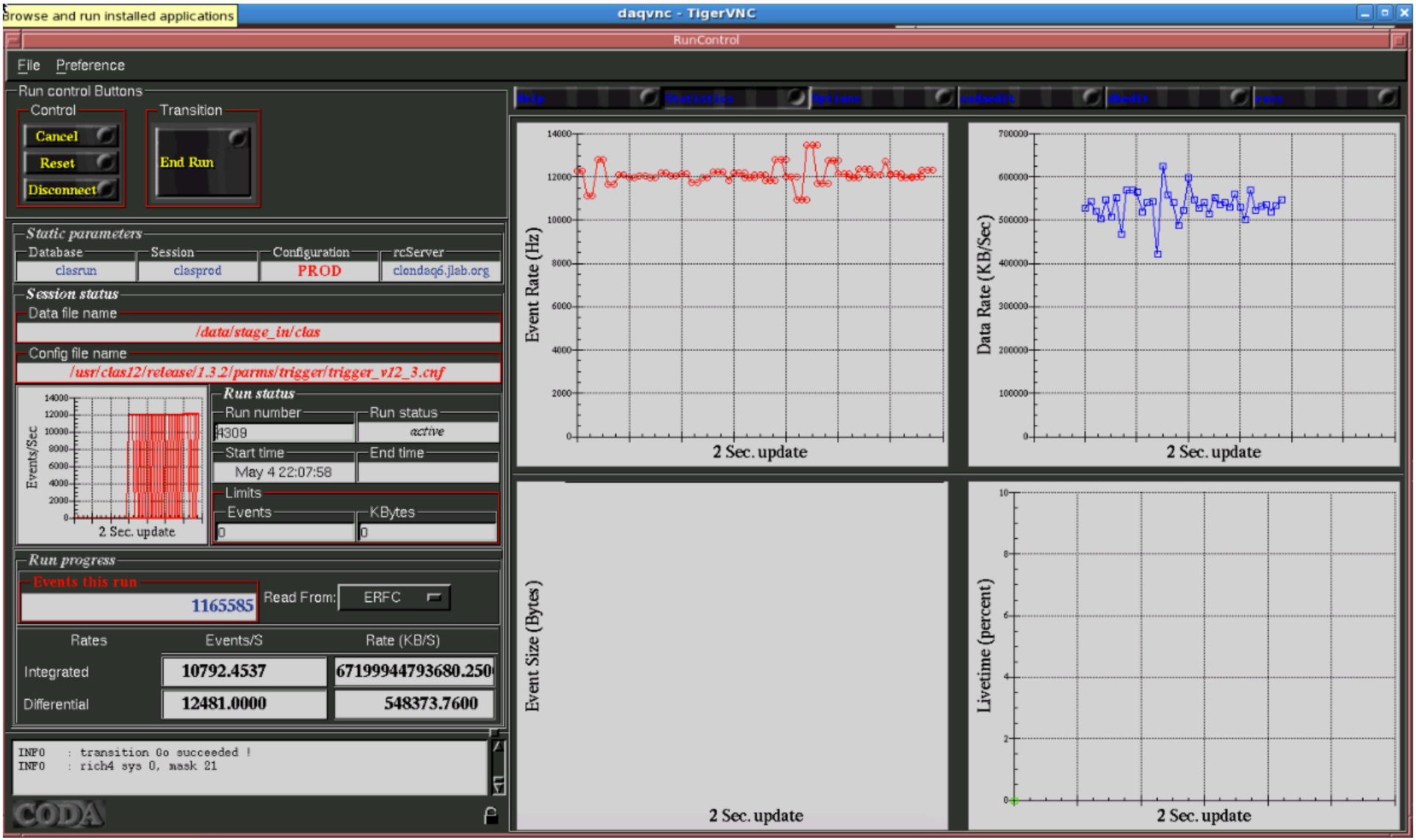
Online System Status

- Available computing hardware is sufficient; bigger data server installed and in commissioning stage (to satisfy 24-hour data buffering requirement)
- Available software: process monitoring and control, CLAS event display, data collection from different sources (DAQ, EPICS, scalers etc) and data recording into data stream, online data monitoring
- Runtime database (RCDB) is running
- ActiveMQ messaging system is running
- ‘Online farm’ issue to be resolved, ‘farm in CC’ option did not work, we started to build one in counting room, 3 machines installed + 3 will be added soon, ready for CLARA installation − work in progress

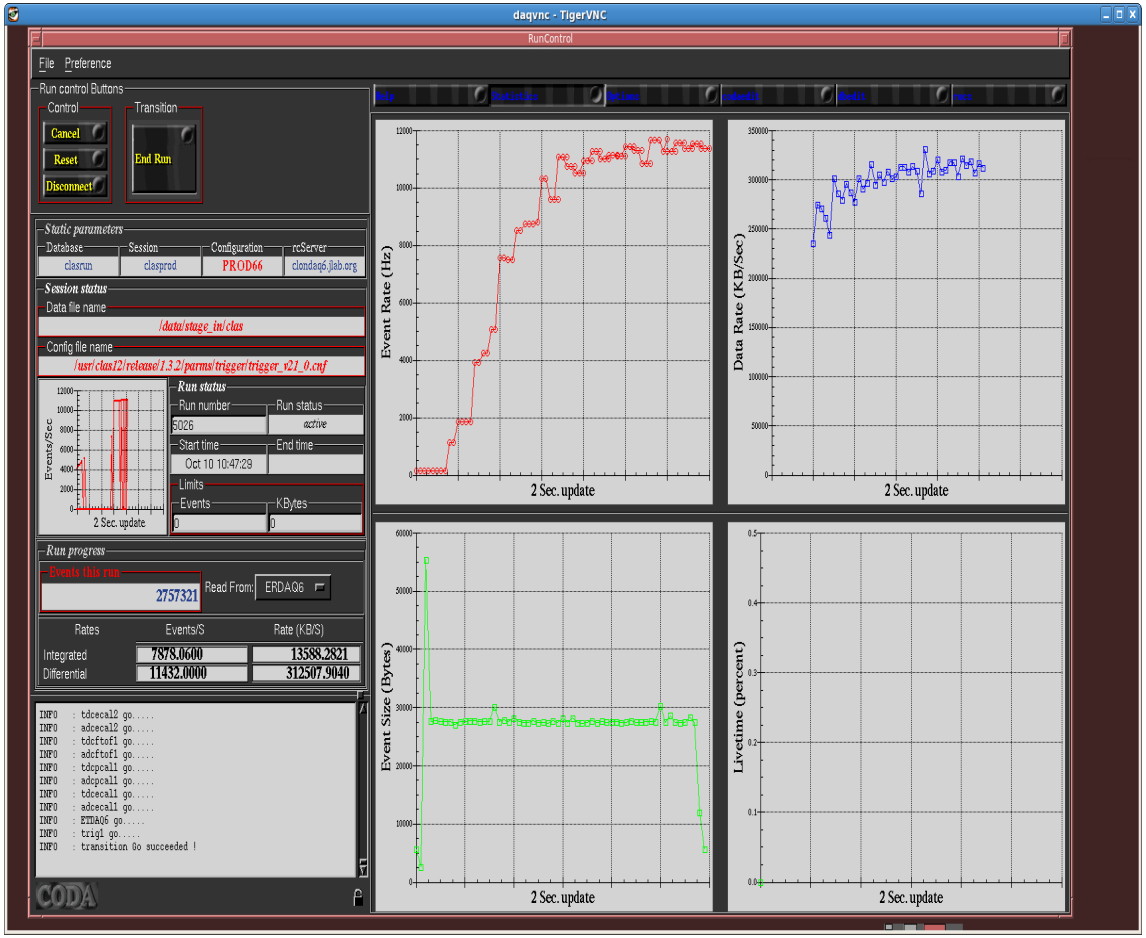
DAQ/Trigger/Online Summary

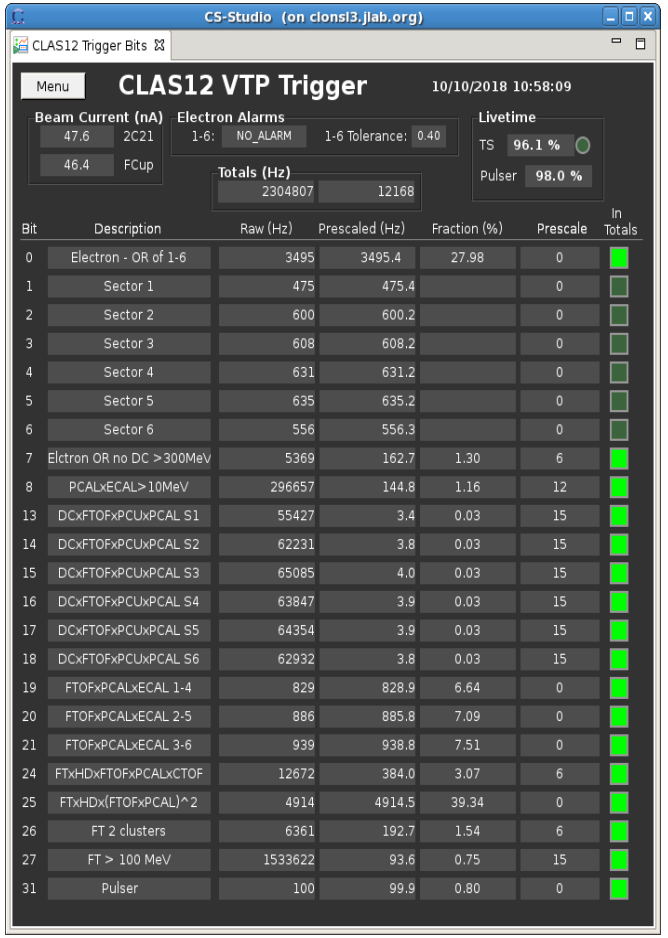
- DAQ/Trigger/Online systems are operational
- Systems are well supported by Hall B team (Sergey Boyarinov and Nathan Baltzell as first line of support, Valery Kubarovsky and Andrea Celentano from run group on trigger settings, and at least one person from every detector group for configuration and data monitoring including outside groups
- DAQ and Trigger systems are well supported by JLAB CODA and Fast Electronics Groups, in particular Ben Raydo and Bryan Moffit for trigger system and front-end libraries

DAQ performance: spring run 50nA beam − 12kHz, 600MB/s, 94% livetime

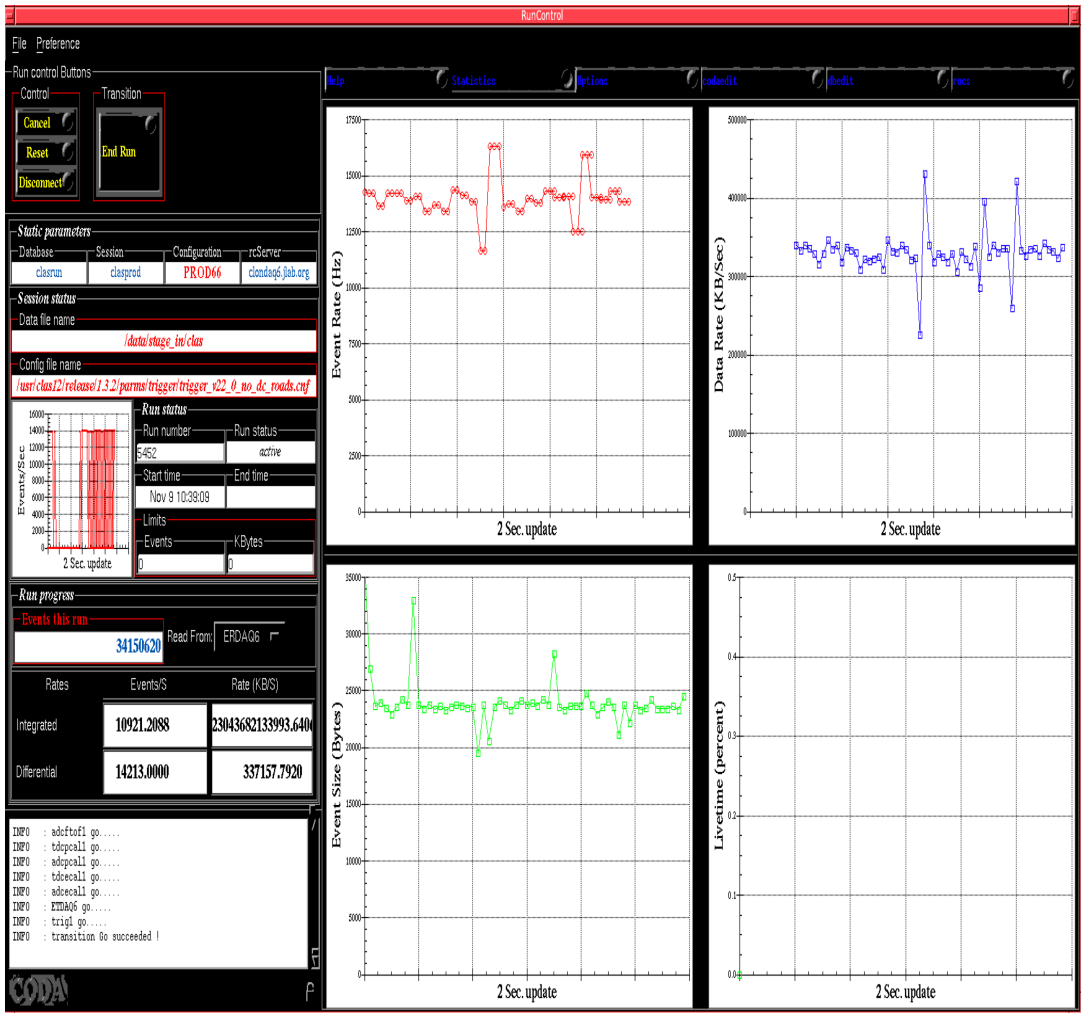


DAQ performance: fall run inbending 45nA beam − 12kHz, 300MB/s, 96% livetime

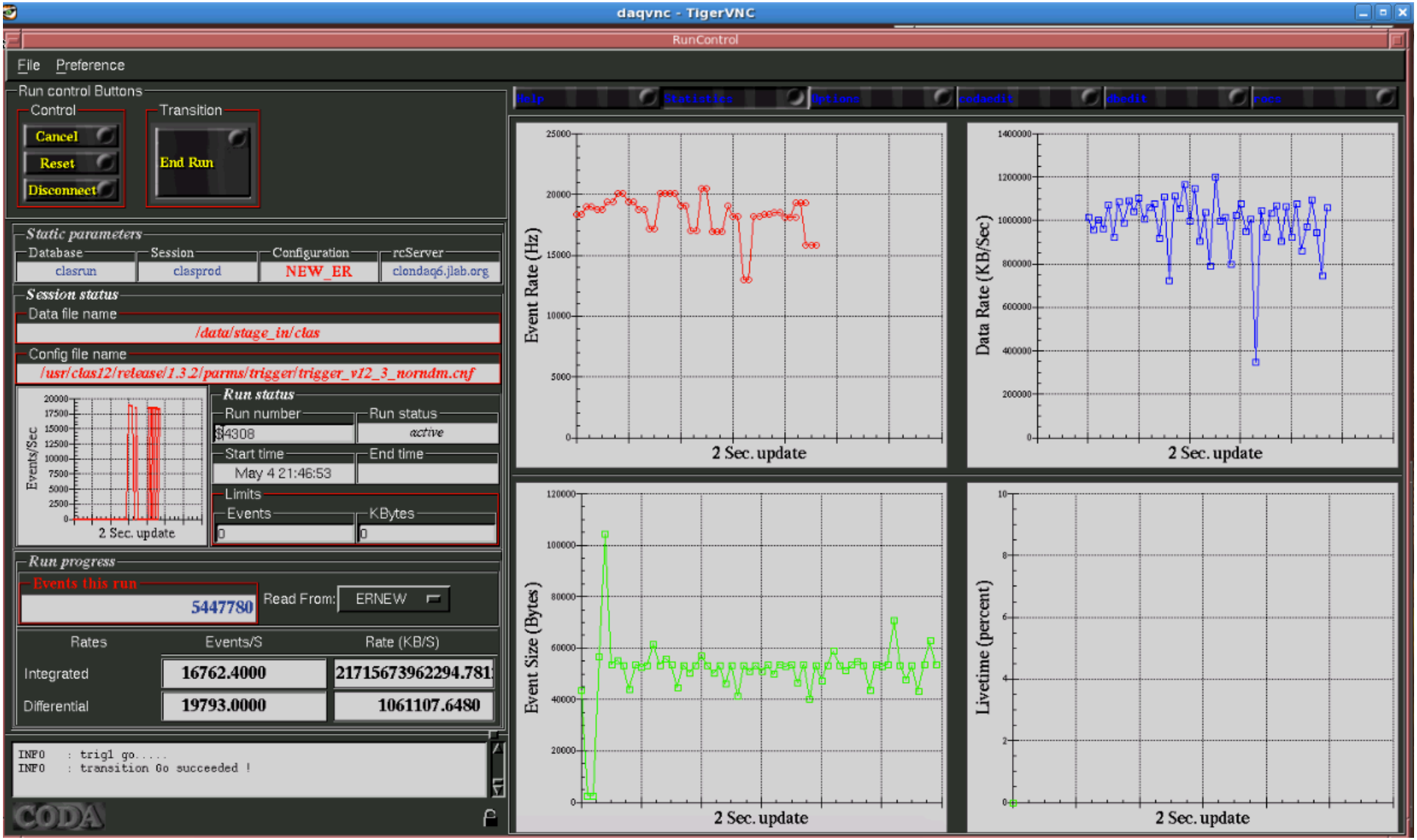




DAQ performance: fall run outbending 40nA beam − 14kHz, 330MB/s, 95% livetime



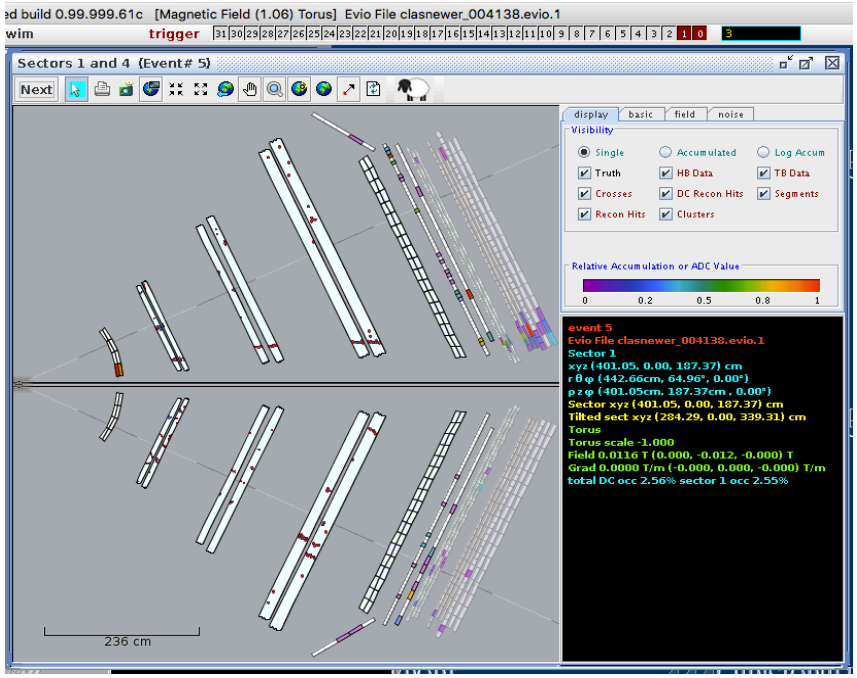
50nA beam daq test (some prescales removed), multi-stream
Event Recorder − 20kHz, 1000MB/s, 88% livetime



Activity between spring and fall runs

- Drift Chamber-based trigger improvement
- Geometry match between different detectors participating in trigger
- FADC data reduction
- MM data reduction
- Fix remaining DAQ and Trigger Issues, mostly related to reliability
- CAEN TDC calibration
- Trigger logic improvements
- Online Farm construction

CLAS12 Drift Chamber-based trigger



- Stage1a: segment finder (based of segment dictionary) in each of 6 superlayers; every superlayer has 6 layers, trigger requires at least 4 layers to have hits
- Stage1b: segments multiplicity (5 out of 6 superlayers must have segments), or road finder (based on road dictionary)
- Stage2: timing (and possible geometry) coincidence with other detectors

- Segment dictionary and road dictionary generated using CLAS12 simulation and reconstruction software
- VHDL code generated from segment/road dictionaries using C-based generator program
- VHDL code incorporated into VTP FPGAs
- Trigger validation performed using beam data with trigger from random pulser
- DC-based trigger decreases event rate up to 30% depending on run conditions, with efficiency close to 100% for electrons with momentum above 1GeV
- In particular, road finder gives extra 10-12% event rate decrease for inbending electrons in compare with segments multiplicity, but only 2-3% for outbending electrons; it is mostly efficient for noisy events where segment multiplicity alone does not work very well

Geometry match between different detectors participating in trigger

- Currently trigger has two geometry matches: Forward Tagger ECAL − Hodoscope, and Forward TOF − Preshower Calorimeter U plane
- With Drift Chamber road finder implemented, geometry match between Drift Chamber track and forward detectors (FTOF hits, PCAL clusters, ECAL clusters) can be included into trigger logic
- DCroads x FTOF and DCroads x PCALU match is in road dictionary, but not in firmware yet

FADC data reduction

- Running in raw mode, FADC data makes 2/3 of overall data traffic
- Plan was to use bit packing algorithm
- C implementation was tested on CLAS12 data, showing more then 2.5 times FADC data size reduction, and it takes up to 40us per event on CLAS12 VME controllers
- C code was passed to CODA and Fast Electronics Groups to be implemented into FADC hardware
- It was implemented by Hai Dong, Ed Jastrzembski and Ben Raydo, allowing to switch between unpacked mode, packed mode and verify mode
- Actual data size reduction achieved about factor 2

MM data reduction

- Micromega data is second largest contributor into event size after FADCs, it creates about 25% of overall data traffic
- Reason for high data rate is that there is no sparsification, and it seems impossible to implement it in current readout design
- Bit packing mechanism was suggested
- MM group worked to implement it; was implemented into second readout list, reduction achieved about 15-20%
- In addition, section of MM was removed decreasing data rate even more

Other Completed Tasks

- Fix most problems in DAQ front end responsible for occasional crashes, in particular long-standing TI firmware reload issue
- Fix broken VTP boards and improve VTP readout protocol
- Added more monitoring and control components (readout from all VTP boards, more detailed logs from various components to help DAQ/Trigger crashes debugging
- Trigger timing was set more precisely, allowing to decrease readout windows and additionally reduce event size
- Move-to-silo process now initiated every 10 minutes reading data in parallel with writing from the same partition; data file names were changed allowing alphabet sorting; subdirectories for every run being created – all that allows scicomp to optimize tape recording process
- CAEN TDC calibration was performed for all high resolution V1290 boards
- New RF board installed
- BAND detector installation in progress, one crate with FADCs, TDCs and hit-based trigger is operational, waiting for remaining hardware

Critical hardware purchases

- 6 TD boards − delivered, will be installed in January
- 6 old TD->TI conversion − will be done in January
- Fix broken VTPs − done
- More FADCs and SDs − in process
- 4 VXS crates − purchased, to be delivered soon
- 4 VME CPUs − delivered
- Event recorder server − delivered, installation is in process

DAQ/Trigger improvements summary

- Event size was decreased by factor 1.8 using FADC and MM bit packing and optimization of readout windows, from previous 45KB to about 25KB
- Event rate was reduced by improving trigger purity by about 15%
- As result we have now event rate for typical luminosity of 12-14kHz, and data rate reduced to 300-330MB/sec from previous 550-600MB/s
- The number of problems in DAQ front end firmwares and libraries were fixed, resulting in more stable running; that work continues
- All critical spare equipment components were ordered and most of them received, including data server to satisfy 24-hour buffer; move-to-tape process was optimized in according to scicomp recommendations

Conclusion

- DAQ, computing and network works as expected meeting current performance requirements
- Reliability improved but some problems still remains − work in progress
- DAQ is not a bottleneck and has significant headroom for both event rate (factor 1.5) and data rates (factor 3), and has a potential for future performance increases
- Trigger system works as expected; trigger structure can be modified on demand to meet upcoming experiments requirements
- Online software is operational, available tools allows to run; online farm still in construction stage