Design Study for a sPHENIX based EIC Detector

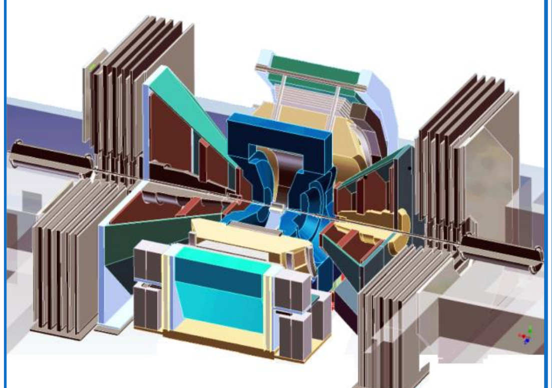
Progress on streaming demonstrations for EIC

Jin Huang (BNL)

Evolution of the RHIC 1008 Interaction region

PHENIX experiment

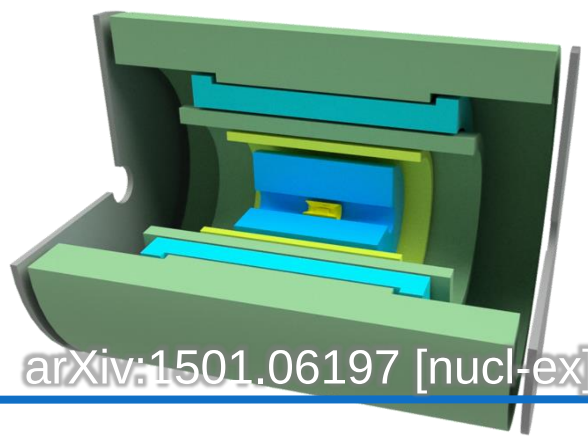
- 16y+ operation
- Broad spectrum of physics 180+ physics papers with 25k citations
- 1.4-M channel streaming



~2000

sPHENIX

- Comprehensive central upgrade base on previous BaBar magnet
- Rich jet and HF physics program
  → Microscopic nature of QGP

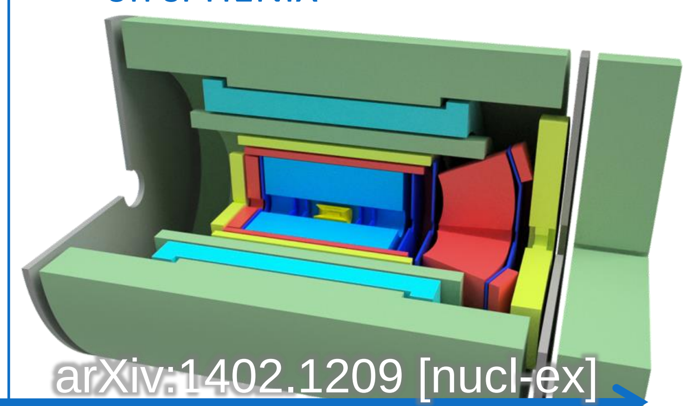


arXiv:1501.06197 [nucl-ex]

2017→2023, CD-1/3A Approved

An EIC detector

- Path of PHENIX upgrade leads to a capable EIC detector
- Large coverage of tracking, calorimetry and PID
- Full streaming DAQ based on sPHENIX



arXiv:1402.1209 [nucl-ex]

Update: sPH-cQCD-2018-001

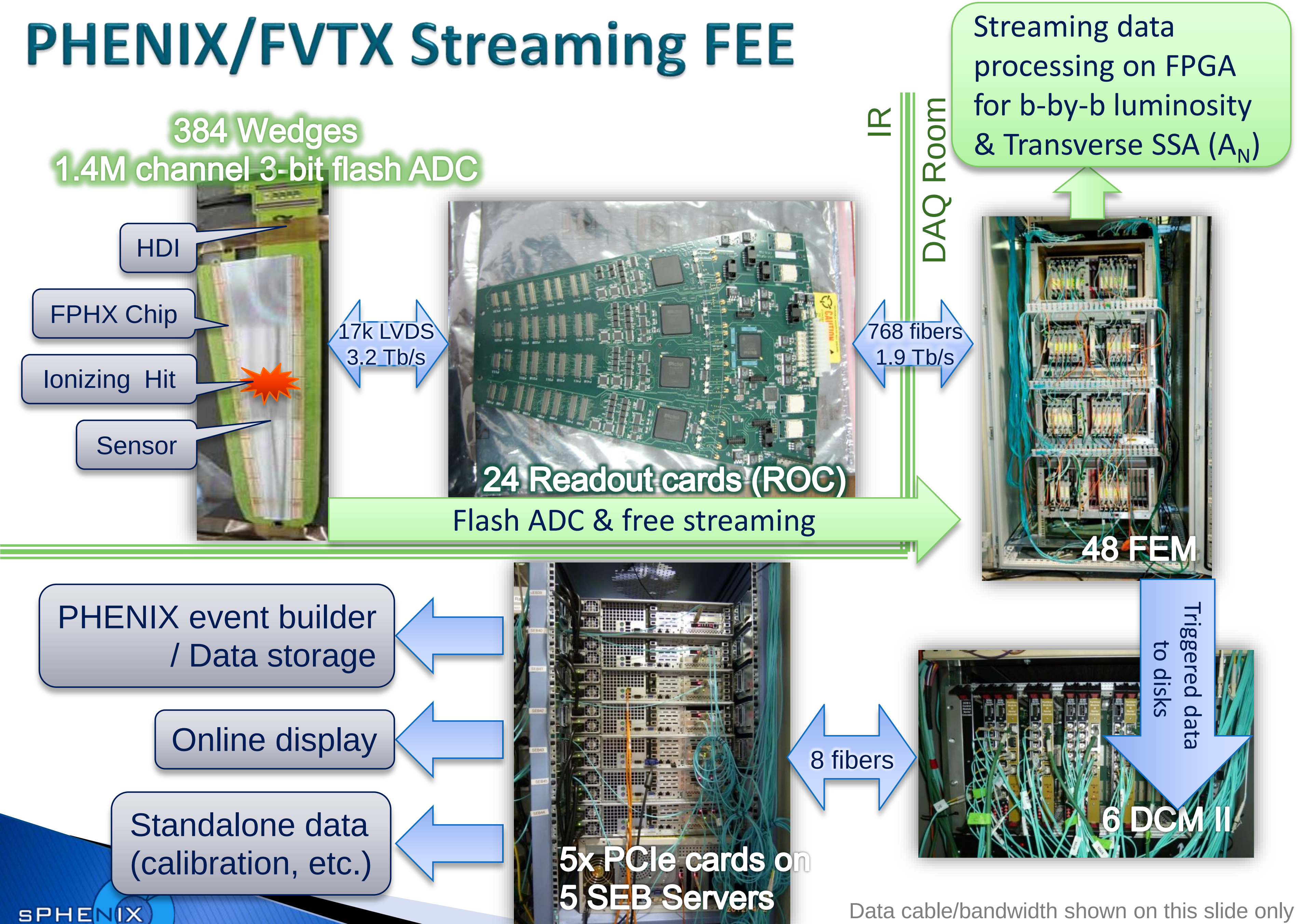
>2025

Time

RHIC: A+A, spin-polarized p+p, spin-polarized p+A

EIC: e+p, e+A

PHENIX/FVTX Streaming FEE

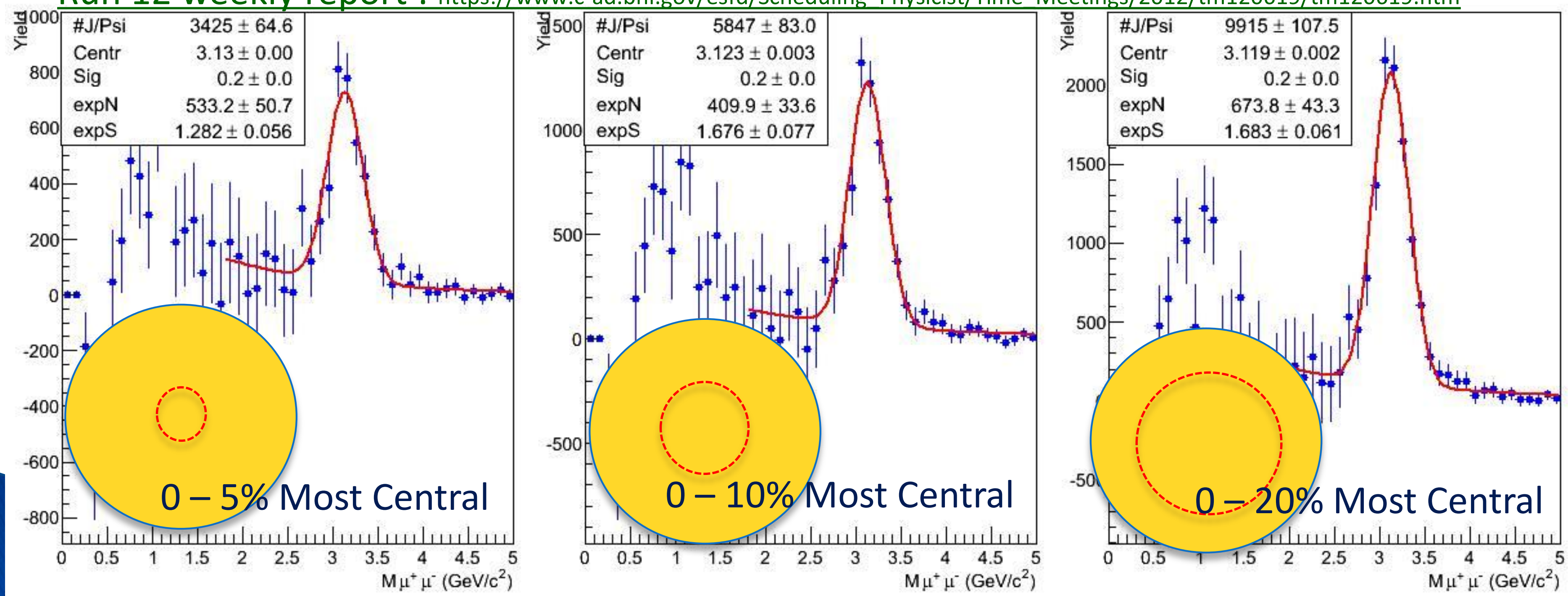


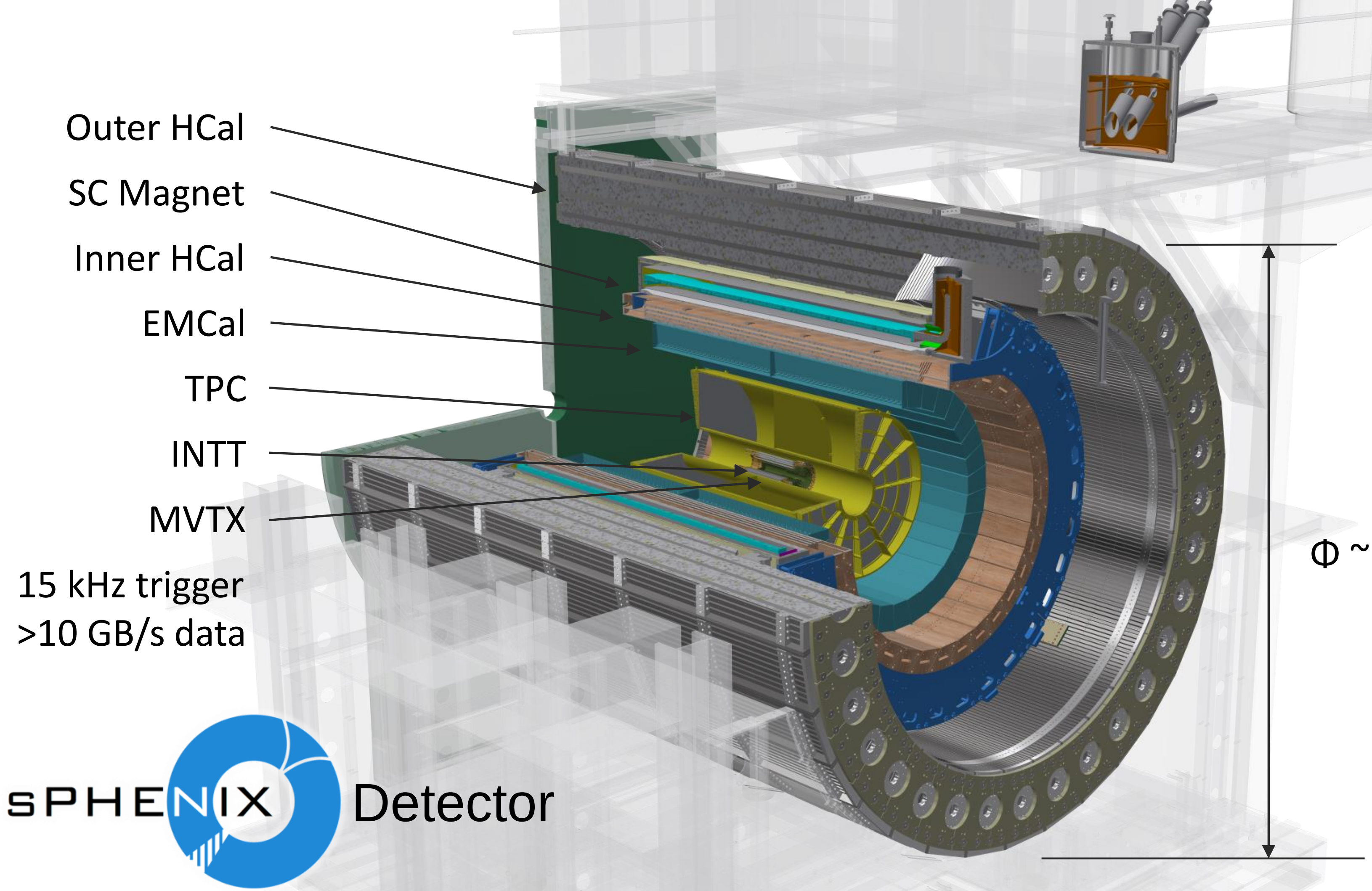
Data cable/bandwidth shown on this slide only

PHENIX Data validation & data processing in near-real-time

- PHENIX validate data and perform majority calibration in near-real-time via online system using a subset of raw data prior to disk write
- PHENIX has enough CPU to final process all data in real-time, but the limitation is usually special data need and manpower for calibration

J/Psi spectrum in Cu+Au @ sqrtS = 200 GeV via run-time data production & analysis, Run 12 weekly report : https://www.c-ad.bnl.gov/esfd/Scheduling_Physicist/Time_Meetings/2012/tm120619/tm120619.htm

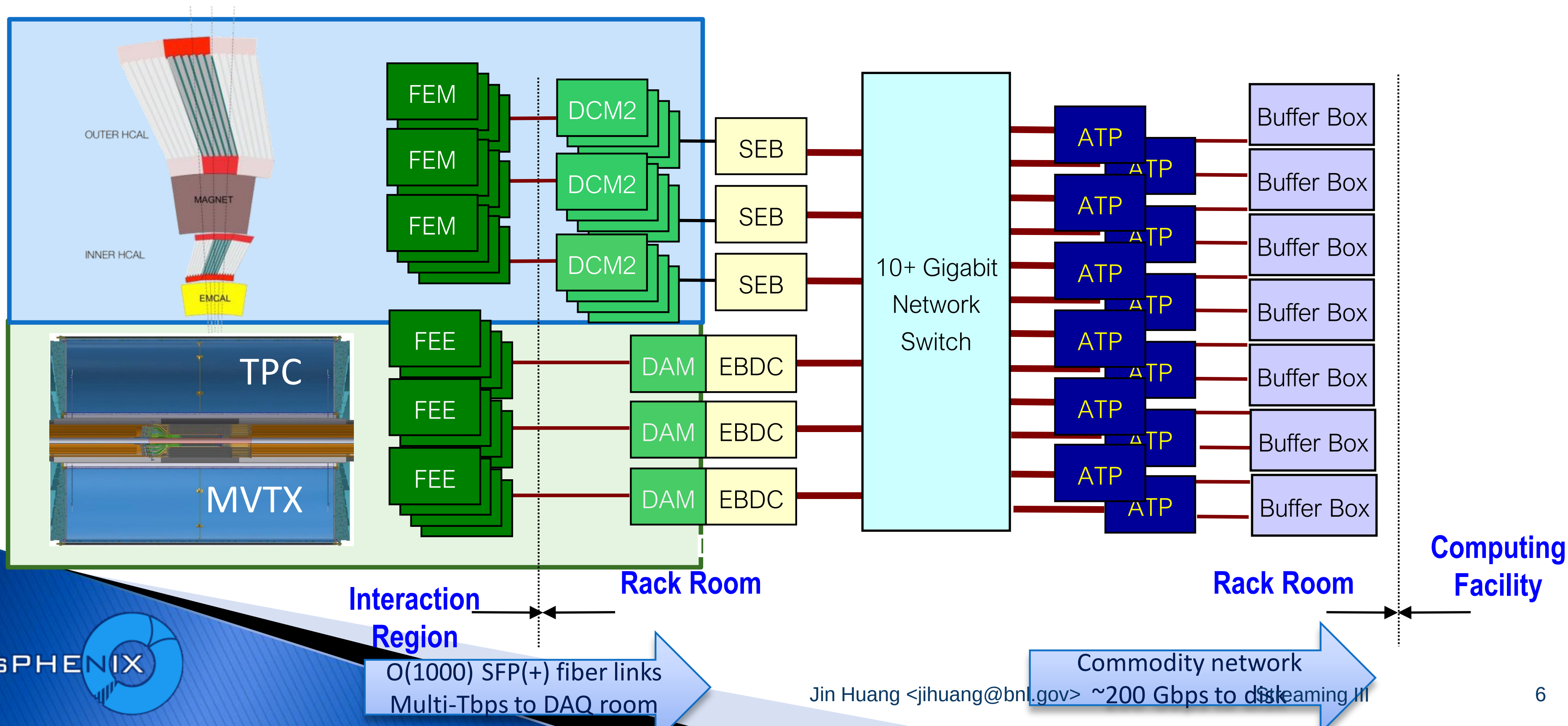




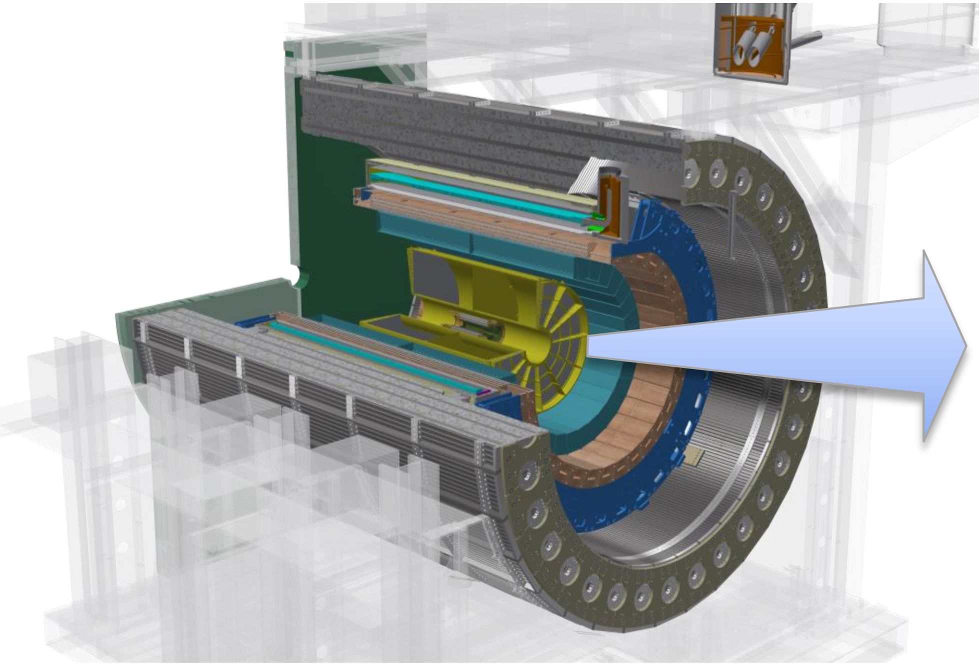
- 2016: Scientific review and DOE mission need Status (CD-0)
- 2018: Cost/schedule review and DOE approval for production start of long lead-time items (CD-1/3A)
- 2022: installation in RHIC 1008 Hall; 2023: First data
  - All tracker front end support streaming readout.
  - DAQ disk throughput for 9M particle/s + pile ups (> EIC ~4M particle/s)

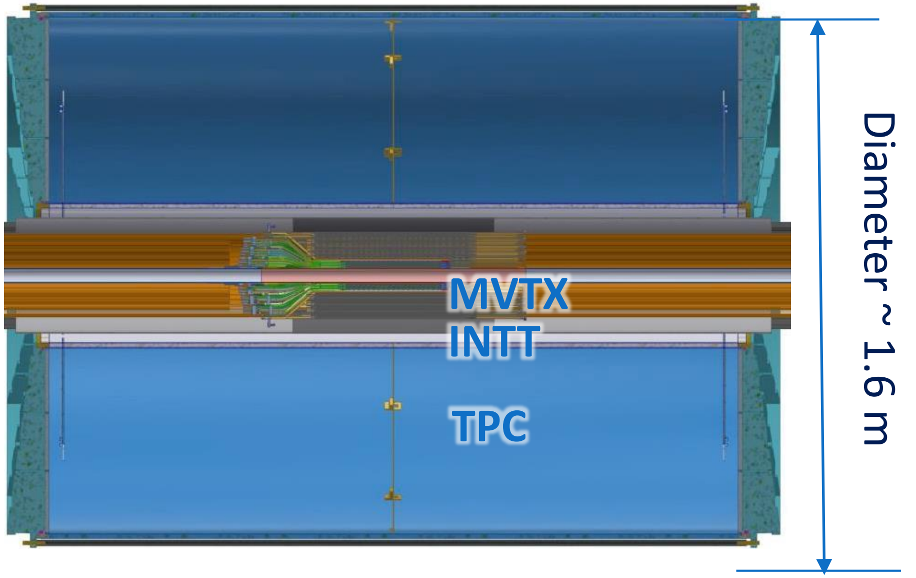
Selection of streaming and triggered front end

- **For calorimeter triggered FEE,**
  (signal collision rate 15kHz x signal span 200ns) << 1:
  No need for streaming readout which significantly reduce front-end transmission rate
- **For TPC and MVTX tracker FEE supports full streaming:**
  (signal collision rate 15kHz x integration time 10-20us) ~ 1:
  Streaming readout fits this scenario. Consider late stage data reduction by trigger-based filtering

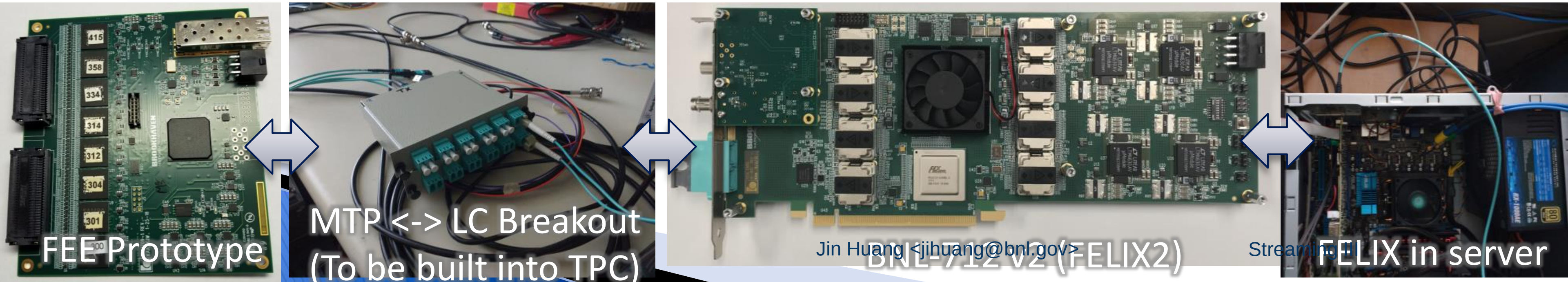


sPHENIX Time projection chamber (TPC)

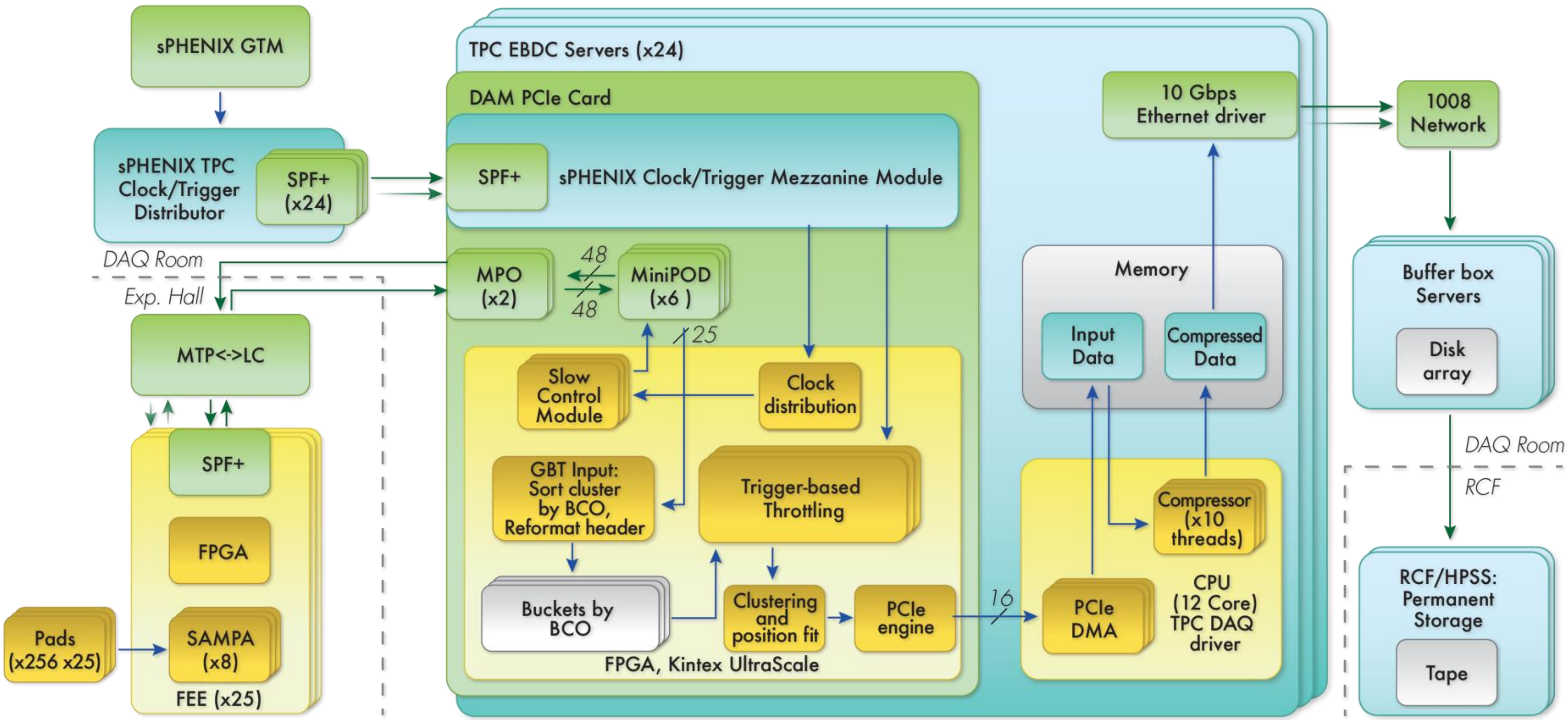




- Next-gen TPC w/ gateless and continuous readout: $\delta p/p < 2\%$ for p_T<10 GeV/c
- Ne-based gas for fast drift (13us). qGEM amplification and zigzag mini-pads.
- 160k channels 10b flash ADC @ 20MHz with SAMPA ASIC -> 2 Tbps stream rate.



TPC DAQ in streaming mode



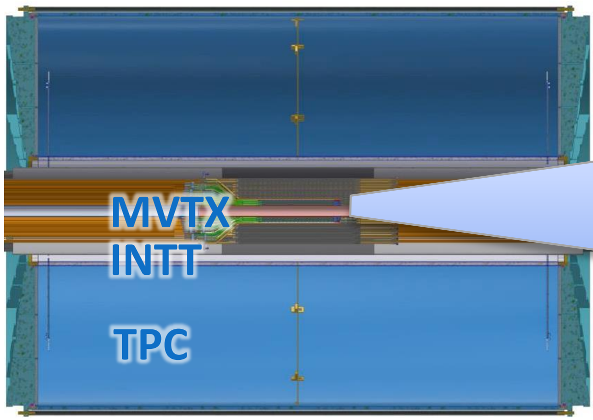
24 sectors, 144k Pads and 600 FEEs in total
1 sector, 25 FEEs per DAM for readout

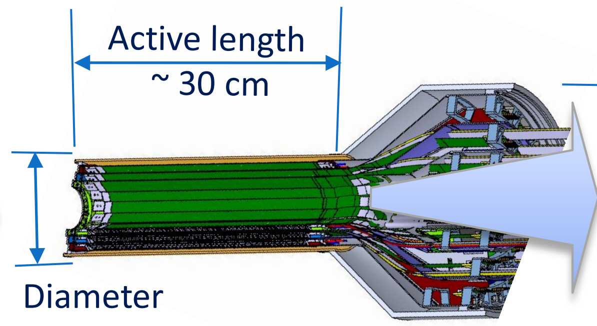
600 Fibers @ 600x 6 Gbps

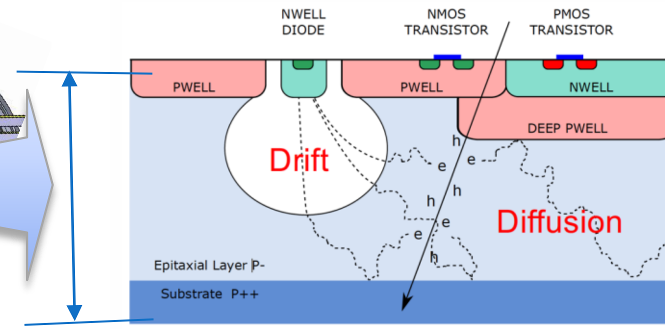
Commodity networking @ 200 Gbps

sPHENIX MVTX

- 200M pixel monolithic active pixel sensors (MAPS) vertex tracker (MVTX) → 5µm position resolution, 0.3% X0 / layer → <50 µ m DCA @ 1 GeV/c
- In close collaboration with ALICE & ATLAS phase-1 upgrades

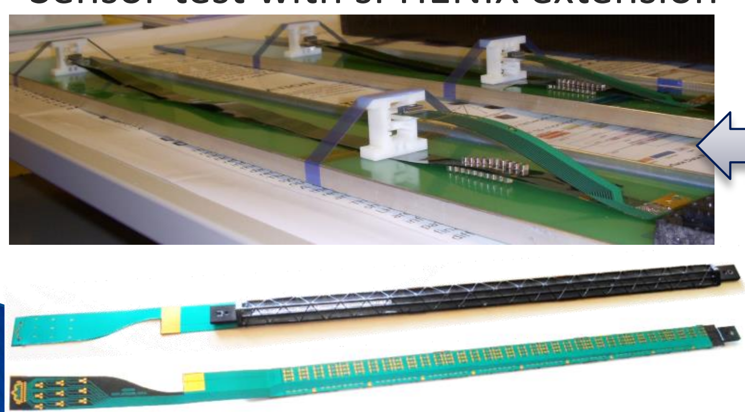




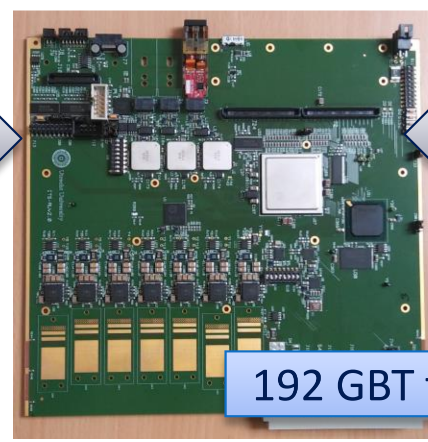


Thickness ~ 50 µm, 30x30 µm pixels

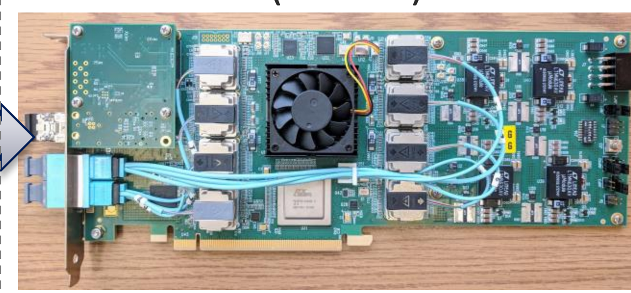
Sensor test with sPHENIX extension



Readout Unit v2



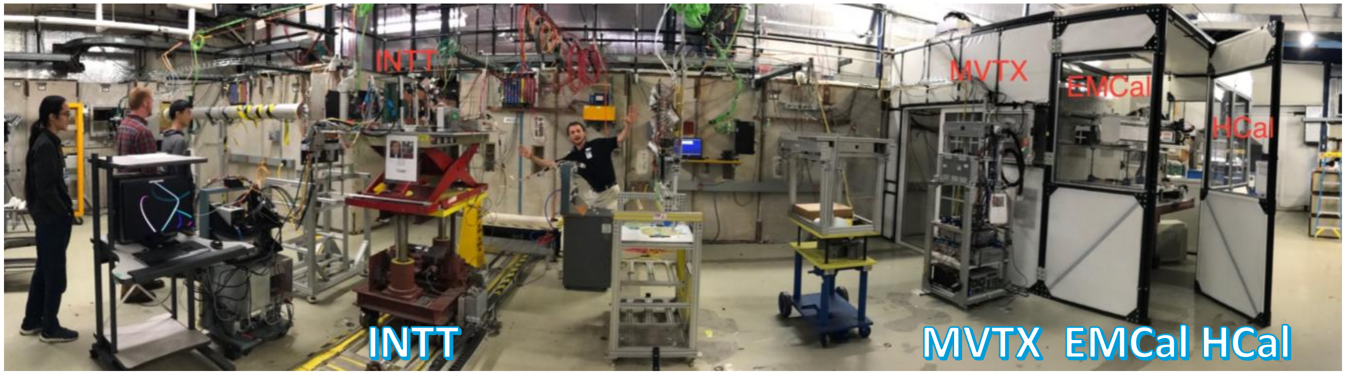
BNL-712 v2 (FELIX2)

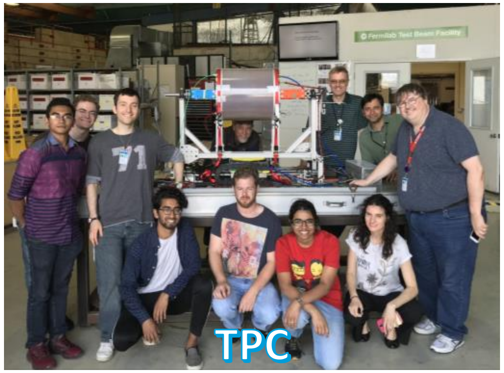


192 GBT fiber links

Exp. Hall | DAQ room

Highlight of sPHENIX prototypes in action

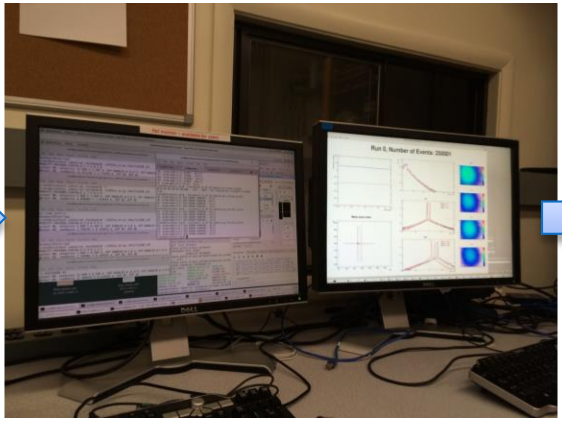




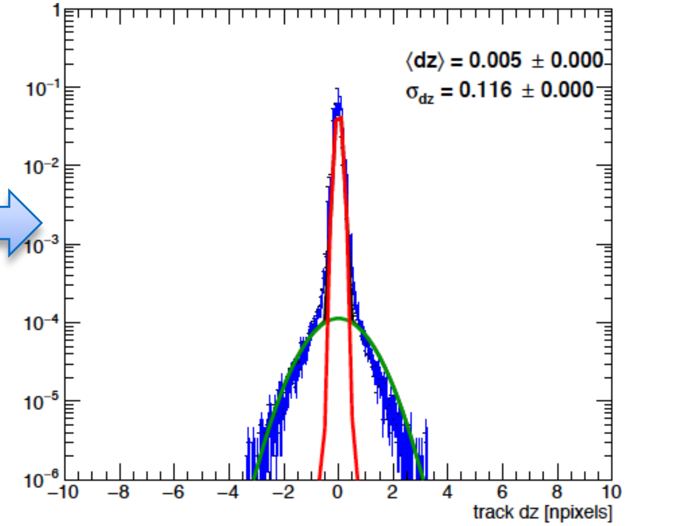
Feb-July 2018 FermiLab Test beam facility, test of each sPHENIX detector subsystem

4x MVTX sensor in beam

sPHENIX DAQ



MVTX Hit Spatial Resolution: < 5 um

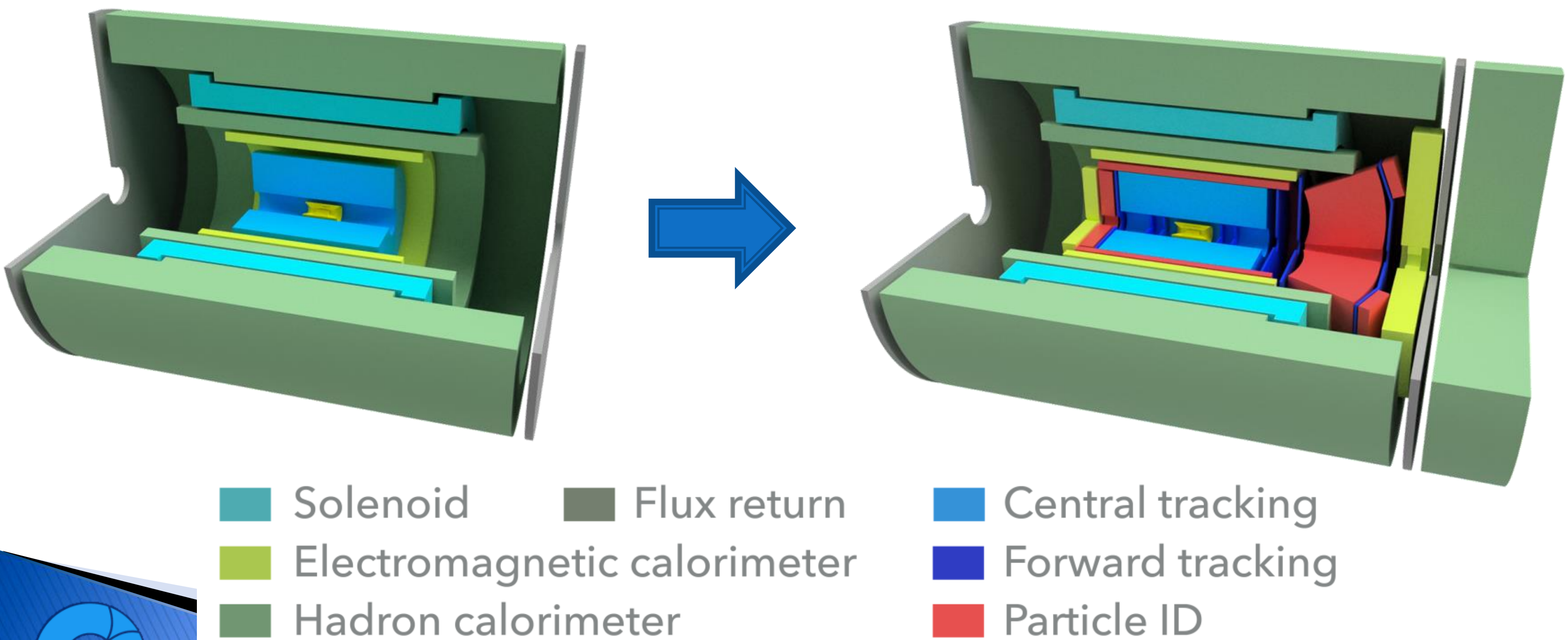


A EIC detector concept based sPHENIX and its streaming DAQ

- Detector concept
- Rate estimation
- DAQ strategy
- DAQ interface

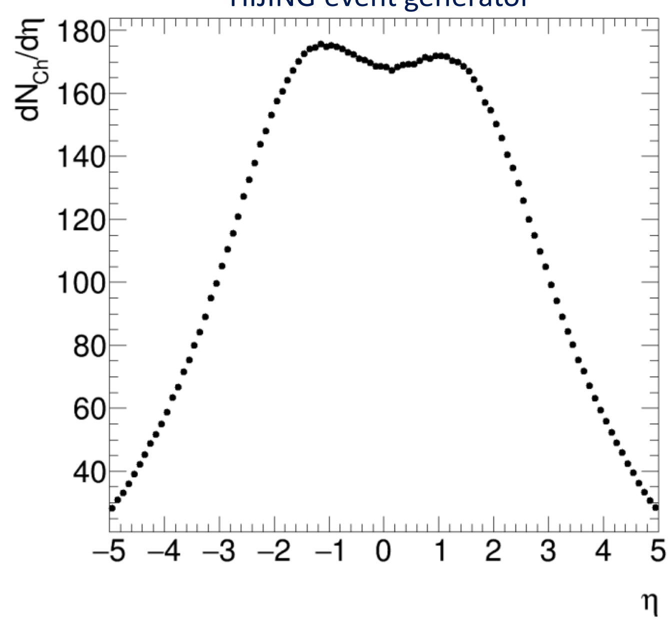
An EIC detector concept based on sPHENIX

- Using sPHENIX as a foundation with further instrumentation of tracker, calorimeter and PID
- Reuse and upgrade the streaming parts of sPHENIX Readout & DAQ
- Letter of intent in 2014: arXiv:1402.1209 [nucl-ex]
- On-going design study in public note: sPH-cQCD-2018-001 @ https://indico.bnl.gov/event/5283/



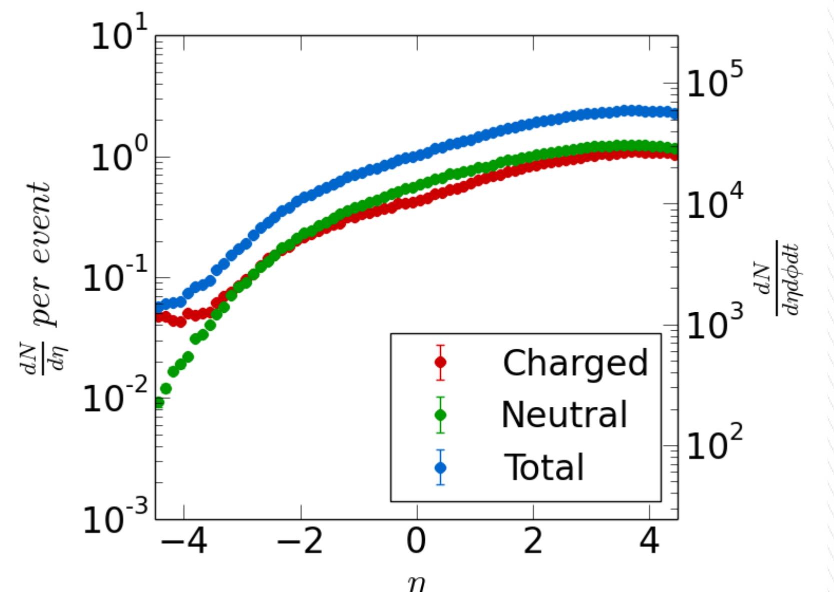
sPHENIX rate VS EIC charge track rate

Charged multiplicity, Au+Au, 100 + 100 GeV/c



Multiplicity, e+p 20+250 GeV/c, 50μb

https://wiki.bnl.gov/eic/index.php/Detector_Design_Requirements



sPHENIX AuAu $dN_{ch}/d\eta$ ~200, $|\eta|<1$

Streaming readout @ 200 kHz collision : 80 M N_{ch}/s

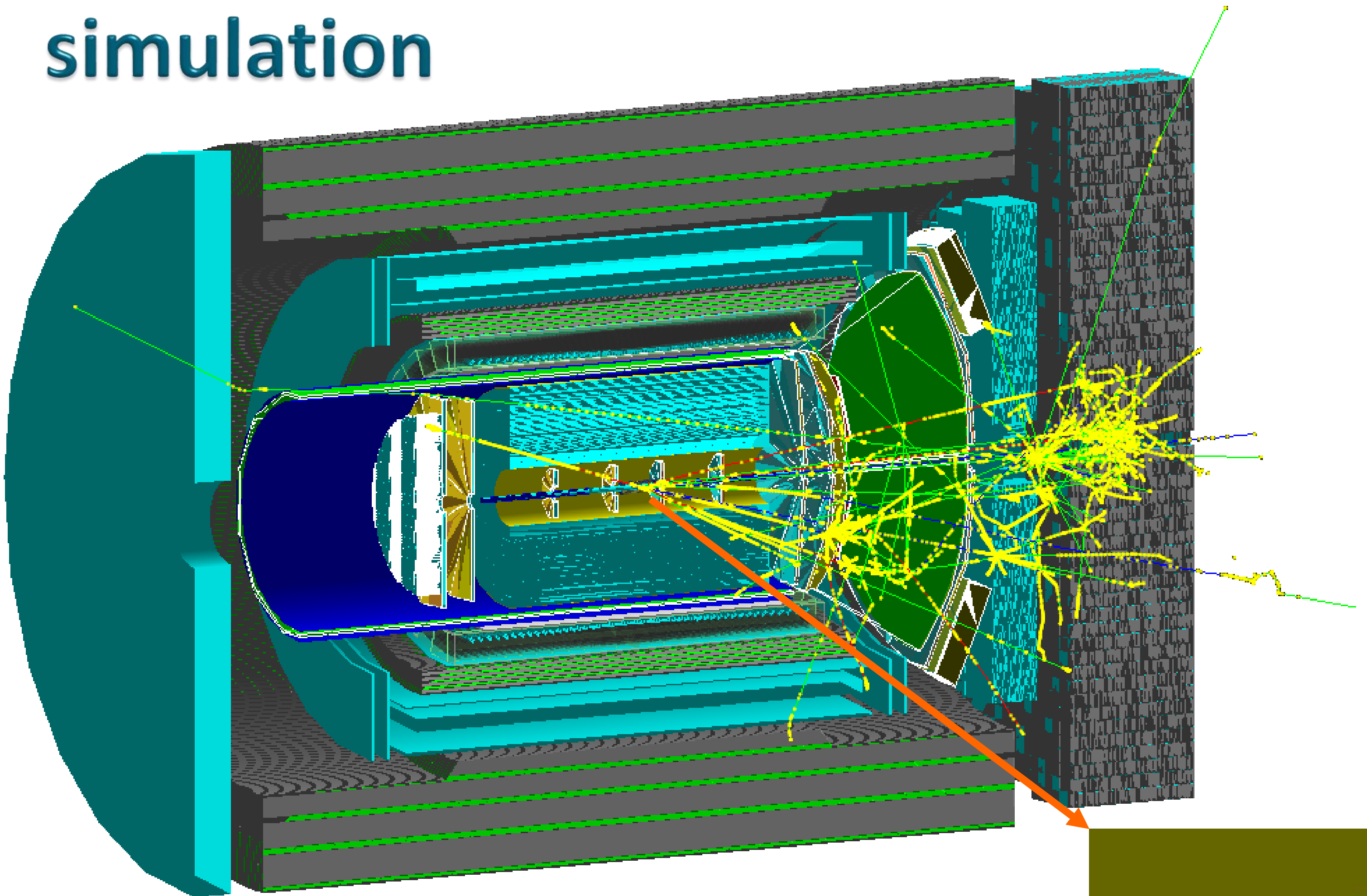
DAQ throughput @ trigger rate 15 kHz: 6 M N_{ch}/s + pile up

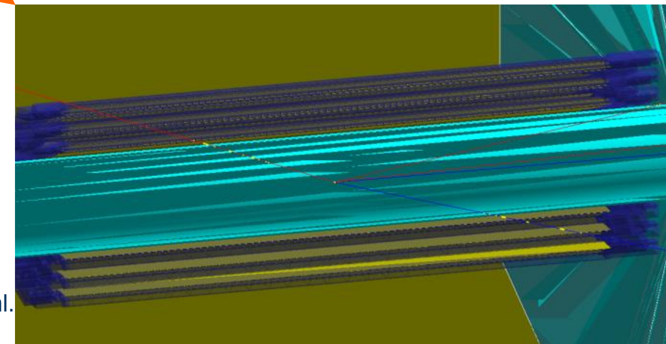
EIC 20+250 GeV/c $dN_{ch}/d\eta$ ~1, $|\eta|<4$

Streaming readout @ 500kHz collision (10^{34} cm^{-2} s^{-1}) : 4 M N_{ch}/s << sPHENIX

DAQ throughput, full stream: 4 M N_{ch}/s <~ sPHENIX

More quantitative? Take a look in EIC simulation



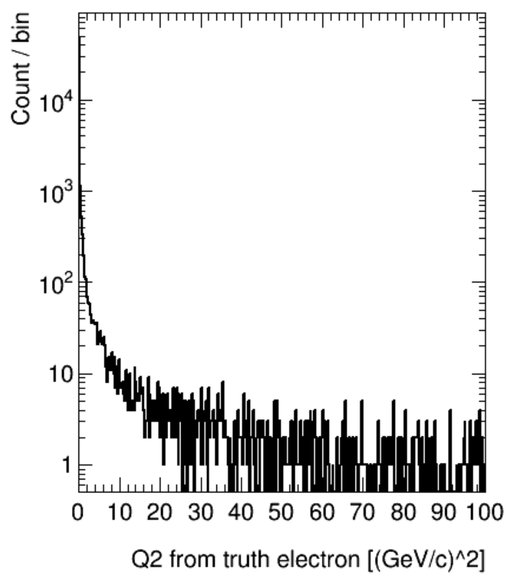


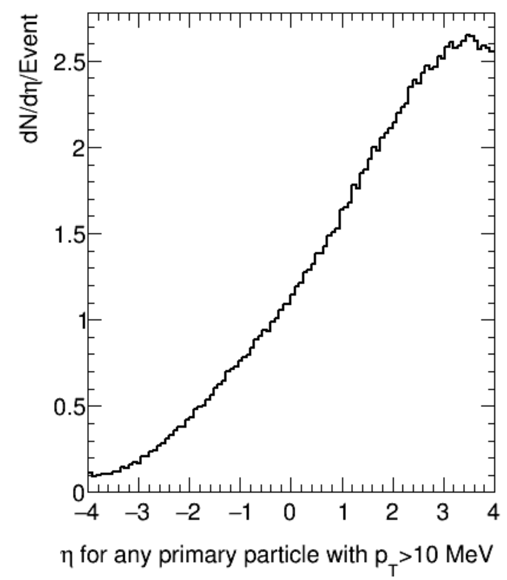
e+p collision 18+275 GeV/c
DIS @ $Q^2 \sim 100\ (\mathrm{GeV}/c)^2$

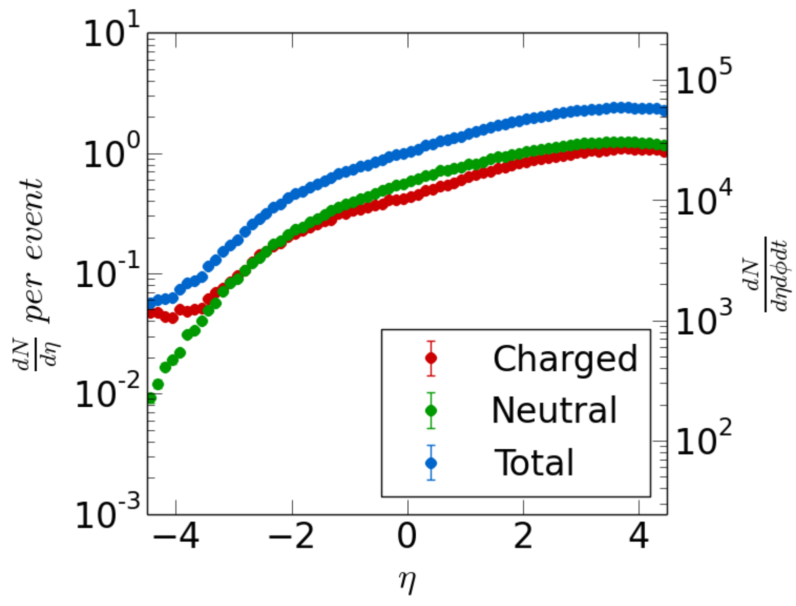
Full detector "Minimal bias" EIC events in sPHENIX framework: quick first look

Multiplicity check for all particles
Minimal bias Pythia6 e+p 20 GeV + 250 GeV
53 μb cross section

BNL EIC taskforce studies
https://wiki.bnl.gov/eic/index.php/Detector_Design_Requirements

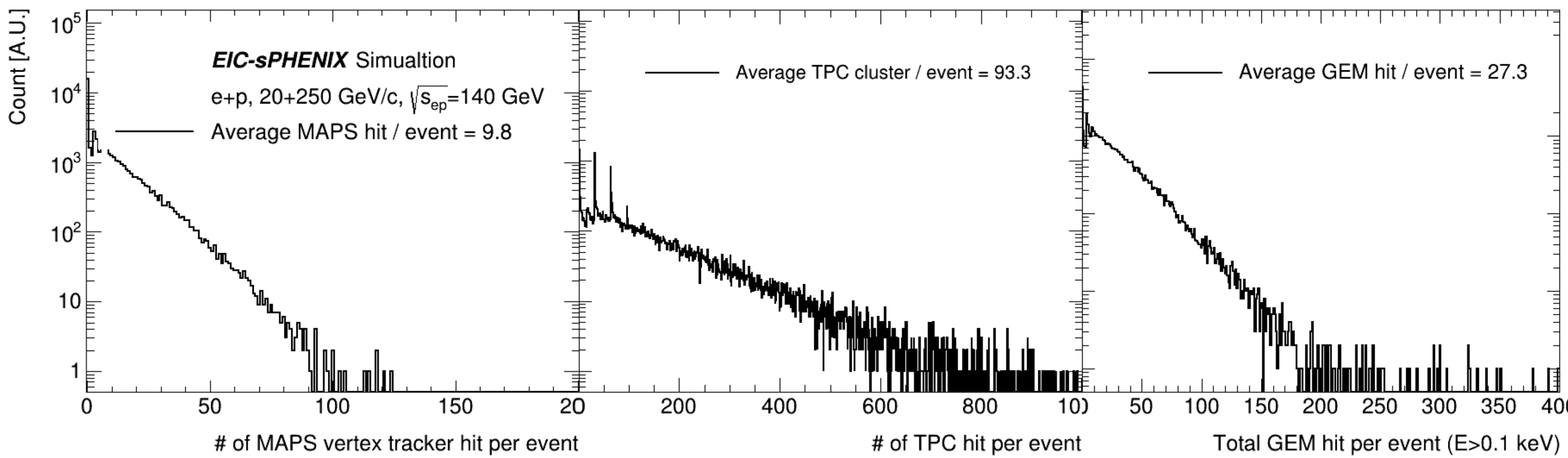






Based on BNL EIC task-force eRHIC-pythia6 event-gen set

GEANT4-based detector simulation for DAQ simulation: tracker



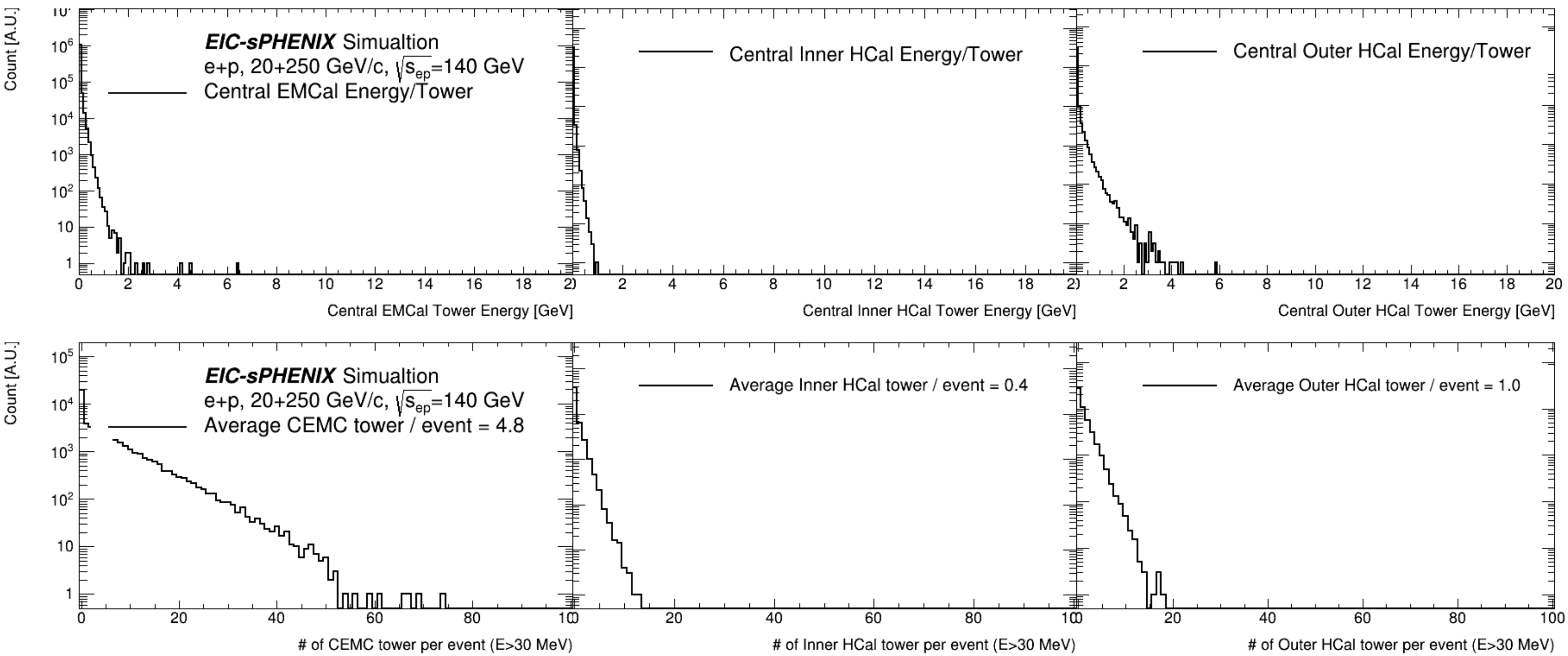
Raw data: 16 bit / MAPS hit

Raw data: 3x5 10 bit / TPC hit
+ headers (60 bits)

Raw data: 3x5 10 bit / GEM hit
+ headers (60 bits)

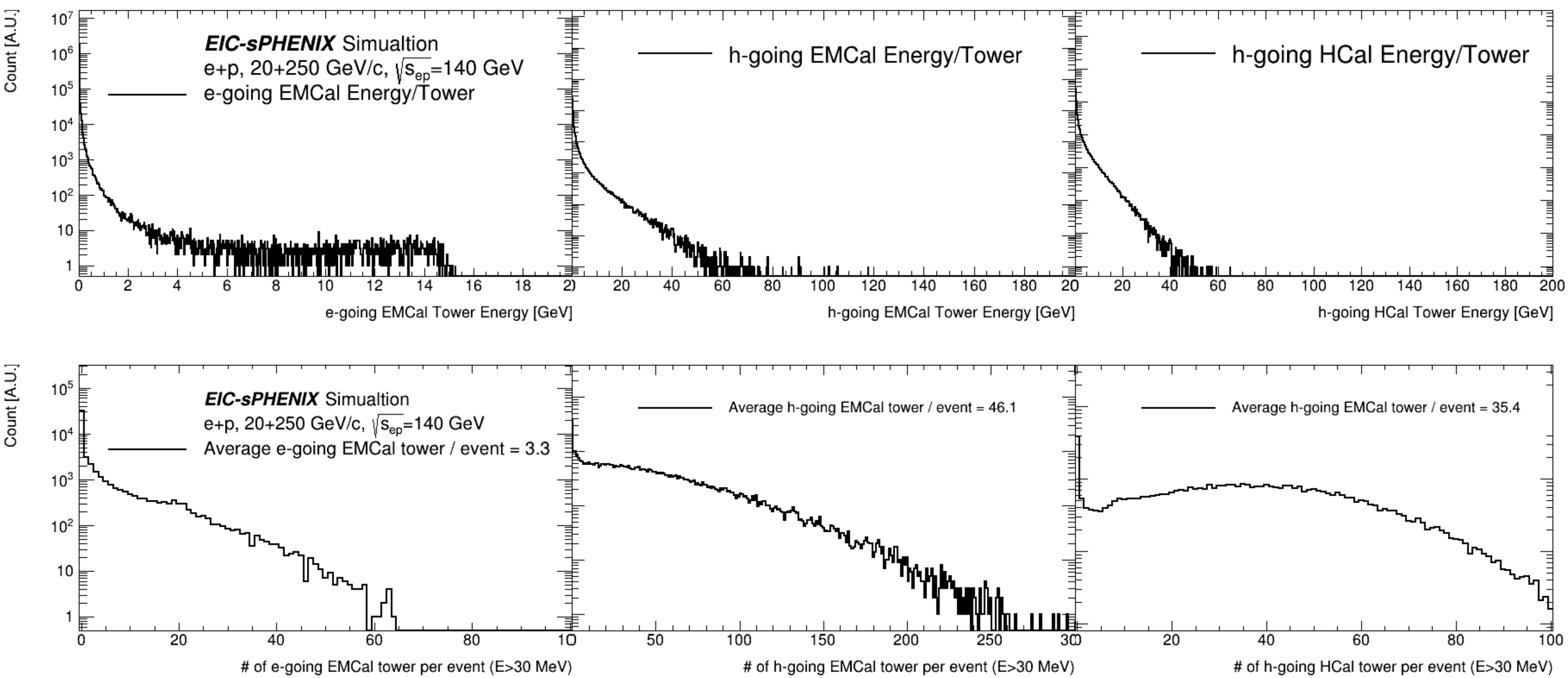
GEANT4-based detector simulation for DAQ simulation: central calorimeters

Raw data: 31x 14 bit / active tower +padding + headers ~ 512 bits / active tower



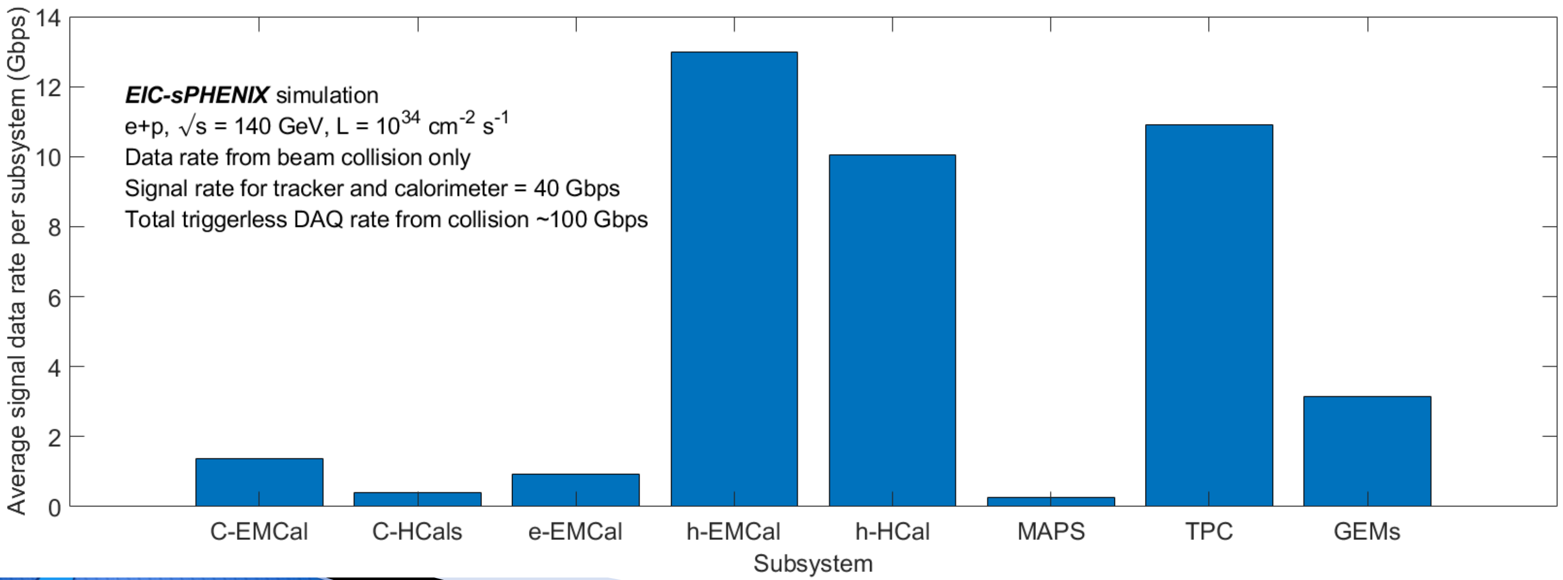
GEANT4-based detector simulation for DAQ simulation: forward calorimeters

Raw data: 31x 14 bit / active tower +padding + headers ~ 512 bits / active tower



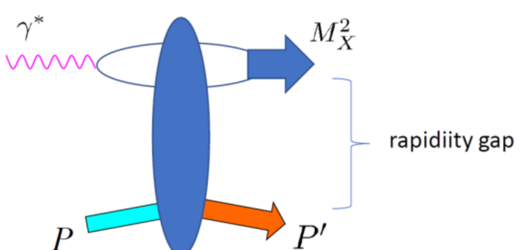
EIC preliminary data rate summary

- Tracker + calorimeter ~ 40 Gbps
- + PID detector + 2x for noise ~ 100 Gbps
- Signal-collision data rate of 100 Gbps seems quite manageable,
  - < sPHENIX TPC disk rate of 200 Gbps
- Machine background and noise would be critical in finalizing the total data rate
  - From on-going sPHENIX R&D prototyping will show noise level from state-of-art MAPS and SAMPA ASICs
  - Prevision for noise filtering in EIC online system



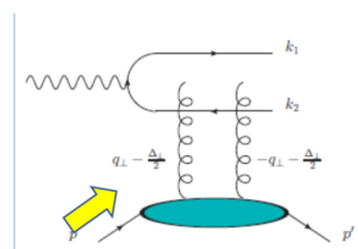
sPHENIX-EIC DAQ Strategy

- Full streaming readout → DAQ interface to commodity computing via PCIe-based FPGA cards (e.g. BNL-712/FELIX series) → Disk streaming raw data → Event tagging in offline production
- Why streaming readout?
  - Versatility of EIC event topology make it challenging to design a trigger on all interested event. e.g. new diffractive-type events below, and new type of events not yet envisioned?
  - Many EIC measurement, e.g. SF, are systematic driven. Streaming minimizing systematics by avoiding hardware trigger decision + keep background and history
  - At 500kHz collision rate, many detector would require streaming, e.g. TPC, MAPS
- Why BNL-712/FELIX series DAQ interface? [More on next slides]
  - 0.5 Tbps x bi-direction IO to FEE <-> large FPGA <-> 100 Gbps to commodity computing
  - O($100) / 10Gbps bidirectional link
- Why keep raw data?
  - At 100 Gbps < sPHENIX rate, we can disk all raw data: If you can, always keep raw data.
  - Achieve final minimal systematics may require refining calibration with integrated and special (e.g. z.f.) data.
  - Calibration in real-time for final production in real-time requires considerable manpower for preparation (100 FTE?) and risky to fit in initial running years.



Diffractive (general)

$d\Delta\sigma \sim$



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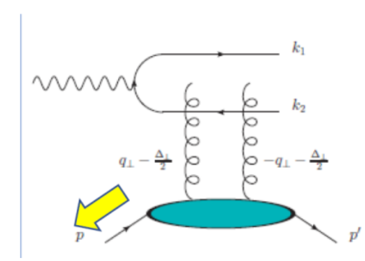

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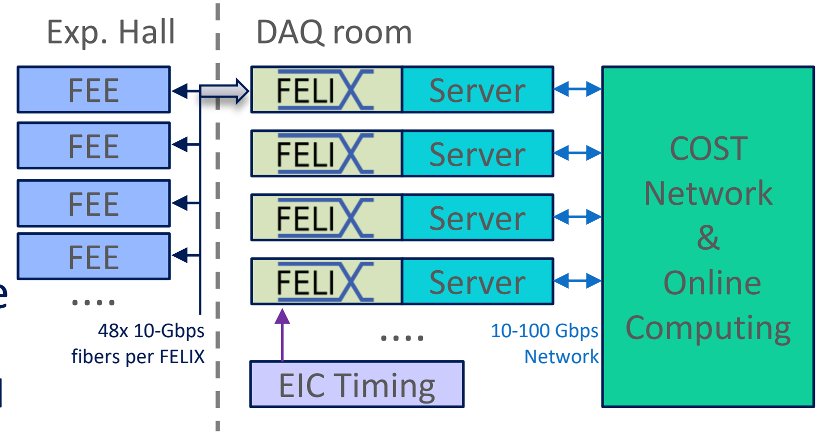
Diffractive di-"jet" :
Promising new channel to access OAM

A streaming DAQ architecture

- Using PCIe FPGA card bridging stream-readout FEE on detector and commodity online computing
  - Similar approach taken at ATLAS, LHCb, ALICE phase-1+ upgrades and sPHENIX
- Implementation: BNL-712-series FPGA-PCIe card
  - 2x 0.5-Tbps optical link to FEE: 48x bi-directional 10-Gbps optical links via MniPODs and 48-core MTP fiber
  - 100 Gbps to host server: PCIe Gen3 x16
  - Large FPGA: Xilinx Kintex-7 Ultra-scale (XCKU115), 1.4 M LC
  - Bridge µs-level FEE buffer length with seconds level DAQ time scale
  - Interface to multiple timing protocols (SPF+, White Rabbit, TTC)
  - Developed at BNL for ATLAS Phase-1 FELIX upgrade, down selection to use for streaming FEE readout in sPHENIX, proto-DUNE, CBM
  - Continued development to upgrade to 25-Gbps optical links, Vertex7 FPGA and PCIe-Gen4



FELIX Card – BNL712 - v2.0

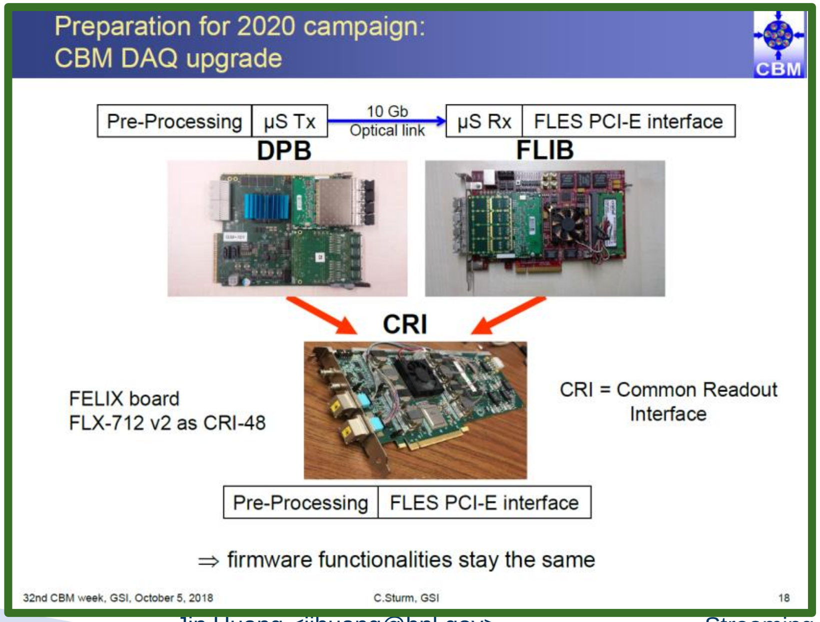
FELIX timing interface mezzanine

FELIX-server test stands at BNL

Productions for BNL-712v2/FELIXv2

- Ongoing FY19 BNL-712v2/FELIXv2 card production from BNL covering sPHENIX advanced R&D
  - CBM working on joining this production and adopting this architecture for 2020 campaign too.
  - 2nd sPHENIX production planned after sPHENIX CD-3B (FY20?)
  - BNL produced 40x cards in various versions of FELIX in ATLAS pre-productions, which will continue too.
- Synergies from further EIC stream readout R&D welcomed too

Courtesy of C. Stum, D. Emschermann (GSI)
See also talk of Dr. Volker Friese (GSI)

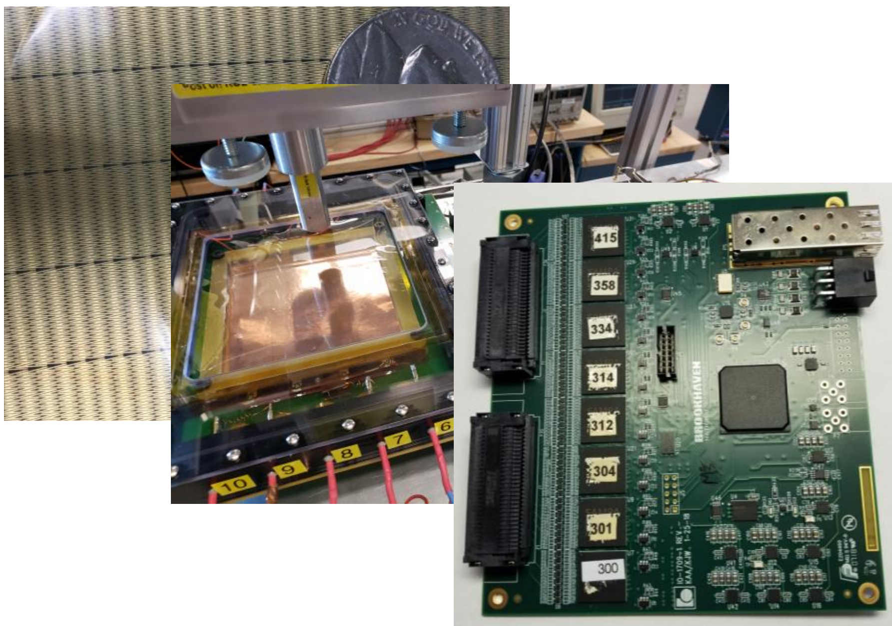


Recent highlights

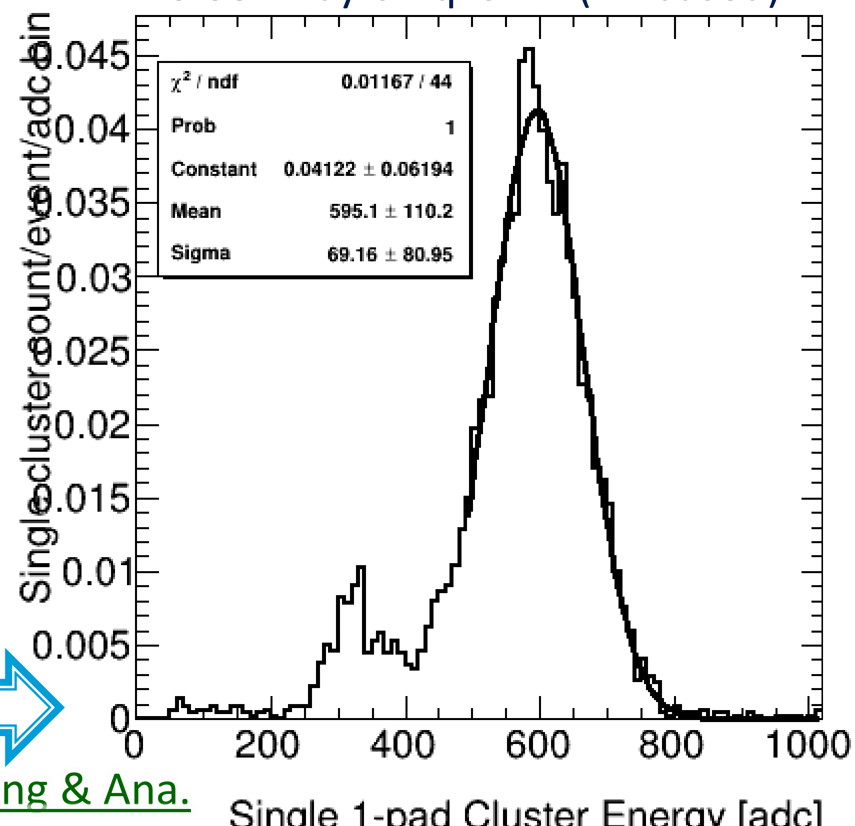
- GEM & TPC streaming FEE – SAMPA
- Timing distribution
- BNL LDRD on high throughput DAQ

SAMPA test stand with EIC RD GEM tracker

- Readout of the eRD6 GEM + zigzag pad with SAMPA FEE + FELIX test stand
- sPHENIX also initiate engineering and production for a special version of SAMPA with ½ current min shaping time (→80ns) @ University of São Paulo & TSMC



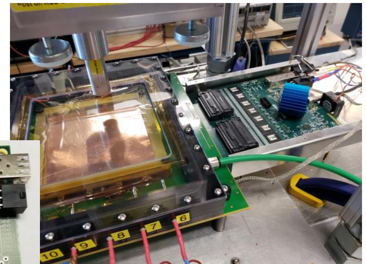
Fe-55 x-ray on q-GEM (Ar-based)



Raw data, decoder, clustering & Ana.

SAMPA test stand with EIC RD GEM tracker

X-ray src, eRD6 GEM + zigzag pad



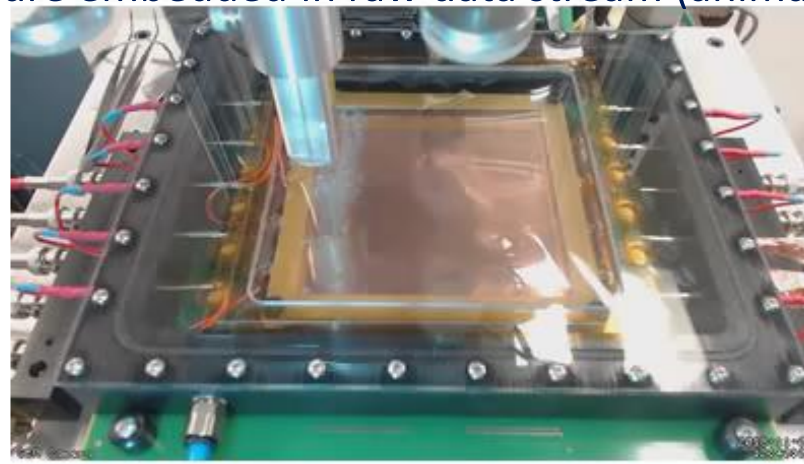
8x SAMPA FEE

BNL-711 (→ BNL-712v2)

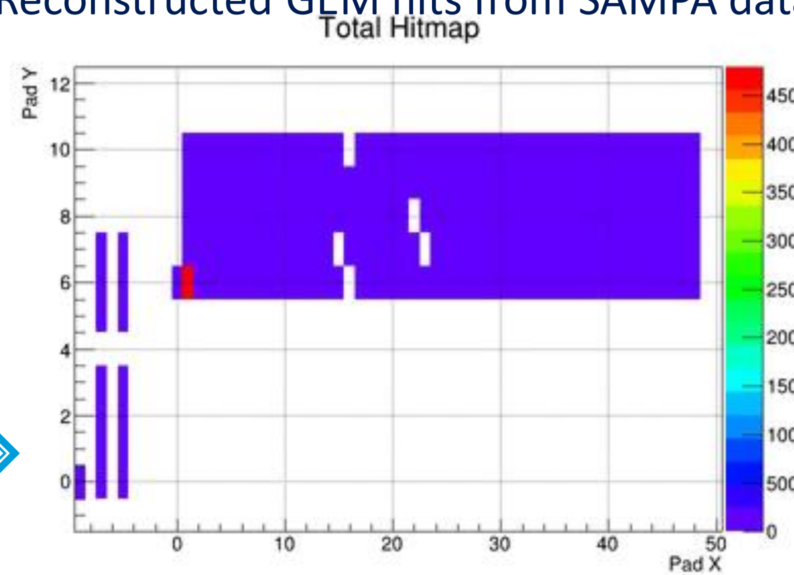
Commodity server

Raw data & Ana.

Picture embedded in raw data stream (animation)

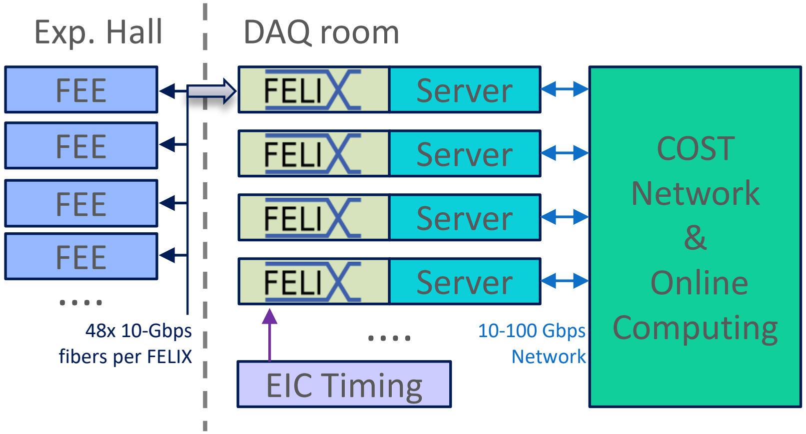


Reconstructed GEM hits from SAMPA data

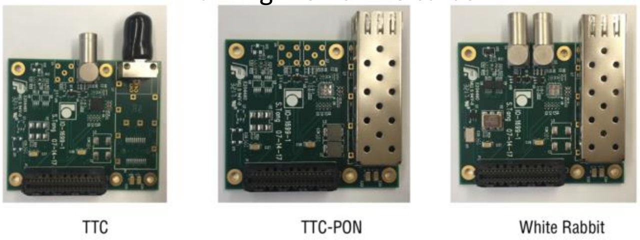


Timing distributions

- All PHENIX/sPHENIX FEE are synced to beam clock/counter. Expecting similar for EIC detector
- BNL-712/FELIX can receive clock of multiple protocols (SPF+, White Rabbit, TTC, …) via a timing mezzanine card
- SI5345 jitter cleaner control jitter to <0.1 ps
- BNL-712/FELIX carries 48x 10 Gbps downlink fiber for control data to FEE. Beam clock and sync word can be encoded on fiber (e.g. 8b10b encoding)
- For EIC hadron beam RF, extra cautious need to be taken for hadron machine ramp from low gamma to high gamma, which leads to clock frequency variation [next slide].

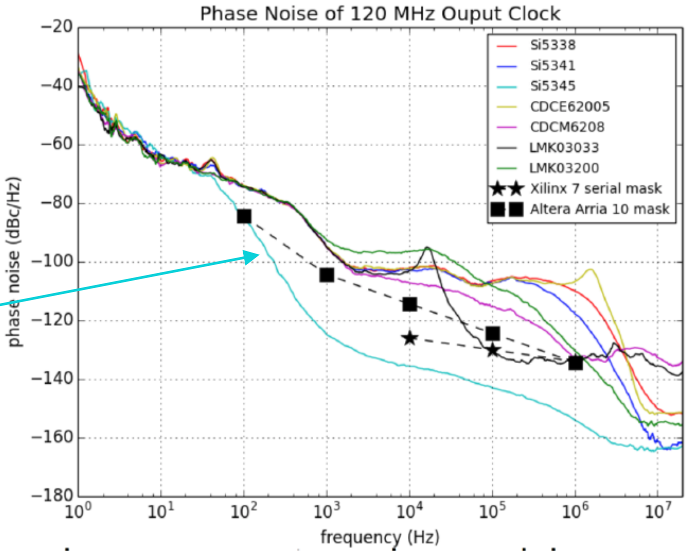


timing mezzanine cards



Device	SI5338	SI5345	SI5341
Jitter (ps)	8.58	0.09	6.39
Device	CDCM6208	LMK03200	LMK03033
Jitter (ps)	2.06	5.91	2.74
Device	CDCE62005		
Jitter (ps)	8.61		

The jitter from 10 kHz to 1 MHz



Courtesy of Kai Chen (BNL)

Kai Chen – FELIX Design Review

Embedded clock demo with variable beam clock frequency

Function generator mimic repeated RHIC clock ramping (triangle pattern)

Demo FELIX
Kintex-7 Ultrascale

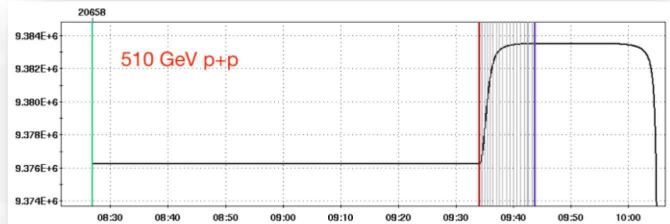
Downlink: 4.8 Gb/s
Multiples of RHIC clock (9.4 MHz)
Recover clock from 8b/10b

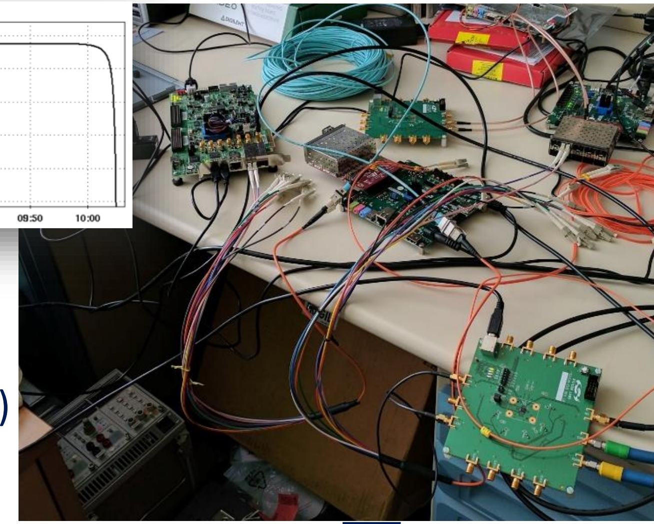
Optical Links

Demo FEE
Atrix-7

Uplink: 4.8 Gb/s, fixed clock

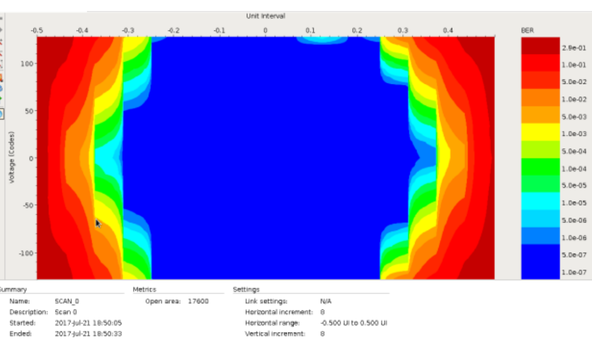
RHIC frequency spread (due to ramp) is large, 9.362 MHz ±22 kHz



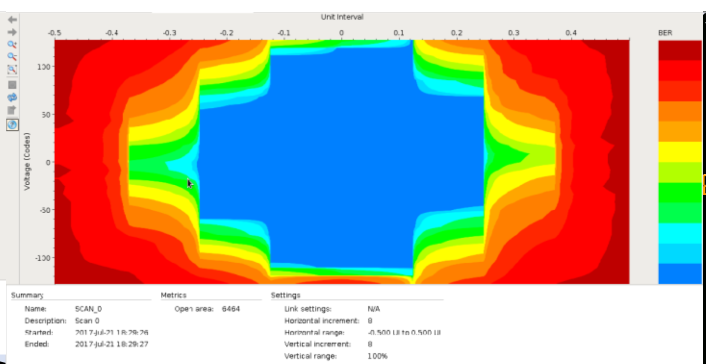


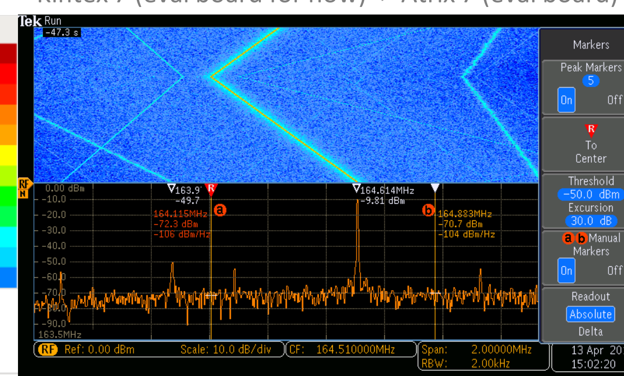
Test recovered “RHIC” clock
Kintex 7 (eval board for now) -> Atrix 7 (eval board)

Uplink iBERT @ DAM: 1.46e-13



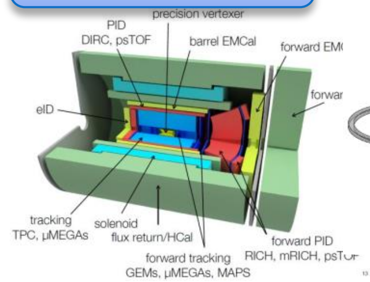
Downlink iBERT @ FEE: 1. 023e-13

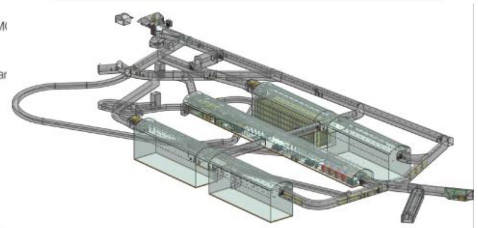


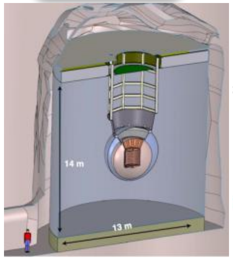


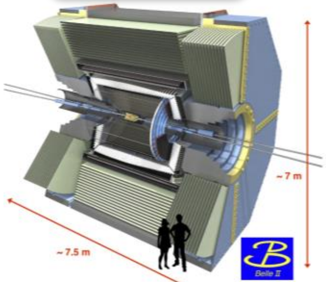
Future explorations, BNL LDRD 19-026: Common development for Advanced DAQ

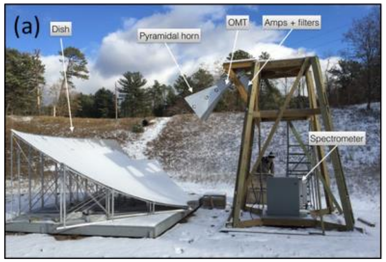
EIC detectors | DUNE far detector | nEXO | BELLE-II | 21-cm digital interferometer

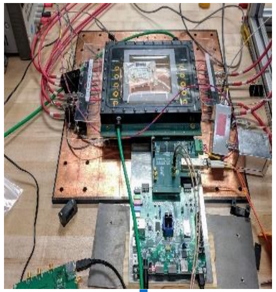


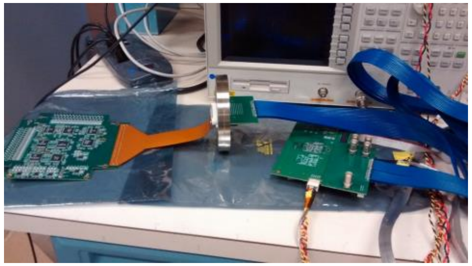


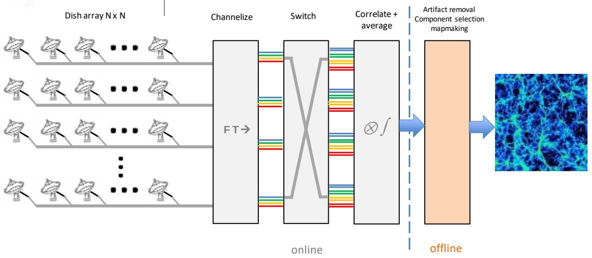












BNL 712 – series PCIe Card

Commodity Computing

Common challenge cross multi-discipline of BNL: Advance DAQ with high throughput @ 100 Gbps

Solution: FELIX-based DAQ, the architecture used in the LHC upgrades in the 2020s

Deliverable: test stand & firmware for each case

Co-PIs: Kai Chen (BNL/ATLAS),
Jin Huang (BNL/sPHENIX)

Strong contribution from BNL instrumentation

Summary

- PHENIX and sPHENIX builds long experience for streaming readout front-end
- We are exploring one way to build EIC detector streaming readout and trigger-less DAQ based on architecture of sPHENIX DAQ. Looks promising
  - Preliminary simulation show disk rate for EIC collision signal (100 Gbps) expected lower than sPHENIX disk rate (200 Gbps)
  - Controlling background for high-L low-σ collisions would be important for collider, detector and DAQ designs.
- BNL-712/FELIX-type DAQ architecture fits EIC purpose. Similar architecture have wide support in 2020+ for high throughput DAQ e.g. ATLAS, ALICE, LHCb, CBM, Bell-2, and cost effectively bridges custom front-end with commodity computing
- Productions planned for BNL-712/FELIX DAQ interface, more EIC R&D interests welcomed

PHENIX/FVTX streaming readout

sPHENIX SAMPA+FELIX DAQ chain reading out EIC GEM detectors