

Previous Streaming Readout Workshops and Funding

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Streaming Readout III

Chritopher Newport University

December 3–5, 2018

Previous Streaming Readout Workshops

January 27, 2017 at MIT

- Conceptual ideas
 - streaming readout concept - Jan Bernauer (MIT)
 - ...
- various approaches
 - sPHENIX - Martin Purschke (BNL)
 - JLab - Graham Heyes (JLab)
 - TDCPix - Matt Noy (CERN)
 - computing in future triggers - Gianluca Lamanna (CERN)
 - concept for detector DAQ - Ryan Herbst (SLAC)
 - ...



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- sPHENIX - Martin Purschke (BNL)
- Evolution of JLab DAQ - Graham Heyes (JLab)
- SoLID - Alexandre Camsonne (JLab)
- SLAC DAQ efforts - Ryan Herbst (SLAC)
- Streaming readout for 12 GeV program - Chris Cuevas (JLab)
- Front-end ASICs and readout electronics - Shaorui Li (BNL)
- Alphacore - Esko Mikkola
- LHCb and machine learning - Mike Williams (MIT)
- Streaming readout and EIC - Markus Diefenthaler (JLab)



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Jan Bernauer - Introduction and Food for Thought

- future experiments may have to handle high luminosities
- triggered readout difficult or unrealistic
- need cheap, fast readout solutions for many detector types
- DarkLight as a case study, 2 TB/s
- need to standardise hardware and software
- FEE detector specific but components can be modular
- data transport ? software? Open Source?

Markus Diefenthaler - Streaming readout and EIC

- estimated EIC event rates 450 kHz
- data rate 21 GB/s
- want to do 3D imaging of quarks and gluons
- emphasise common interfaces: geometry, event, track reconstruction
- structures must be robust to allow exascale computing
- machine learning in real-time: calibration, reconstruction, analysis
- connected, smart detectors, self optimising

Jose Repond - TOPSiDE Concept of an EIC Detector

- maximize coverage, 5D concept (E, x, y, z, t)
- very high granularity, 50–80 million channels
- imaging calorimeter, low bit depth, detector technology exists
- simplifies tracking, particle flow, PID, software corrections
- advantages of streaming: software trigger, complex triggers possible
- trigger electronics not needed !
- DHCAL test case, 500,000 $1 \times 1 \text{ cm}^2$ channels, 1 bit resolution
- DCAL chip (FNAL, ANL)

Martin Purschke - Streaming Readout in sPHENIX

- TPC uses 8 SAMPAs ASICs on FEE - 256 channels, 10 MS/s, 10 bit
- FEE readout with ATLAS FELIX card (Data Aggregation Module)
- FELIX card in PC (Event Buffering and Data Compression)
- continuous readout of TPC, select chunk correlated with trigger
- working point 100 Gb/s to storage

Alexandre Camsonne - SoLID DAQ Overview

- 100,000–200,000 channels, PVDIS or SIDIS
- 200–600 kHz trigger rate
- FADC readout via VXS 4 GB/s
- large number of GEM channels and occupancy problematic
- also problem with network and storage limits
- need to reduce data in real time

Ryan Herbst - SLAC DAQ Efforts

- Advanced Instrumentation for Research (AIR) group at SLAC
- strong group developing electronics as needed
- general purpose Reconfigurable Cluster Element (RCE)
- system-on-chip based on Zynq FPGA
- external bi-directional high speed links 12 Gb/s each
- 8 RCE nodes on a Cluster On Board (COB)
- provides DAQ on custom ATCA blade
- experiment specific rear transition module, 96 high speed serial links
- basis in a number of experiments

Shaorui Li - Front-end ASICs and readout electronics

- staff of 45 at BNL instrumentation division
- several ASIC's designed for specific experiments

Esko Millola - Alphacore

- high performance analog, mixed signal, RF electronics
- integrated circuit design, 1 or 16 channels / chip
- pre-amplifiers, ADC's, readout integrated circuits
- 10–12 bit ADCs, 50–200 MS/s
- < 1 ps timing resolution on 10 GS/s ADC
- radiation hard

Graham Heyes - Evolution of JLab DAQ

- currently pipeline readout, VME based trigger processor
- 272 channels / VME crate, trigger communication via VXS serial bus
- global trigger capable of 64 crates
- GlueX 1.5 GB/s stored, 50+ VXS systems, custom trigger electronics
- works but ...
- TDIS, timing for proton track $\sim \mu\text{s}$, electron $\sim \text{ns}$, 4 GB/s !
- propose to use SAMPA ASIC
- SoLID 30 GB/s,
- streaming concept detector signals in serial stream
- FPGA stream processor, stream aggregator

Chris Cuevas - Streaming readout for 12 GeV program

- VITA 41 system, 250 MHz FADC, 8 μ s pipeline, FPGA
- extracts energy sum and timing, data for cluster finding, etc.
- provides data compression, high level information
- VME64X, 4 lanes 8Gb/s to each FADC slot
- VXS Trigger Processor in each crate
- Global trigger processor
- Trigger supervisor distributes trigger back to crates for readout

Mike Williams - LHCb and machine learning

- 1 TB/s input rate after zero suppress
- feature building in FPGA reduce rate to 50 GB/s 1 MHz
- real-time reconstruction, particles $P_T > 0.5$ GeV, 8 GB/s
- buffer on 10 PB disk
- full real-time reconstruction for all particles
- machine learning heavily used
- real-time alignment and calibration
- 0.7 GB/s final data set (mix of full and partial events)
- run 3 will process 5 TB/s

Status of Funding and Prospects

Marco Battaglieri - Italian Ministry of Foreign Affairs

- ~55,000 € for first year starting mid-2019
- ~15,000 € matching funds from INFN expected 2/2019
- 3 year program includes post-doc, equipment, and travel

Marco Battaglieri and Jan Bernauer - BNL EIC Detector R&D

- recognition of streaming readout consortium (eRD23) as a group
- \$ 7,500 for travel and to collaborate with sub-detector groups
 - planning to support travel to next workshop in Genova

Markus Dieffenthaler - JLab LDRD (Laboratory Directed R&D)

- development and evaluation of techniques for streaming readout
- \$ 30,000 to develop hardware and software solutions
 - prototype components and parameters for streaming readout
 - prototype event level, real time analysis



Backup slide