Multi-Channel Readout ICs Development Status

Streaming Readout Meeting

December 2, 2018

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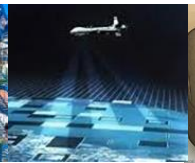
About Alphacore

ALPHACORE

Robust High Performance Microelectronics

- Founded in 2012 and located in Arizona's "Silicon Desert"
- Providing technology that enable major advances in:
  - Homeland Security
  - Defense
  - Aerospace
  - Scientific Research
  - Medical Imaging
- Product areas span:
  - High performance analog and mixed signal
  - High-speed visible light and infrared camera systems
  - Radiation-hard electronics


Alphacore's Team

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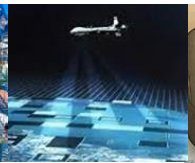
Alphacore's team is a combination of engineering and business professionals with long histories of delivering products and services to customers who demand state-of-the-art performance.

Our team has had successful careers at companies ranging from start-ups to multinationals including **Raytheon, Texas Instruments, Analog Devices, Bell Labs, Intel, United Technologies,** and **Honeywell**.


Multi-Channel Readout IC for Nuclear Physics Experiments

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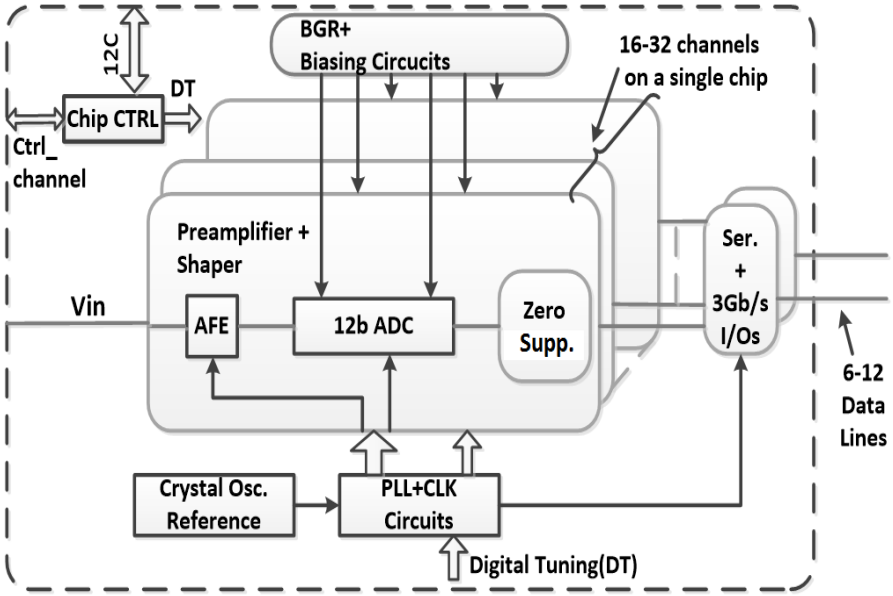
The need

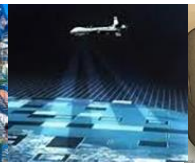
"Universal", low-cost, high-performance, readout integrated circuits (ROICs) for several planned nuclear physics experiments



DOE STTR Phase II

Key features include:

- 1-channel, 8-channel and 16-channel ICs
- Three types of ICs: 1) Preamplifiers, 2) ADCs and 3) Combined ROICs
- 300-800ENC CSA preamplifier for Cd = 0 - 50pF
- 1,300ENC current conveyer preamplifier for Cd = 0 - 300pF
- 12-bit pipeline ADC, 100-200 MSPS, 70mW
- 10-bit pipeline ADC, 50-100 MSPS, <10mW
- Low-cost 180nm CMOS fabrication TID > 300krad
- SEL, SEU, SEFI hardened
- Non-ionizing energy loss (NIEL) > $2*10^{13}$
- First full engineering run tape out finalized in September 2018 in the XFAB 180nm process
- Chips coming back for testing in January 2019


Preamplifier Info

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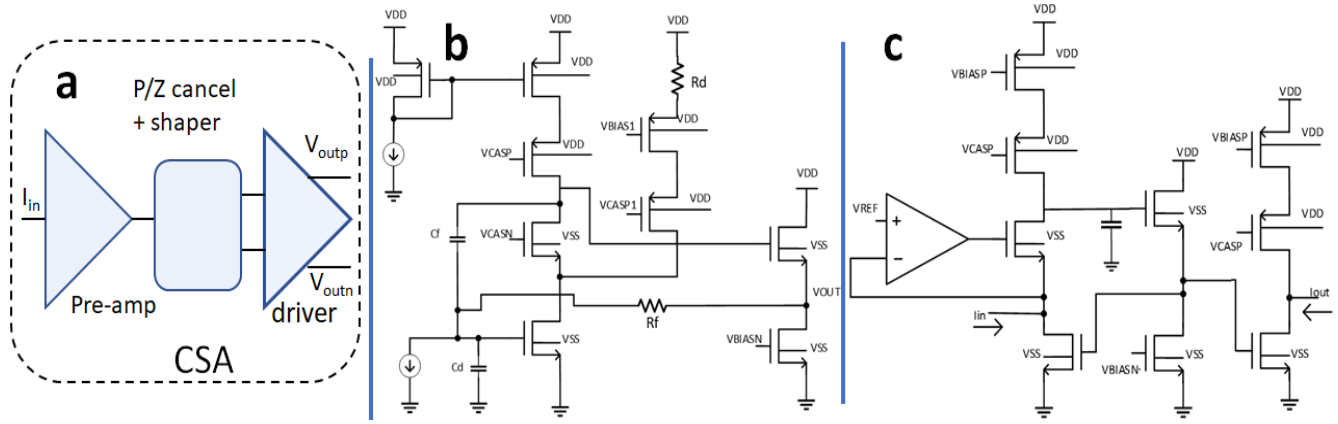


Figure 1: (a) Alphacore's preamplifier architecture, (b) CSA1 charge sensitive pre-amp + shaper (c) CSA2, current conveyer amplifier + shaper

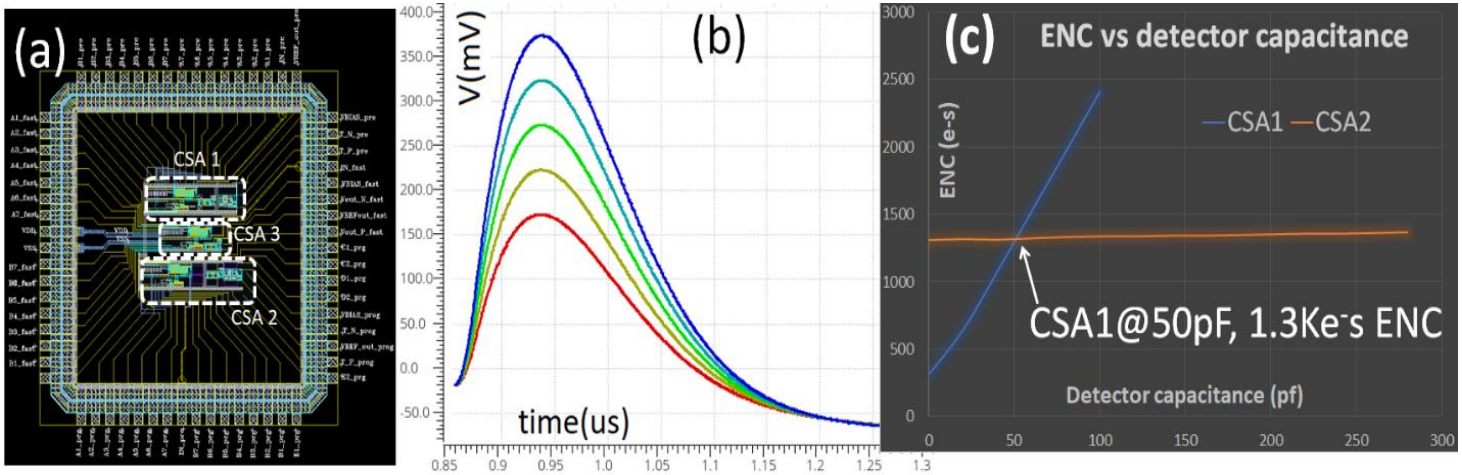
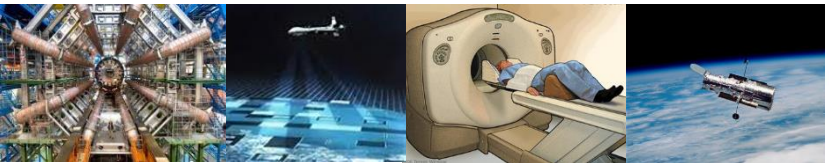


Figure 2: a) Alphacore's test chip to characterize the CSAs b) transient simulations of CSAs for varying input current pulses c) comparison of ENC of CSA1 and CSA2.



ADC Info

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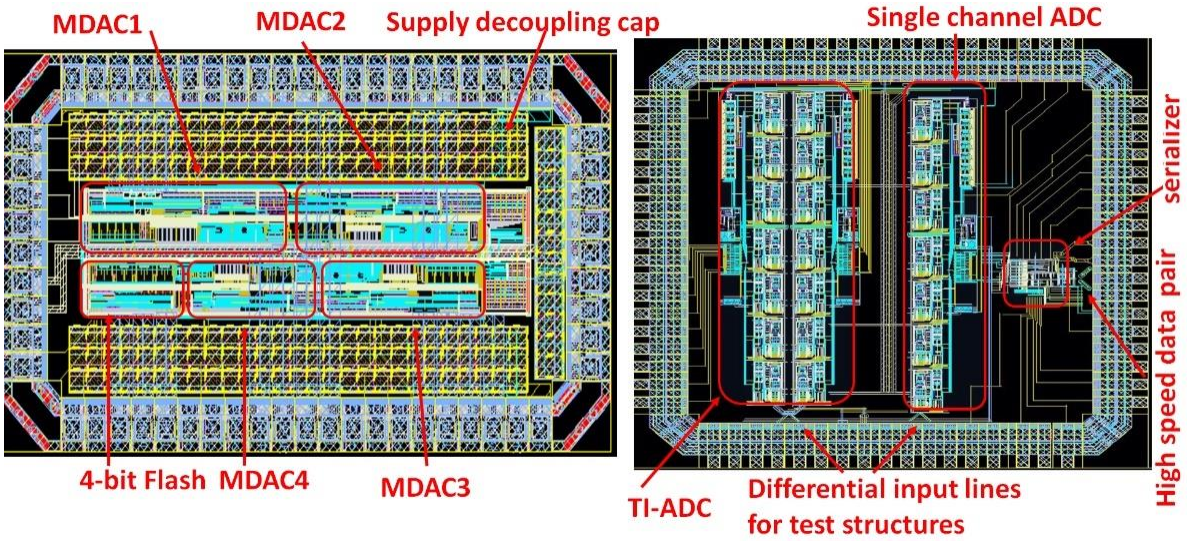


Figure 3: Alphacore's test chips sent for fabrication to measure performance of 12bit 100MS/s ADC (left) and 10bit 50MS/s ADC (right) in different configurations (including time-interleaving). A total of three different layouts are sent for fabrication to test various configurations of the ADCs.

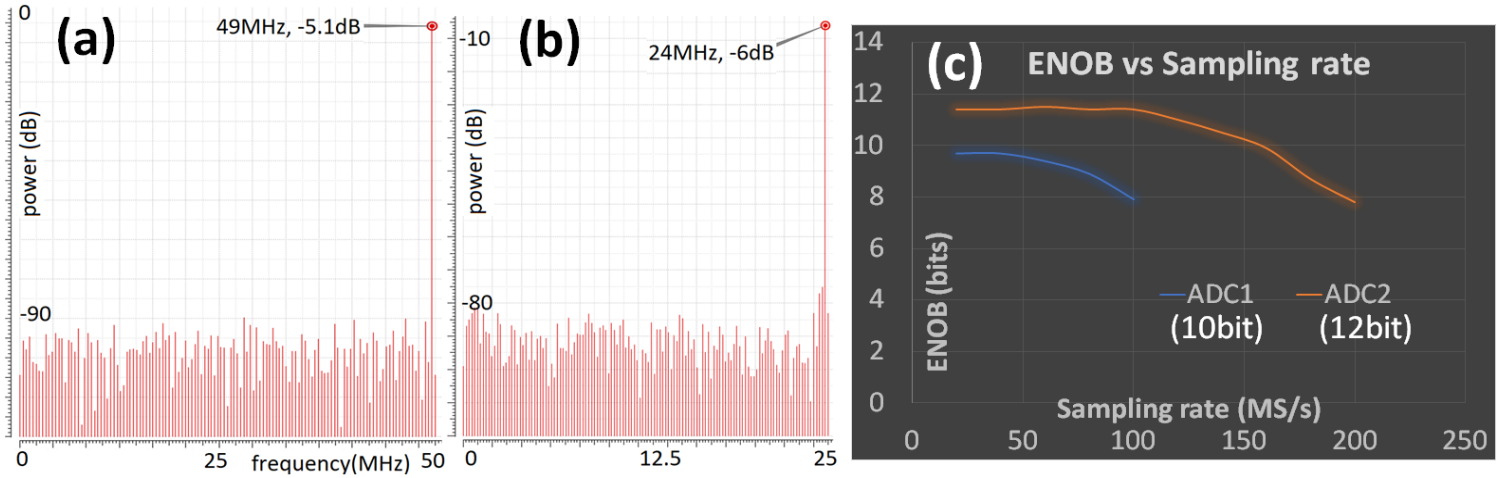
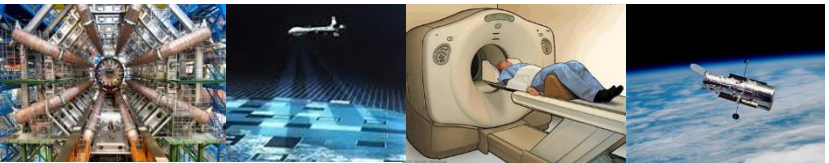


Figure 4: FFT response of 12bit, 100MS/s and 10bit, 50MS/s ADCs



RADHARD JESD204A Serialized I/O

Provides robust 800Mb/s, or 1.6Gb/s speeds per single I/O pair

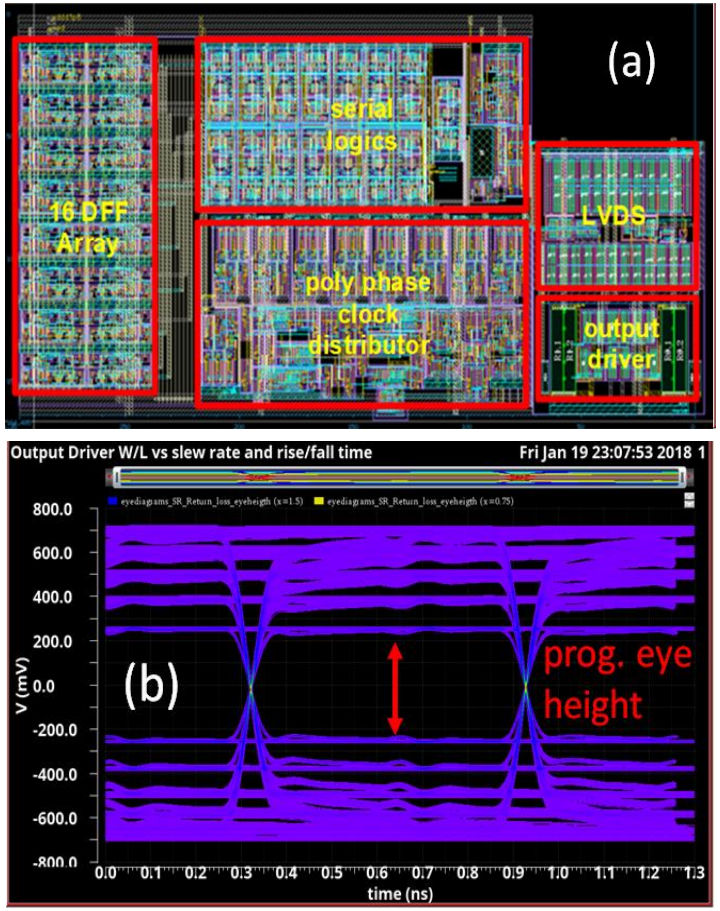


Figure 6: a) Alphacore's serializer layout and b) programmable eye height for easy signal swing matching to FPGA receiver.

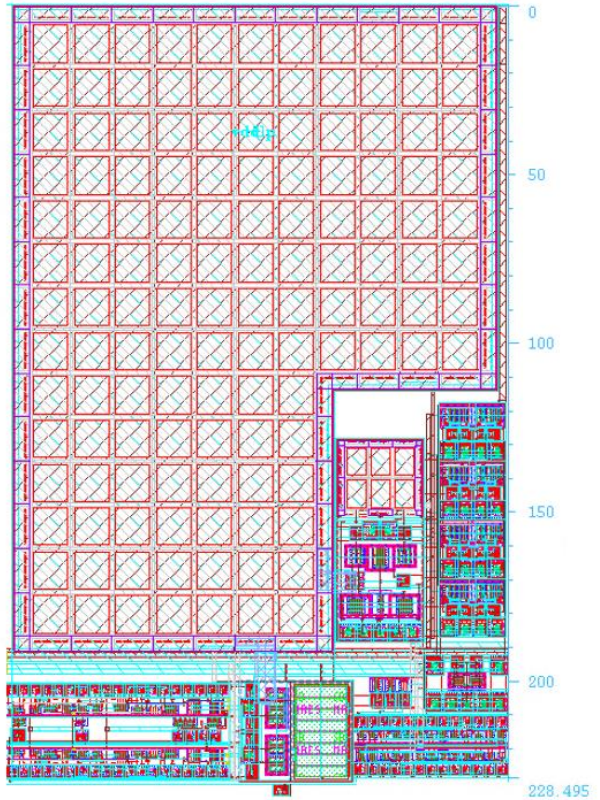


Figure 7: 400MHz – 800MHz PLL layout

Preparation for Chip Evaluations, Status (1/2)

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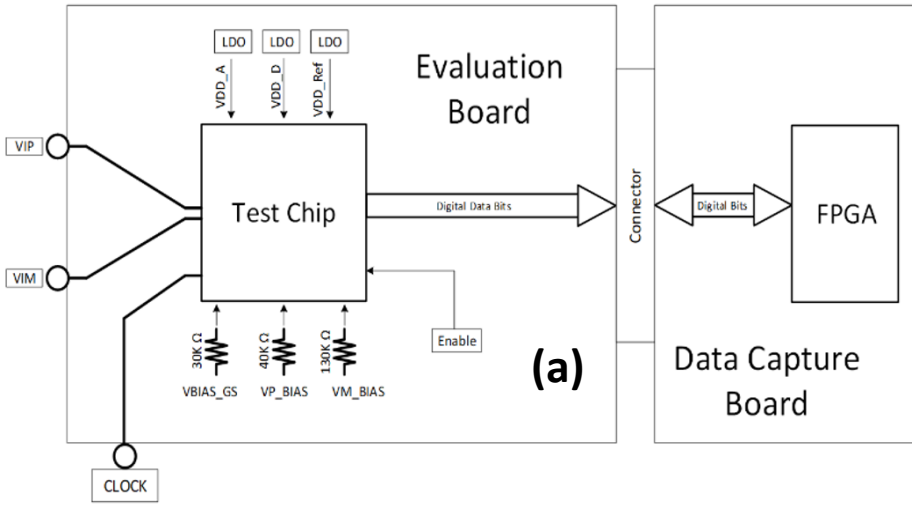
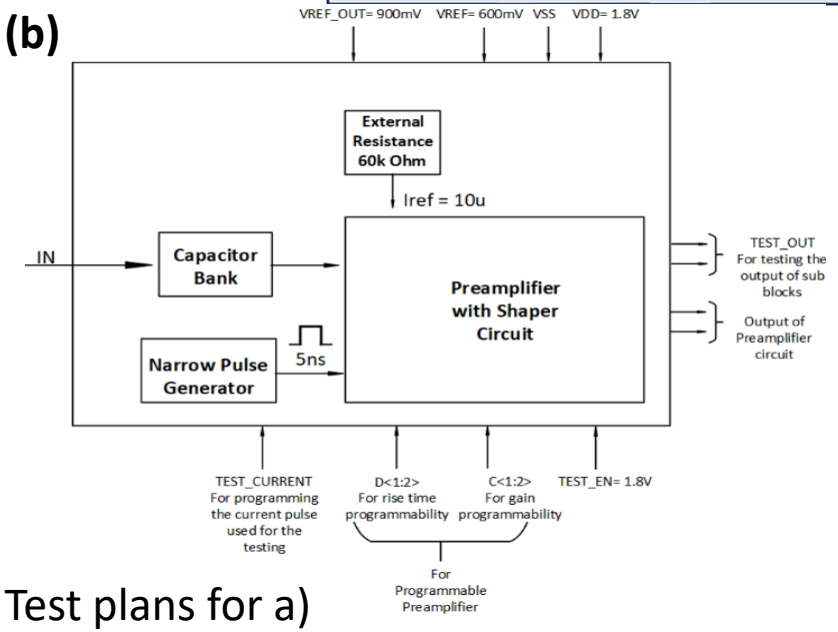




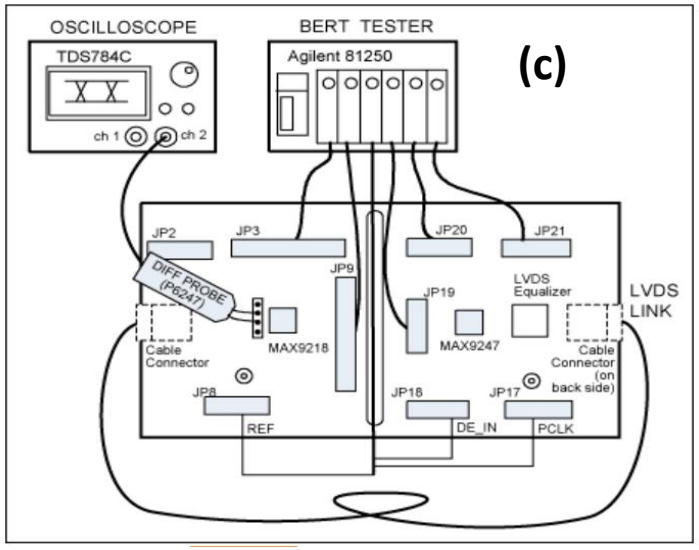
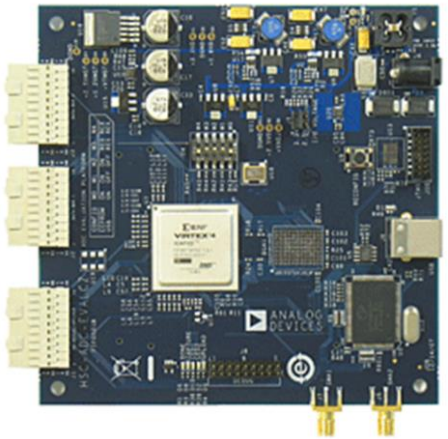
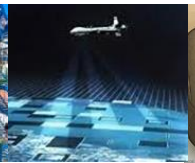


Figure 8: Test plans for a) ADCs, b) CSAs c) Serializer

Wide functionality testing will be performed with lab equipment and COTS ADC evaluation boards.





Preparation for Chip Evaluations, Status (2/2)

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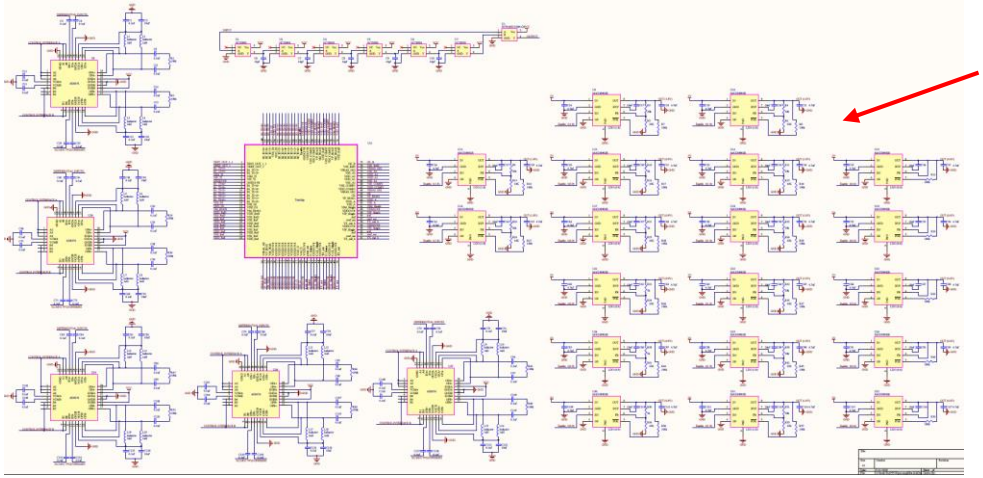
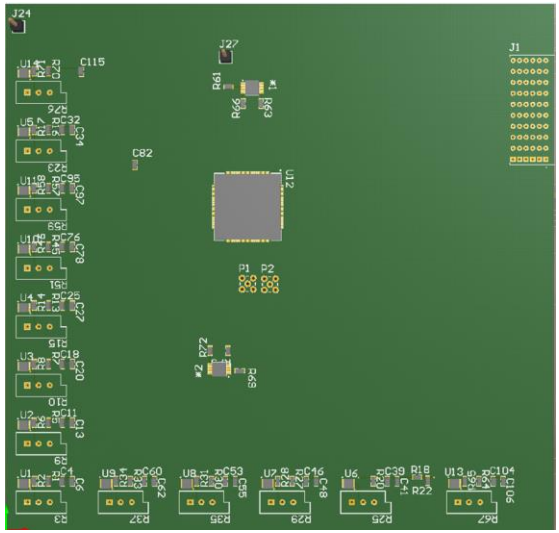
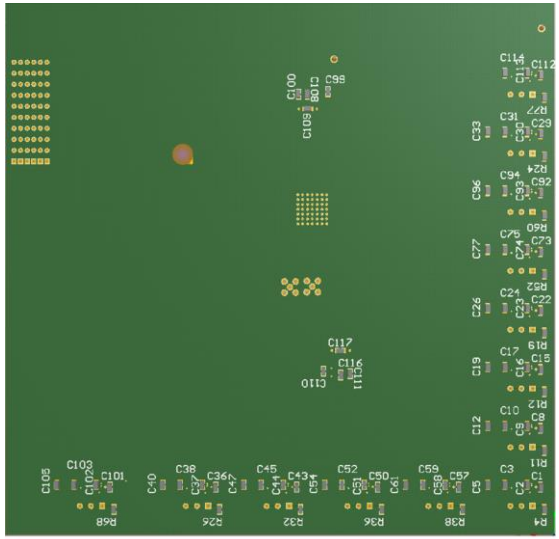
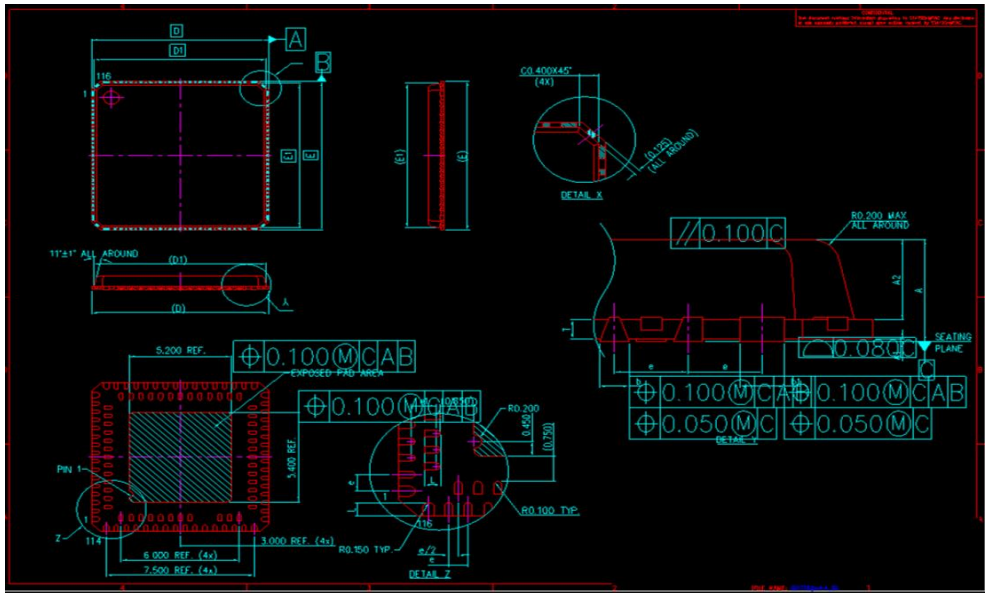


PCB schematic for ADC (both 12 and 10 bits) boards

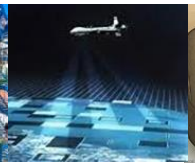


Board (under development) Top and bottom views





Custom Dual in row package for low bond wire parasitics



New Development: 12b, 50MSPS, 9mW ADC for Cryogenic Operation

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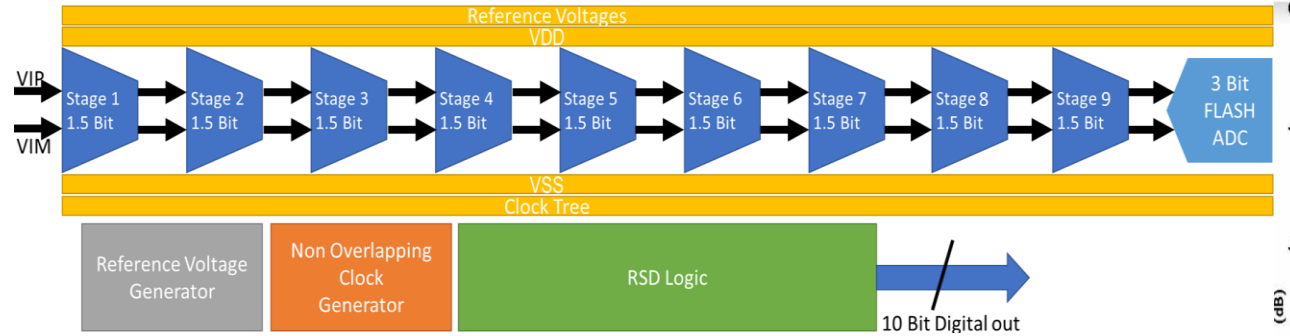
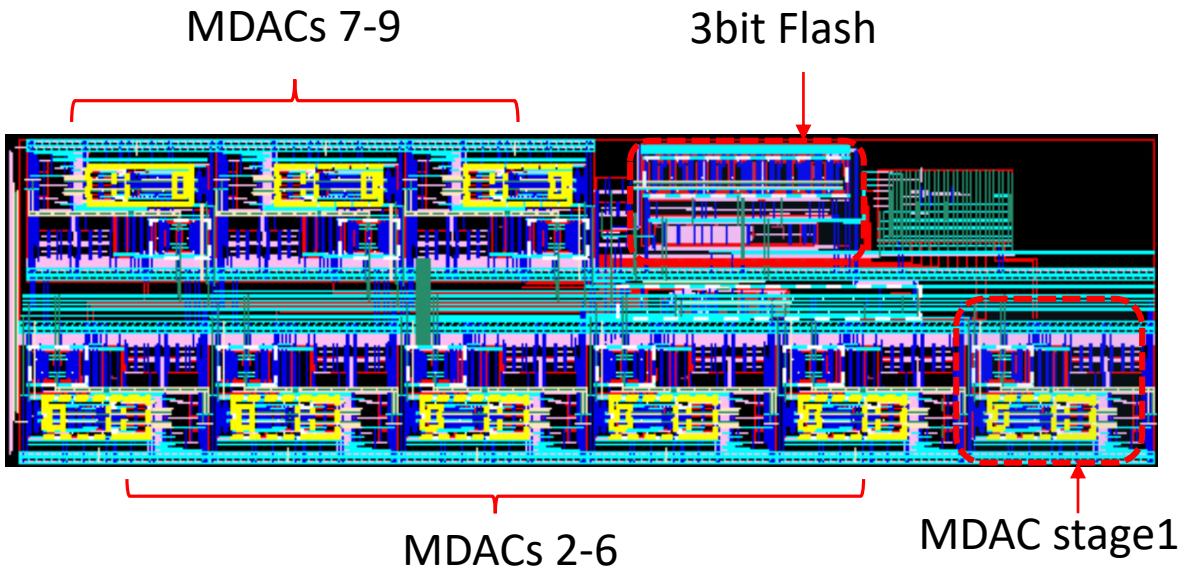
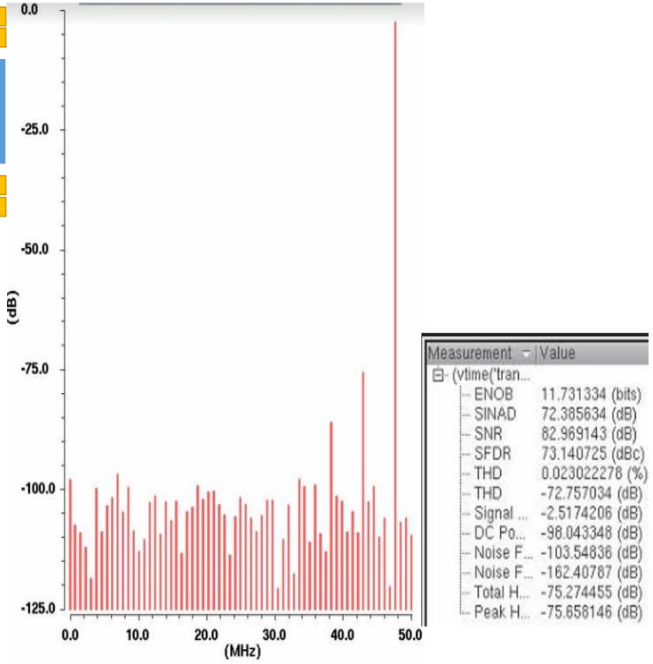


12-bit pipeline ADC architecture

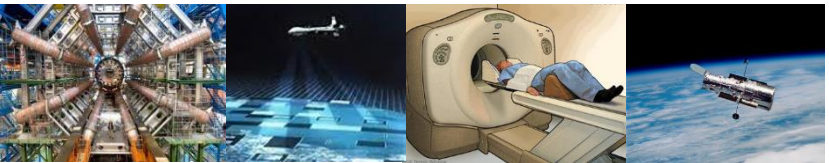


12-bit pipeline ADC layout



FFT

This rad-hard ADC is designed with 77K (cryogenic operation) transistor models. Available in ON Semiconductor 180nm CMOS process. Chips will arrive in December 2018.



Picosecond Timing Measurement IC for Particle Physics Experiments

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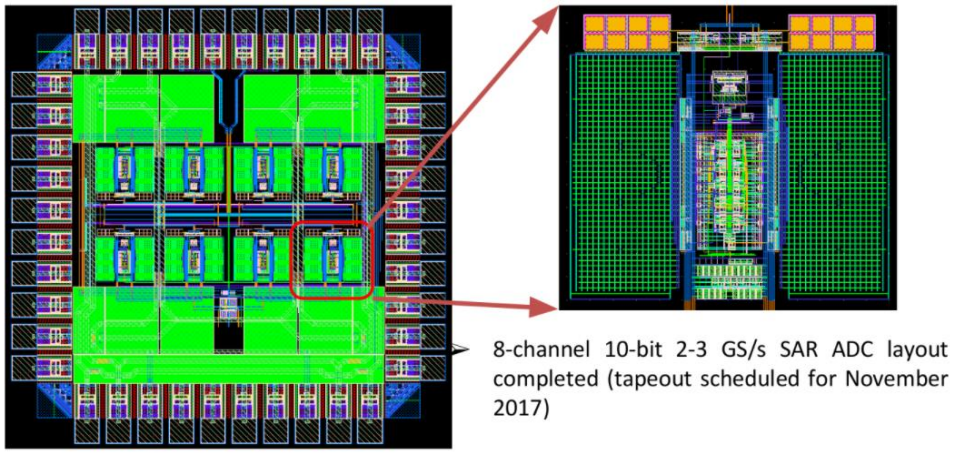
Requirement: IC for accurate timing measurements and transient digitization 1 - 10 GSPS, timing resolution <1ps, conversion resolution > 9 ENOB, and power < 1W.



8-channel 10-bit 2-3 GS/s SAR ADC layout completed (tapeout scheduled for November 2017)

Layout of Alphacore's high-speed, high-resolution SAR ADC

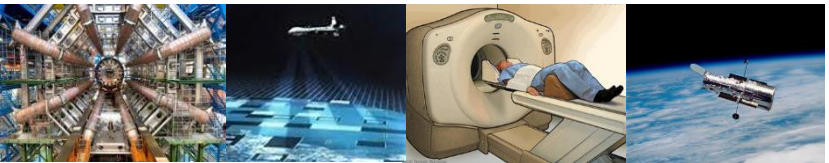
Status: Chips will arrive for testing this week !

DOE SBIR Phase II

Key Features:

- Innovative successive approximation register (SAR) analog-to-digital converter (ADC)
- Fully continuous ADC with no sample buffer depth or dead-time limitation.
- Jitter and time-skew both < 100fs

Specification	Alphacore's ADC
Sampling Speed (GSPS)	1 - 10
Analog Bandwidth, 3dB (GHz)	>5
Resolution	10
ENOB	8.5 (at 10GSPS and 5GHz)
Unit ADCs per chip	4 x 8
Aperture Jitter, random (RMS)	80fs
ENOB (at 1GHz, random jitter included)	>8.6
Radiation hardness	>300 krad
Power (per channel) (mW)	<200 (at f_s = 10GSPS) <70 (at f_s = 3GSPS)
Buffer depth (points per sample)	Unlimited
Latency (ns)	3
Interface type and total output rate	8b/10b encoded, serialized CML, 125Gb/s
CMOS node	28nm



Fully Continuous Real-Time ADC vs. Switched Capacitor Array Digitizer

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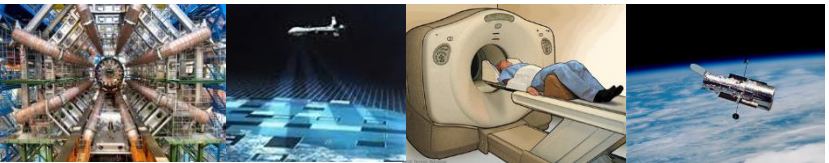
Specification	Alphacore's Continuous 180nm CMOS ADC	Alphacore's 28nm CMOS Switched-Capacitor Array Digitizer	Alphacore's Continuous 28nm CMOS ADC
Resolution (bits)	10-12	10 - 12	10
Sampling rate	100 MSPS	1 – 6 GSPS	1-10 GSPS
Input bandwidth	100MHz	>3GHz	>5GHz
Channels per chip	8	8	4
Power per channel	70mW	<10mW	70mW
Deadtime between inputs pulses	10ns	500ns	3ns
Maximum input pulse rate	50MHz	2MHz (up to 10MHz with higher power)	1.5GHz
Sampling buffer depth	Infinite	1,024	Infinite
Time skew	300fs	<2ps	80fs
Jitter	300fs	<2ps	80fs
Price per channel for 2,000 channels	$40	~$100	<$200
Price per channel for 20,000 channels	$15-20	~$30	~$50
Price per channel for 100,000 channels	~$10	~$25	<$40
Current status	Taped out	Schematic-level design	Taped out

Note that preamplifiers have comparable or lower per-channel pricing than the 180nm ADC.

Questions: Is a GHz digitizer IC needed as well? Will pulse rate be >10MHz in any experiment ? Is a switched capacitor array digitizer with 500ns deadtime a good match to the applications ?



Rad-Hard High-Speed Camera

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Requirement: A triggerable, high speed imaging chip and a complete camera system for investigating rapidly occurring phenomena in radiation environments. The primary application is beam monitoring in accelerator facilities.

Key specs include:

- 1 Megapixel
- 20µm x 20µm pixel size
- 10,000 frames per second continuous video output
- 120Gb/s total output data rate
- Low-noise pinned photodiodes
- ADC ENOB = 10.3 bits
- The chip has 8,000 X 12b, 3MSPS ADCs
- 300krad(Si) radiation tolerance

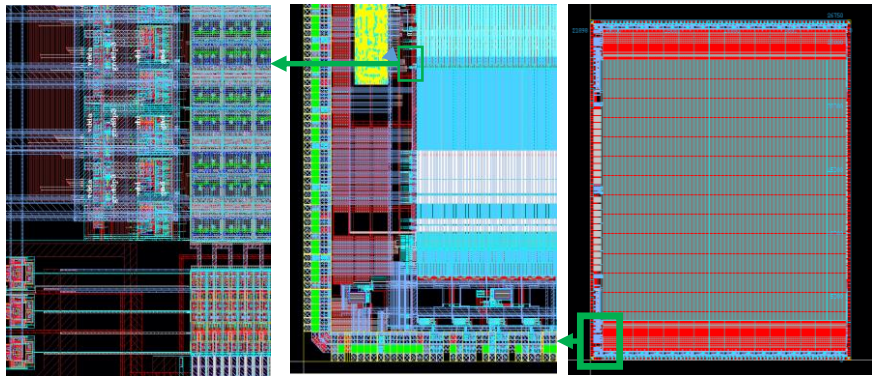
Status 10,000-pixel, 10,000FPS image sensor and camera tested and fond functional. 1Mpix, 10,000FPS version of the image sensor taped out in September 2018.

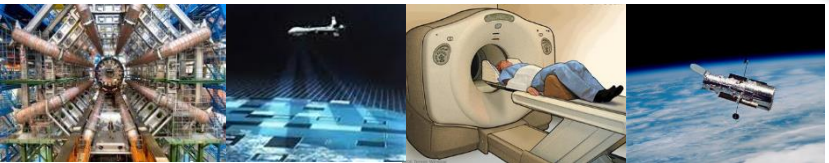
DOE SBIR Phase I & Phase II

Zoom: Px array, column bias, row decoders, …

Zoom: Pixels, column ADCs, PLL, …

Full 1 Mpx chip 27mm x 22mm



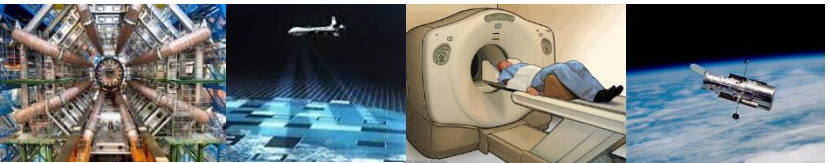


Summary

- Alphacore presented the current status of detector readout IC development including rad-hard preamplifiers, ADCs and combined ROICs.
- Large tapeout was completed and IC testing will start in January 2019.

Questions for the audience?

- **Is there a need for a "Combined ROIC", i.e. a chip that has both preamplifiers and ADCs, or can they be on separate chips?**
- **What are the target experiments, their schedule, channel counts, and readout specifications?**
- **Radiation hardness requirements?**
- **Integration level requirements (IP? Wafers? Packaged chips? Packaged and tested chips? Evaluation boards? Ready-made readout boards with FPGAs ?)**




Questions/Comments for Alphacore?

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