Multi-Channel Readout ICs
Development Status

Streaming Readout Meeting
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Founded in 2012 and located in Arizona’s “Silicon Desert”

Providing technology that enable major advances in:

- Homeland Security
- Defense
- Aerospace
- Scientific Research
- Medical Imaging

Product areas span:

- High performance analog and mixed signal
- High-speed visible light and infrared camera systems
- Radiation-hard electronics
Alphacore’s team is a combination of engineering and business professionals with long histories of delivering products and services to customers who demand state-of-the-art performance.

Our team has had successful careers at companies ranging from start-ups to multinationals including Raytheon, Texas Instruments, Analog Devices, Bell Labs, Intel, United Technologies, and Honeywell.
The need

“Universal”, low-cost, high-performance, readout integrated circuits (ROICs) for several planned nuclear physics experiments

Key features include:

• 1-channel, 8-channel and 16-channel ICs
• Three types of ICs: 1) Preamplifiers, 2) ADCs and 3) Combined ROICs
• 300-800ENC CSA preamplifier for $Cd = 0 - 50\text{pF}$
• 1,300ENC current conveyer preamplifier for $Cd = 0 - 300\text{pF}$
• 12-bit pipeline ADC, 100-200 MSPS, 70mW
• 10-bit pipeline ADC, 50-100 MSPS, $<10\text{mW}$
• Low-cost 180nm CMOS fabrication TID > 300krad
• SEL, SEU, SEFI hardened
• Non-ionizing energy loss (NIEL) > $2 \times 10^{13}$
• First full engineering run tape out finalized in September 2018 in the XFAB 180nm process
• Chips coming back for testing in January 2019
Preamplifier Info

Figure 1: (a) Alphacore's preamplifier architecture, (b) CSA1 charge sensitive pre-amp + shaper (c) CSA2, current conveyer amplifier + shaper

Figure 2: a) Alphacore’s test chip to characterize the CSAs b) transient simulations of CSAs for varying input current pulses c) comparison of ENC of CSA1 and CSA2.
Figure 3: Alphacore’s test chips sent for fabrication to measure performance of 12bit 100MS/s ADC (left) and 10bit 50MS/s ADC (right) in different configurations (including time-interleaving). A total of three different layouts are sent for fabrication to test various configurations of the ADCs.

Figure 4: FFT response of 12bit, 100MS/s and 10bit, 50MS/s ADCs
Provides robust 800Mb/s, or 1.6Gb/s speeds per single I/O pair.

Figure 6: a) Alphacore’s serializer layout and b) programmable eye height for easy signal swing matching to FPGA receiver.

Figure 7: 400MHz – 800MHz PLL layout
Wide functionality testing will be performed with lab equipment and COTS ADC evaluation boards.
Preparation for Chip Evaluations, Status (2/2)

PCB schematic for ADC (both 12 and 10 bits) boards

Board (under development)
Top and bottom views

Custom Dual in row package for low bond wire parasitics
New Development: 12b, 50MSPS, 9mW ADC for Cryogenic Operation

12-bit pipeline ADC architecture

MDACs 7-9
3bit Flash

MDACs 2-6
12-bit pipeline ADC layout

FFT
This rad-hard ADC is designed with 77K (cryogenic operation) transistor models. Available in ON Semiconductor 180nm CMOS process. Chips will arrive in December 2018.
Picosecond Timing Measurement IC for Particle Physics Experiments

**Requirement:** IC for accurate timing measurements and transient digitization 1 - 10 GSPS, timing resolution <1ps, conversion resolution > 9 ENOB, and power < 1W.

**Key Features:**
- Innovative successive approximation register (SAR) analog-to-digital converter (ADC)
- Fully continuous ADC with no sample buffer depth or dead-time limitation.
- Jitter and time-skew both < 100fs

<table>
<thead>
<tr>
<th>Specification</th>
<th>Alphacore's ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Speed (GSPS)</td>
<td>1 - 10</td>
</tr>
<tr>
<td>Analog Bandwidth, 3dB (GHz)</td>
<td>&gt;5</td>
</tr>
<tr>
<td>Resolution</td>
<td>10</td>
</tr>
<tr>
<td>ENOB</td>
<td>8.5 (at 10GSPS and 5GHz)</td>
</tr>
<tr>
<td>Unit ADCs per chip</td>
<td>4 x 8</td>
</tr>
<tr>
<td>Aperture Jitter, random (RMS)</td>
<td>80fs</td>
</tr>
<tr>
<td>ENOB (at 1GHz, random jitter included)</td>
<td>&gt;8.6</td>
</tr>
<tr>
<td>Radiation hardness</td>
<td>&gt;300 krad</td>
</tr>
<tr>
<td>Power (per channel) (mW)</td>
<td>&lt;200 (at $f_s = 10$GSPS)</td>
</tr>
<tr>
<td></td>
<td>&lt;70 (at $f_s = 3$GSPS)</td>
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<tr>
<td>Buffer depth (points per sample)</td>
<td>Unlimited</td>
</tr>
<tr>
<td>Latency (ns)</td>
<td>3</td>
</tr>
<tr>
<td>Interface type and total output rate</td>
<td>8b/10b encoded, serialized CML, 125Gb/s</td>
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<tr>
<td>CMOS node</td>
<td>28nm</td>
</tr>
</tbody>
</table>

**Layout of Alphacore’s high-speed, high-resolution SAR ADC**

**Status:** Chips will arrive for testing this week!
## Fully Continuous Real-Time ADC vs. Switched Capacitor Array Digitizer

<table>
<thead>
<tr>
<th>Specification</th>
<th>Alphacore’s Continuous 180nm CMOS ADC</th>
<th>Alphacore’s 28nm CMOS Switched-Capacitor Array Digitizer</th>
<th>Alphacore’s Continuous 28nm CMOS ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution (bits)</td>
<td>10-12</td>
<td>10 - 12</td>
<td>10</td>
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<tr>
<td>Sampling rate</td>
<td>100 MSPS</td>
<td>1 – 6 GSPS</td>
<td>1-10 GSPS</td>
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<tr>
<td>Input bandwidth</td>
<td>100MHz</td>
<td>&gt;3GHz</td>
<td>&gt;5GHz</td>
</tr>
<tr>
<td>Channels per chip</td>
<td>8</td>
<td>8</td>
<td>4</td>
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<tr>
<td>Power per channel</td>
<td>70mW</td>
<td>&lt;10mW</td>
<td>70mW</td>
</tr>
<tr>
<td>Deadtime between inputs pulses</td>
<td>10ns</td>
<td>500ns</td>
<td>3ns</td>
</tr>
<tr>
<td>Maximum input pulse rate</td>
<td>50MHz</td>
<td>2MHz (up to 10MHz with higher power)</td>
<td>1.5GHz</td>
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<tr>
<td>Sampling buffer depth</td>
<td>Infinite</td>
<td>1,024</td>
<td>Infinite</td>
</tr>
<tr>
<td>Time skew</td>
<td>300fs</td>
<td>&lt;2ps</td>
<td>80fs</td>
</tr>
<tr>
<td>Jitter</td>
<td>300fs</td>
<td>&lt;2ps</td>
<td>80fs</td>
</tr>
<tr>
<td>Price per channel for 2,000 channels</td>
<td>$40</td>
<td>~$100</td>
<td>&lt;$200</td>
</tr>
<tr>
<td>Price per channel for 20,000 channels</td>
<td>$15-20</td>
<td>~$30</td>
<td>~$50</td>
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<td>Price per channel for 100,000 channels</td>
<td>~$10</td>
<td>~$25</td>
<td>&lt;$40</td>
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<tr>
<td>Current status</td>
<td>Taped out</td>
<td>Schematic-level design</td>
<td>Taped out</td>
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</table>

Note that preamplifiers have comparable or lower per-channel pricing than the 180nm ADC.

Questions: Is a GHz digitizer IC needed as well? Will pulse rate be >10MHz in any experiment? Is a switched capacitor array digitizer with 500ns deadtime a good match to the applications?
Rad-Hard High-Speed Camera

Requirement: A triggerable, high speed imaging chip and a complete camera system for investigating rapidly occurring phenomena in radiation environments. The primary application is beam monitoring in accelerator facilities.

Key specs include:
- 1 Megapixel
- 20µm x 20µm pixel size
- 10,000 frames per second continuous video output
- 120Gb/s total output data rate
- Low-noise pinned photodiodes
- ADC ENOB = 10.3 bits
- The chip has 8,000 X 12b, 3MSPS ADCs
- 300krad(Si) radiation tolerance

Status 10,000-pixel, 10,000FPS image sensor and camera tested and found functional. 1Mpix, 10,000FPS version of the image sensor taped out in September 2018.

DOE SBIR Phase I & Phase II

Full 1 Mpx chip 27mm x 22mm

Zoom: Pixels, column ADCs, PLL, …

Zoom: Px array, column bias, row decoders, …
Summary

- Alphacore presented the current status of detector readout IC development including rad-hard preamplifiers, ADCs and combined ROICs.
- Large tapeout was completed and IC testing will start in January 2019.

Questions for the audience?

- Is there a need for a “Combined ROIC”, i.e. a chip that has both preamplifiers and ADCs, or can they be on separate chips?
- What are the target experiments, their schedule, channel counts, and readout specifications?
- Radiation hardness requirements?
Questions/Comments for Alphacore?

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