CLAS12 DAQ/Trigger/Online Status

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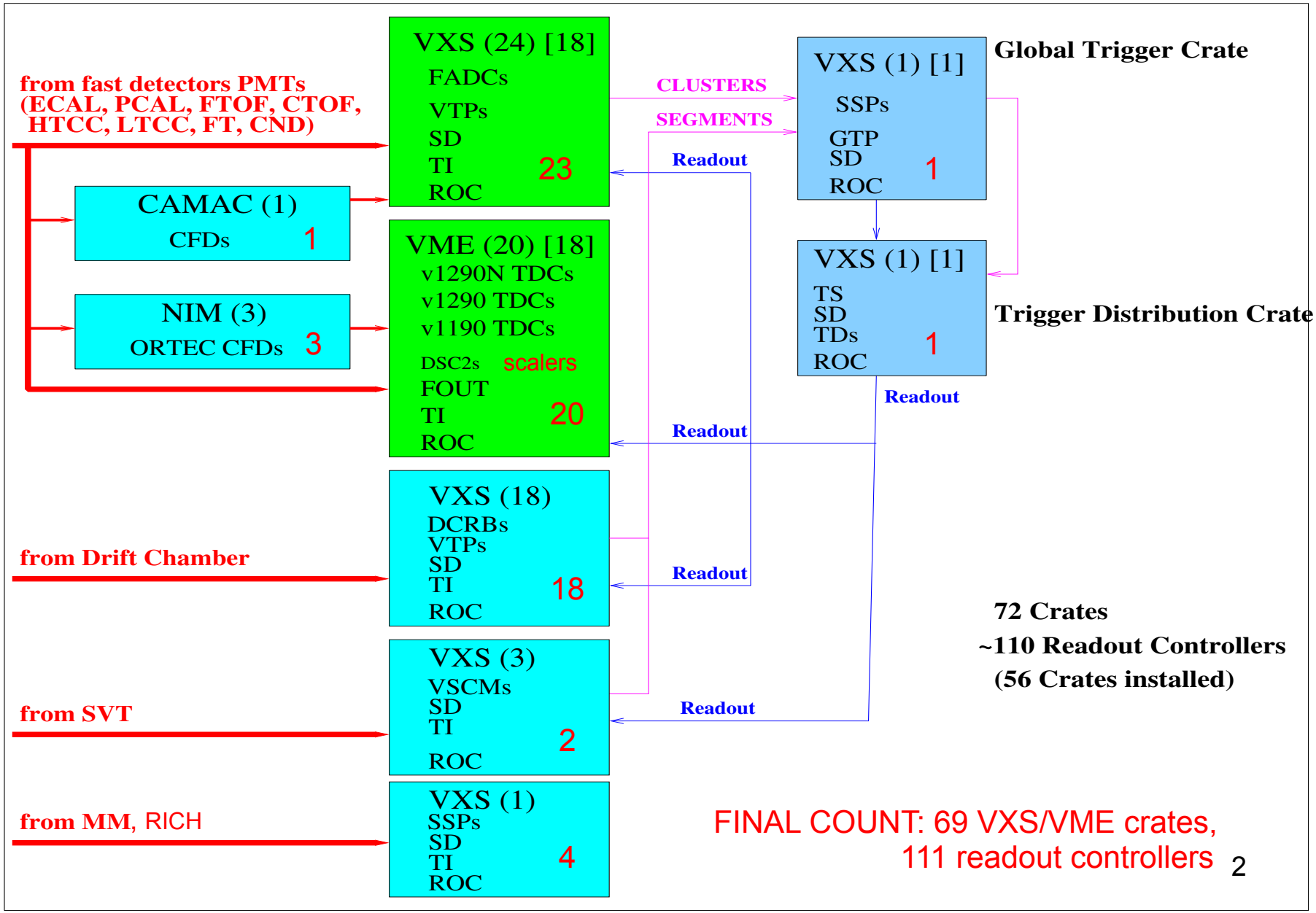
DAQ/Trigger Hardware



CLAS12 DAQ Status

- Detectors supported: ECAL, PCAL, FTOF, LTCC, DC, HTCC, CTOF, CND, SVT, MM, FT/HODO, RICH
- Online computer cluster: 30+ computers, 4 DAQ servers
- Networking: 1 router, 20+ switches, 40GBit to CC
- DAQ software is operational, reliability is acceptable
- 50nA beam: 12kHz event rate, 600MByte/sec data rate, 90% livetime
- Move to tape: up to 1500MByte/sec

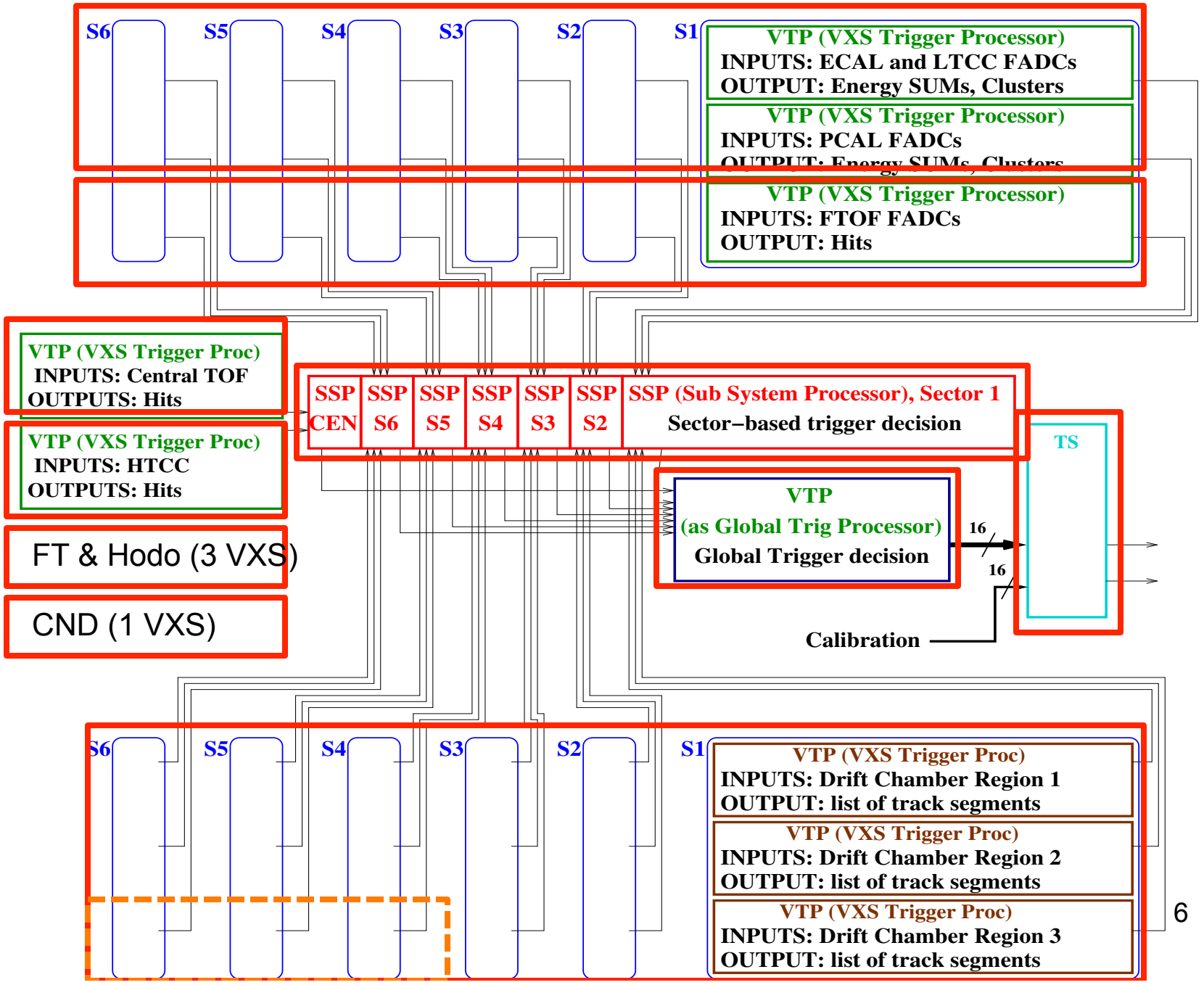
DAQ requirements, current status and plans

DAQ parameter	Electron trigger requirement	Electron/ hadron trigger requirement	Current status	Plan for the fall of 2018
Event rate (kHz)	10kHz	20kHz	12kHz	20kHz
Data rate (Mbyte/sec)	100MB/s - 200MB/s	400MB/s	600MB/s	1200MB/s
Livetime (%)	>90%	>90%	>90%	>90%
Online monitoring	CED, data monitoring, rcdb, scalers	+ Trigger monitoring	+ scalers and histos over messaging	+ more info
Online data processing		temporary on DAQ machine	First online farm machine in CC	Online farm in CC

CLAS12 DAQ Remaining Work

- bug fixes (collecting information, will be addressed after the run, mostly in front-end electronics firmware)
- Restore spare electronics pool (originally planed 5-10% spares, now hope for at least 2-3%)
- Buy faster/bigger event recorder server (have 35TB storage vs HallD >150TB with comparable data rate)
- Upgrade back-end software to increase data rate

CLAS12 Trigger System Logic



CLAS12 Trigger status

- Stage 1: ECAL, PCAL, HTCC, FTOF, CTOF, FT/HODO - operational
- Stage 1: CND – operational, calibration in progress
- Stage 1: DC segment finder and superlayer multiplicity − operational
- Stage 2: FTOF-PCAL(U) geometry match - operational
- Stage 2, stage 3: timing match/multiplicity/logic – operational
- Validation process underway, procedures established and producing useful feedback allowing to implement new components and fix problems
- The number of different trigger configurations were prepared and used during er-a/b and rg-a runs, parameter setting procedures were developed (FADC thresholds, FADC pedestals, FADC delays, stage 1/2/3 thresholds and width/delays, delay scans, config files etc)

CLAS12 Trigger Remaining Work

- Fix broken VTP boards
- Continue system validation using beam data, including random pulser runs
- Add more monitoring and control components (readout from all VTP boards, more scalers and histograms over messaging, convenient delay scan procedures, built-in scopes etc)
- New trigger components (DC road finder)
- Need better communication between trigger development and offline reconstruction suites

Online Status and Work

- Available computing hardware is almost sufficient, need bigger data server
- Available software: process monitoring and control, CLAS event display, data collection from different sources (DAQ, EPICS, scalers etc) and data recording into data stream, online data monitoring
- Runtime database (RCDB) is running
- ‘Online farm’ issue to be resolved, need farm in CC (one rack, 10 machines scale), one machine is installed and under testing

Conclusion

- DAQ, computing and network works as expected meeting original CLAS12 requirements; performance will be increased to meet growing demands; reliability problems remains and will be addressed
- Trigger system works as expected; some parts to be finished; trigger structure will be constantly improving to meet experiment demands
- Online software is ready in general, available tools allows to run; online farm will significantly improve prompt data processing

Notation

- ECAL – old EC (electromagnetic calorimeter)
- PCAL – preshower calorimeter
- DC – drift chamber
- HTCC – high threshold cherenkov counter
- FT/HODO – forward tagger and hodoscope
- TOF – time-of-flight counters
- MM – micromega tracker
- SVT – silicon vertex tracker
- VTP – VXS trigger processor (used on trigger stage 1 and stage 3)
- SSP – subsystem processor (used on trigger stage 2)
- FADC – flash analog-to-digital converter
- FPGA – field-programmable gate array
- VHDL – VHSIC Hardware Description Language (used to program FPGA)
- Xilinx – FPGA manufacturer
- Vivado_HLS – Xilinx High Level Synthesis (translates C++ to VHDL)
- Vivado – Xilinx Design Suite (translates VHDL to binary image)
- GEMC – CLAS12 GEANT4-based Simulation Package
- CLARA – CLAS12 Reconstruction and Analysis Framework
- DAQ – Data Acquisition System