

SAMPA ASIC and Test Stand

TDIS Workshop - 2/22/18
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DAQ Group

“**SAMPA**” - nickname for the city of São Paulo, Brazil

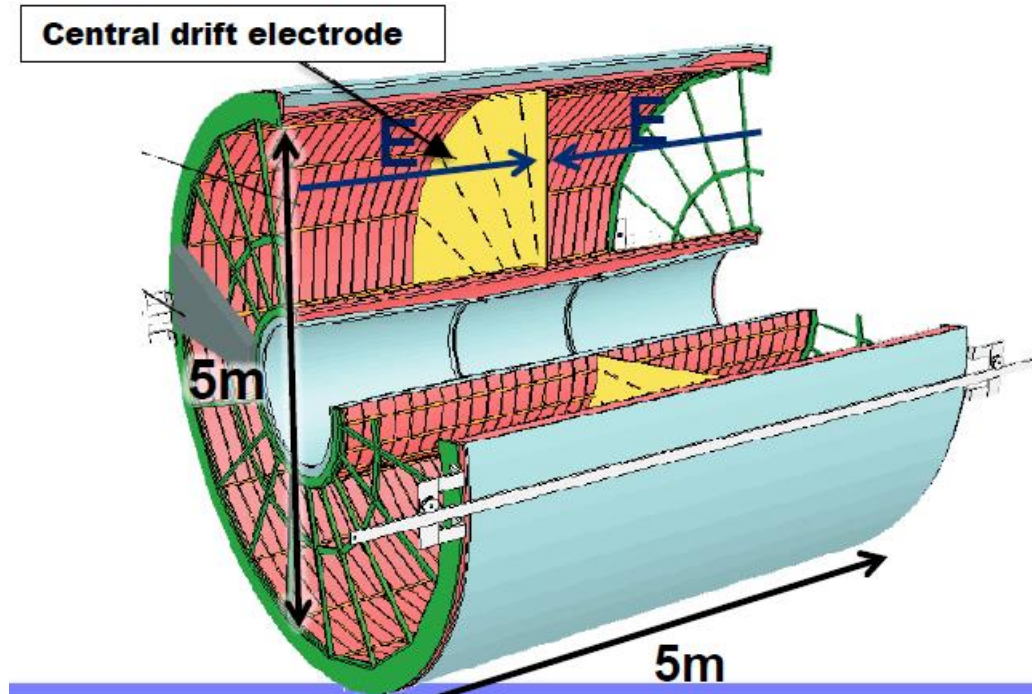
- New ASIC for the ALICE TPC and Muon Chamber (MCH) upgrades
- Combines functions of the **PASA** (analog) and **ALTRO** (digital) chips currently being used
- Design effort led by University of São Paulo, Brazil
- Chosen for TPC readout by sPHENIX and STAR upgrade at RHIC
- ALICE alone > 50,000 chips (1.5 M channels)
- All plan to use **continuous readout mode** for their TPCs

Useful Sources of Information

- TDRs for the Upgrade of ALICE
 - <https://cds.cern.ch/record/1622286/files/ALICE-TDR-016.pdf>
 - <http://cds.cern.ch/record/1603472/files/ALICE-TDR-015.pdf>
- Other
 - https://www.bnl.gov/aum2014/content/workshops/Workshop_1/bnl_david_silvermyr.pdf
 - <http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7031978>
 - <http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7543104>
- SAMPA chip prototype tests
 - <http://iopscience.iop.org/article/10.1088/1748-0221/12/04/C04008/pdf>
 - <http://iopscience.iop.org/article/10.1088/1748-0221/11/02/C02088/pdf>

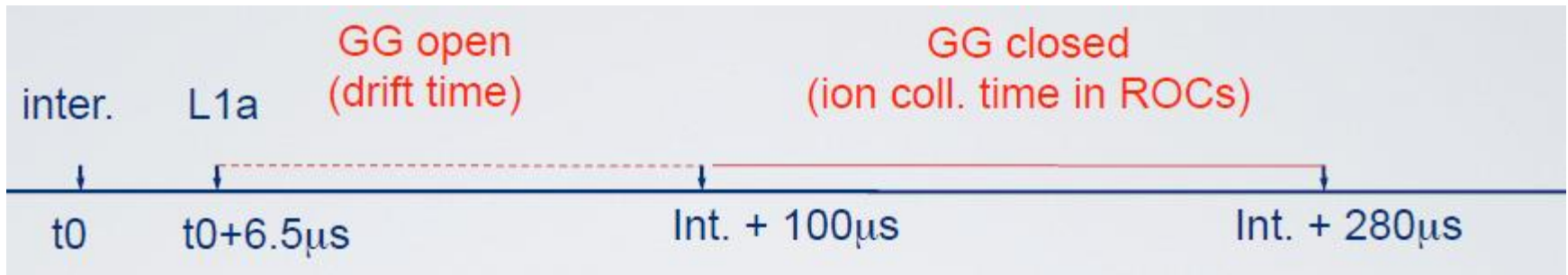
- Collection of links to up-to-date SAMPA technical documents
 - <https://docs.google.com/spreadsheets/d/16SnfEWtvvZYONnxmMhVzUo-St-ZtPRVV3Z6mfy13dRU/edit?usp=sharing>

Background - ALICE TPC



Volume = 90 cubic meters (largest in world)
~ 100 us electron drift time (90% Ne – 10% CO₂)
Current detector – MWPC (end plates) (0.5 M channels)

ALICE TPC



ROC = Read out chamber

Active Gating Grid - trigger causes grid to be transparent, allowing ionization electrons to pass into the amplification region. After 100 μs , Gating Grid is biased with alternating voltage that renders grid opaque to electrons and ions. This protects the amplification region against unwanted ionization from the drift region, and prevents back-drifting ions from entering the drift volume (leading to drift-field distortion).

Trigger rate limited to 3.5 KHz

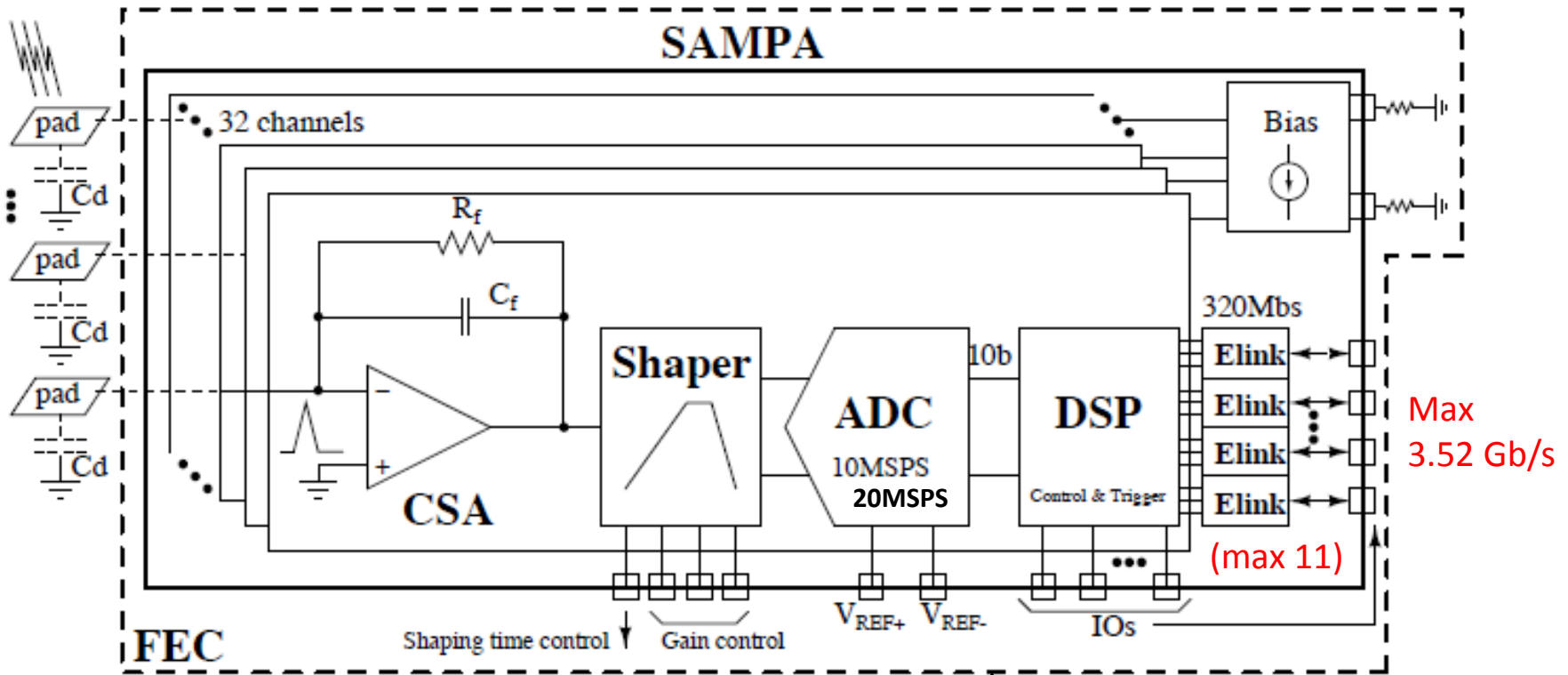
LHC Luminosity Upgrade

- LHC Run 3 (**2021**) → 50 KHz interaction rate (Pb-Pb)
- ~ 5 events (100 us * 50 KHz) concurrent in TPC volume
- TPC Gating grid would cause large loss of data
- Replace MWPC with **quad-layer GEM detectors** (resistant to backflow of ions into drift volume).
- Continuous readout of TPC data desirable (~1 TByte/s)
- **New ASIC developed** – requirements set to meet needs of both TPC and Muon chambers

SAMPA Status

- Developers are currently evaluating latest engineering batch of SAMPA chips (V3, V4)
- Production run should be at the end of 2nd quarter 2018

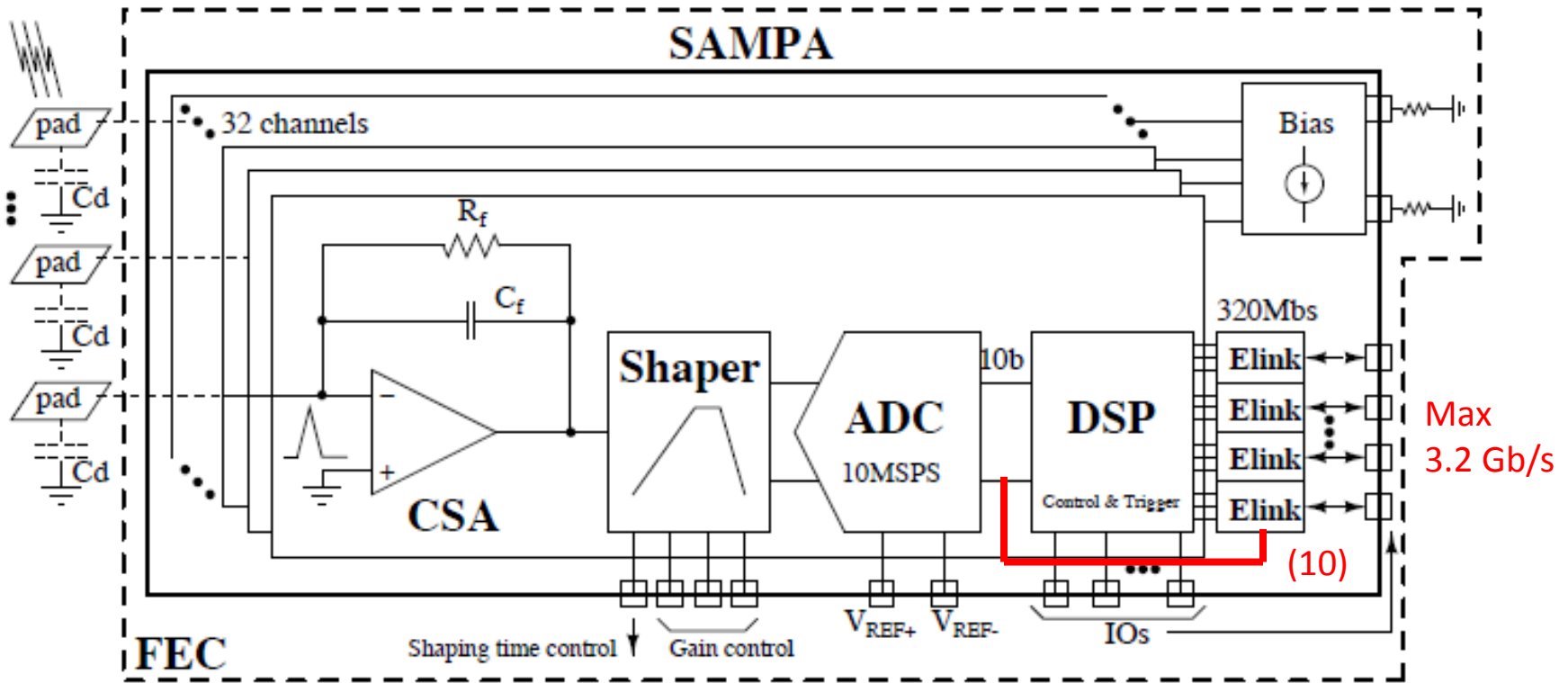
SAMPA Block Diagram



Max
3.52 Gb/s

$$\begin{aligned} \text{Raw data rate (10MHz)} &= 32\text{ch} \times 10\text{b} \times 10\text{M/s} = 3.2\text{Gb/s} \\ &\quad (20\text{MHz}) \qquad \qquad \qquad = 6.4\text{Gb/s} \end{aligned}$$

SAMPA Block Diagram



Max
3.2 Gb/s

(1 Elink for synchronization)

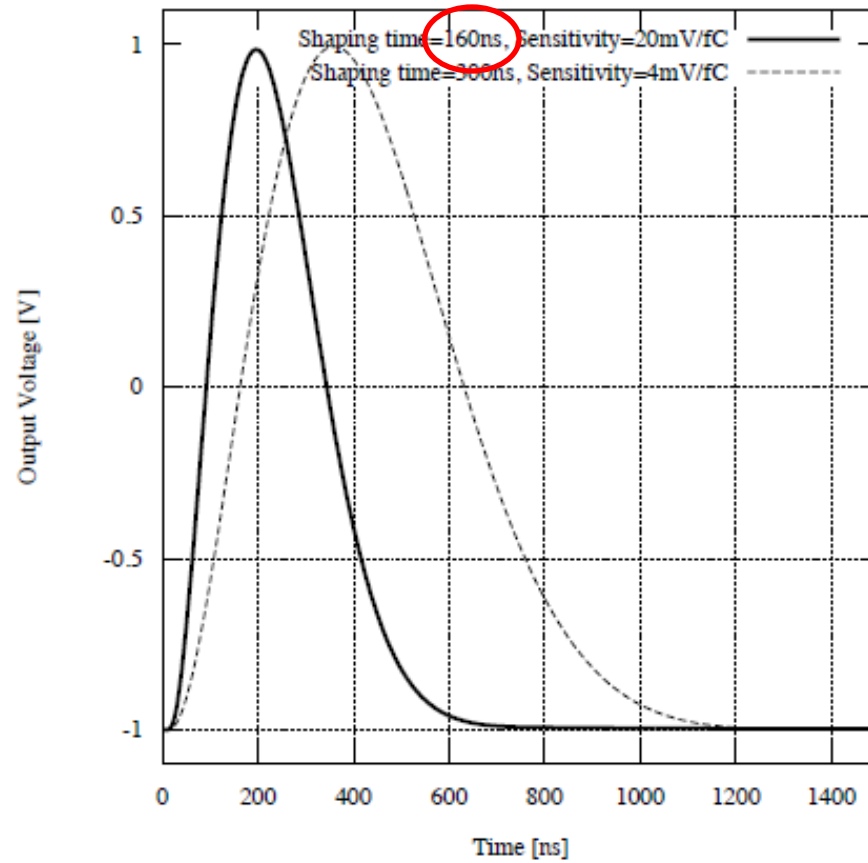
Direct Mode – bypass DSP

(Raw data rate (10MHz) = 3.2Gb/s)

Functional Blocks

- Charge Sensitive Amplifier (CSA)
 - Integrates and amplifies short current pulse
 - Output is a Voltage signal with amplitude proportional to the total charge Q
 - Tail of Voltage pulse is long ($T = R_f * C_f$)
 - Vulnerable to pile-up unless followed by a shaping filter
- Shaper
 - Creates a 4th order semi-Gaussian pulse shape
 - Available shaping times (TS): ~~80~~, 160, 300 ns
 - Permits sampling by ADC at reasonable rates (10, 20 MHz)
 - 80 ns option eliminated in order to reduce noise in CSA

Pulse from Shaper



Functional Blocks

- ADC
 - 10 bit precision
 - 10 MSPS or 20 MSPS
 - SAR architecture for low power (Successive Approximation Register)
 - ADC data rate = 10 MSPS * 10 bits * 32 channels = 3.2Gb/s (6.4 Gb/s)
- DSP
 - Baseline Correction 1 (BC1) – removes low frequency perturbations and systematic effects
 - Digital Shaper (DS) – tail cancellation or peaking time correction (IIR filter)
 - Baseline Correction 2 (BC2) – moving average filter
 - Baseline Correction 3 (BC3) – slope based filter (alternative to BC2)
 - Zero suppression – fixed threshold
 - Formatting; encoding for compression – Huffman
 - Buffering (16K x 10 bit)

Functional Blocks

- e-link
 - Electrical interface for transmission of serial data over PCB traces or electrical cables, for distances of several meters
 - Up to 320 Mb/s
 - Developed by CERN for the connection between Front-end ASICs and their GigaBit Transceiver (**GBTx**) chip
 - Based on SLVS standard (Scalable Low-Voltage Signaling) – supply voltage as low as 0.8 V
 - Radiation-hard IP blocks for integration into ASICs
 - SAMPA: 11 e-links → 3.52 Gb/s max data output
 - Number and speed of SAMPA e-links used is programmable

SAMPA Specifications

Specification	TPC	MCH
Voltage supply	1.25 V	1.25 V
Polarity	Negative	Positive
Detector capacitance (Cd)	18.5 pF	40 pF - 80 pF
Peaking time (ts)	160 ns	300 ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 600e@ts=160 ns*	< 950e @ Cd=40 pF* < 1600e @ Cd=80 pF*
Linear Range	100 fC or 67 fC	500 fC
Sensitivity	20 mV/fC or 30 mV/fC	4 mV/fC
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3% @ ts=160 ns	< 0.2% @ ts=300 ns
ADC effective input range	2 V _{pp}	2 V _{pp}
ADC resolution	10-bit	10-bit
Sampling Frequency	10 (20) Msamples/s	10 Msamples/s
INL (ADC)	<0.65 LSB	<0.65 LSB
DNL (ADC)	<0.6 LSB	<0.6 LSB
ENOB (ADC)**	> 9.2-bit	> 9.2-bit
Power consumption (per channel) CSA + Shaper + ADC	< 15 mW	< 15 mW
Channels per chip	32	32

* $R_{esd} = 70\Omega$

** @ 0.5MHz, 10Msamples/s

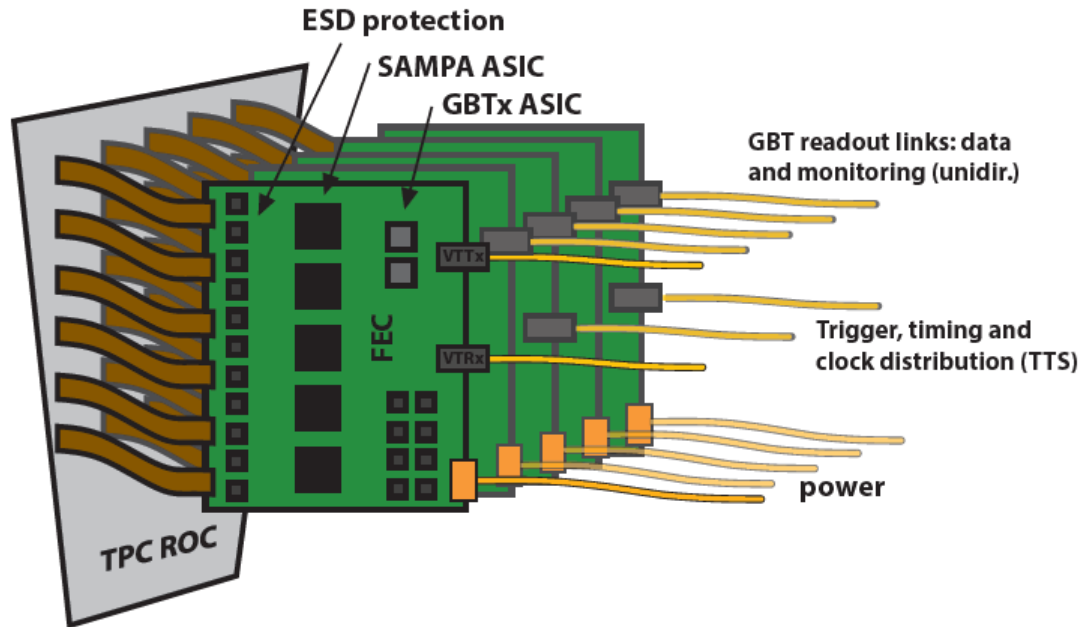
Outlook for TDIS Radial TPC

- Average time between hits on a strip = **120 ns** (worst case) (P.M.King – 6/6/2017)
- Even with peaking time of **80 ns** there would be significant pile-up in the analog front end of the SAMPA chip
- High occupancy will also make it difficult to reduce raw data rate
- SAMPA chip not usable with TDIS radial TPC

Outlook for TDIS mTPC

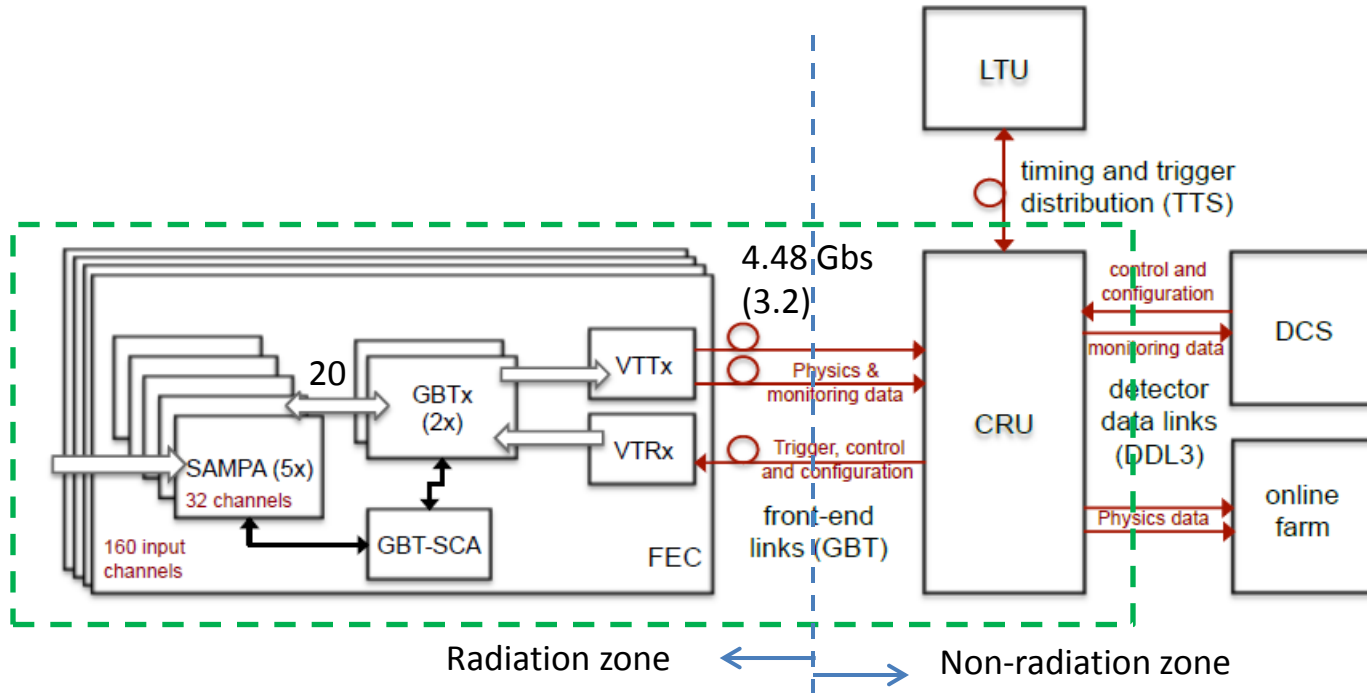
- Average time between hits on a strip = $\sim 1 \text{ us}$ (?) (worst case)
- Even with peaking time of **160 ns** pile-up in the analog front end of the SAMPA chip is manageable
- SAMPA chip readout is possible for mTPC

ALICE Front-end Card (FEC)



Schematic of the readout system of the GEM TPC. Each FEC supports 5 SAMPA chips (160 ch). The **20 e-links** from the SAMPAs are routed into 2 GBTx chips (10 per). Each GBTx drives a fiber transmitter (VTTx) at 3.2Gb/s. Trigger, timing, clock, configuration data, and control commands are received on a separate fiber by a pair of FECs.

ALICE SYSTEM



FEC – Front End Card (160 ch / FEC)

CRU – Common Readout Unit (12 FECs / CRU = 1920 ch / CRU)

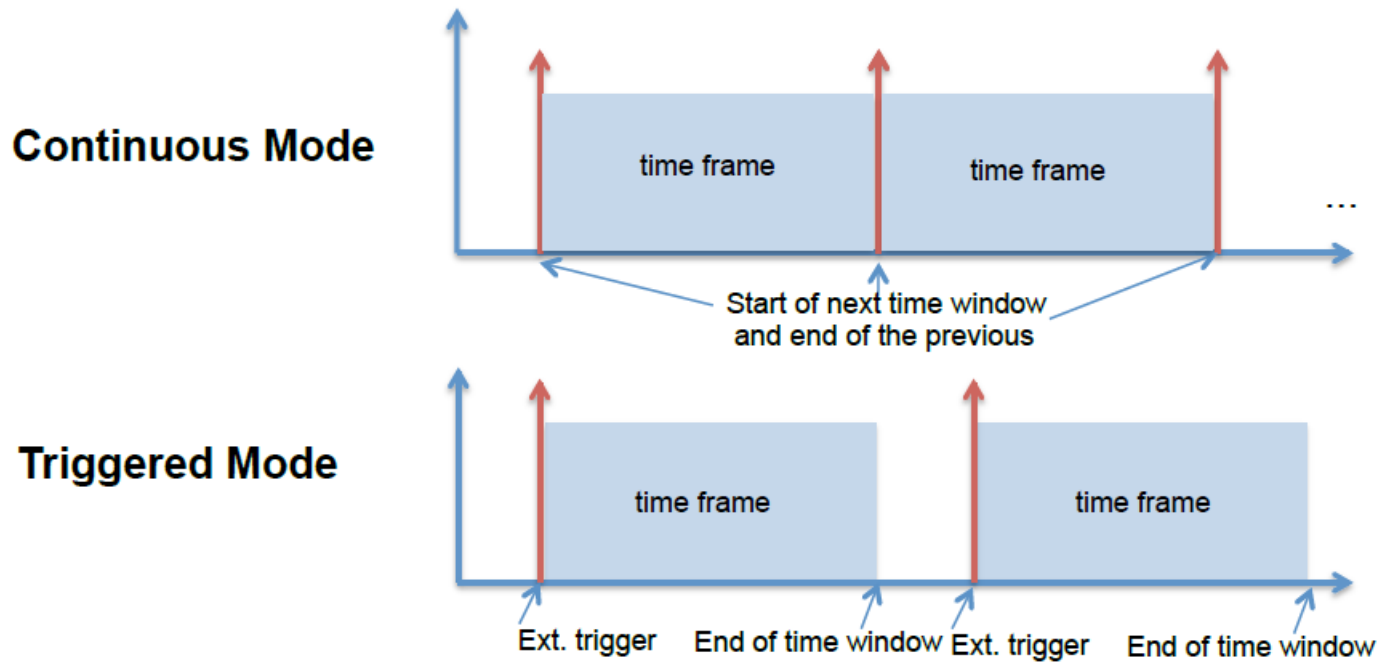
DCS – Detector Control System

LTU – Local Trigger Unit

Common Readout Unit (CRU)

- Interface between the on-detector systems, the online computing system, and the Central Trigger Processor
- Multiplexes data from several front-end links into higher speed data links
- Can do processing on data
- Sends trigger, control, and configuration data to front-ends
- Based on commercial high-performance FPGA
- Located outside of radiation area, so no worry of SEUs
- **PCIe** platform

SAMPA Readout



Each time frame is 1024 samples
102.4 us @ 10 MSPS (~ electron drift time in TPC)
(51.2 us @ 20 MSPS)

SAMPA Readout

- Continuous mode
 - New time frame starts when preceding frame is finished
 - All channels and chips use the same time frame – aligned by the *sync* input of the chip (at startup)
- Triggered mode
 - Time frame starts when external trigger is received
 - Data from ADC can be delayed by up to 192 samples to account for trigger latency
 - All channels use the same time frame
 - All chips that are programmed with the same delay (latency) have time frames that are aligned (assuming triggers are aligned)

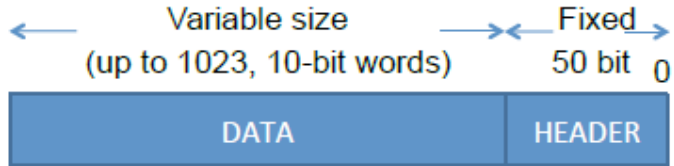
SAMPA Readout (Zero Suppression)

- Cluster – consecutive ADC samples above threshold (> 1)
- pre/post samples can be included in the cluster
(programmable number - same for all channels of chip)
- Clusters are merged if there are up to 2 samples below threshold separating them

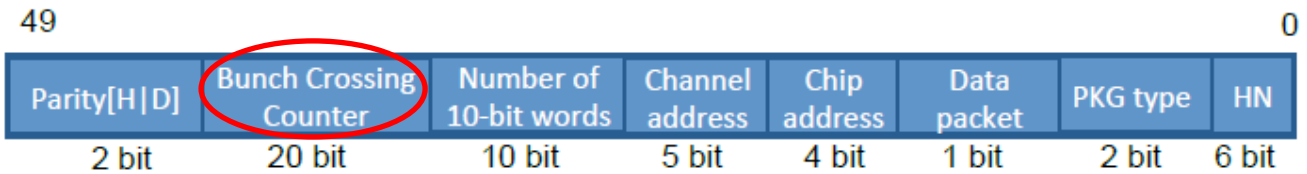
- For each time frame all channels produce their own data packet from the cluster data
- Header for data packet has time stamp (bunch crossing counter)
- Cluster data has time offset (sample number) appended

Data Format

Data packet



Header

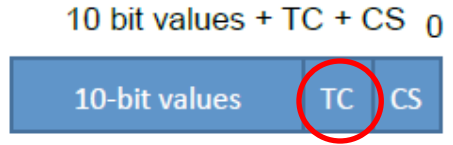


Data

Data contains variable number of clusters



Cluster



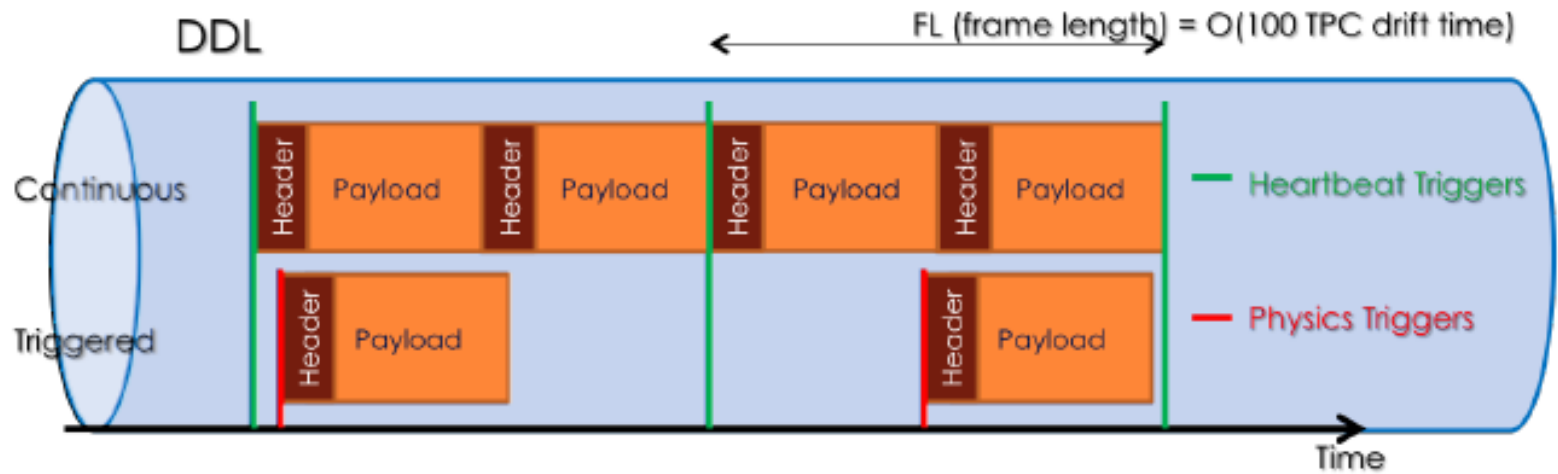
Packet (PKG) type indicates type of data packet:
 Data, heartbeat, synchronisation, channel_fill, data truncated
 HN: Hamming code protection field

CS: Cluster Size
TC: Time Count

Linking Triggered and Continuous Data

- All data packets from both triggered and continuous sources are time stamped with bunch crossing number
- Heartbeat Trigger
 - Non-physics trigger generated by Central Trigger Processor (CTP)
 - Regular frequency, highest priority
 - All detector readout systems respond by inserting a “Heartbeat Event”
 - These events separate the data streams into pieces (heartbeat time frames) that are used in event building
 - Event building nodes get different frames; data associated with trigger near end of frame may extend to *next* frame, so at least part of the next frame must also be sent to node.
 - Can also be used as a synchronization event: by sending global time stamp with heartbeat trigger, detector readout unit can compare with its local time stamp and report/correct difference

Heartbeat Trigger



JLab Test Stand Goal

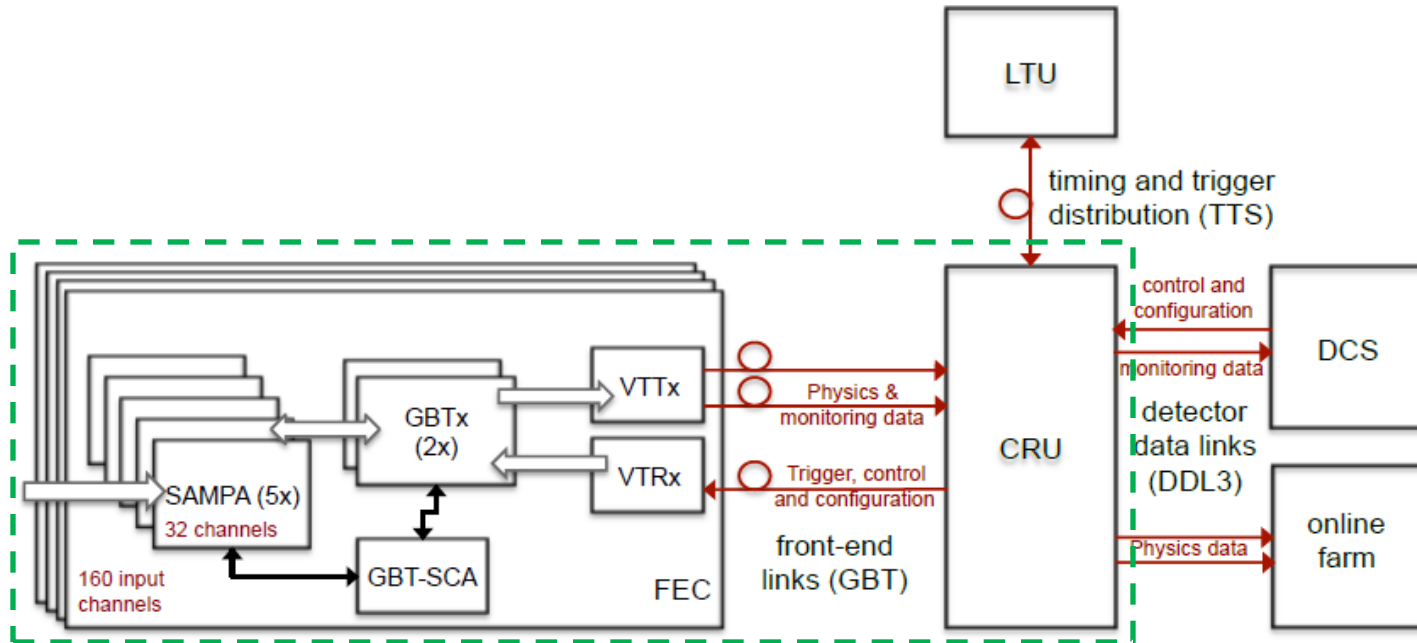
- Determine if the **SAMPA** chip is appropriate for the TDIS TPC as well as other detectors systems at JLab
- To achieve this goal we should:
 - Understand the SAMPA front end response to detector signals
 - Learn how to utilize the complex SAMPA DSP functionality to reduce data volume
 - Deal with a continuous readout data stream and link it with triggered data streams from other sources
- The last point goes beyond the SAMPA chip. Continuous readout systems are expected to be used in many future experiments.

- Ideally we should have a test system that can be scaled up and used for the final detector
- We should be able to connect the test system to an existing detector (e.g. prototype GEM detector at JLab or UVA)
- We should have a mechanism to pulse the inputs in a controlled fashion to study the effects of pileup and high rates on the SAMPA's DSP functions

Pathways

- **From Scratch** – Build a prototype Front-End Card (FEC) for SAMPA chip
 - Use FPGA on FEC to multiplex serial data streams (e-links) from SAMPA(s) into multi-gigabit data stream(s)
 - Optical link to JLab SSP (Sub-System Processor) or similar module for data processing and formatting.
 - For SSP, readout over VME or through VTP (VXS Trigger Processor)
 - Reverse optical link to FEC for programming of SAMPA chip (I2C)
 - Advantages:
 - simple concept
 - some components on hand (SSP, VTP)
 - Disadvantages:
 - hardware and firmware development
 - Non-trivial PCB (mixed-signal design, BGA components)
 - doesn't easily translate to final design due to radiation effects on FPGA and commercial optical transceivers

- **Fast Track** – use as many components of the ALICE TPC readout/control chain as possible



FEC – Front End Card (160 ch / FEC)

CRU – Common Readout Unit (12 FECs / CRU = 1920 ch / CRU)

DCS – Detector Control System

LTU – Local Trigger Unit

Advantages of Fast Track Solution

- System components have been verified and tested together.
- Almost “plug and play”.
- Development is reduced to coding (VHDL for data processing and formatting in FPGA, and software integration into CODA).
- Although the FEC would have to be redesigned to match the detector, the data transport model and sub-components (GBTx, GBT-SCA, VTRx, VTTx) can be used in the final solution.
- The CRU can be used in the final solution.
- What we learn from the test setup can be carried over to the actual system implemented.

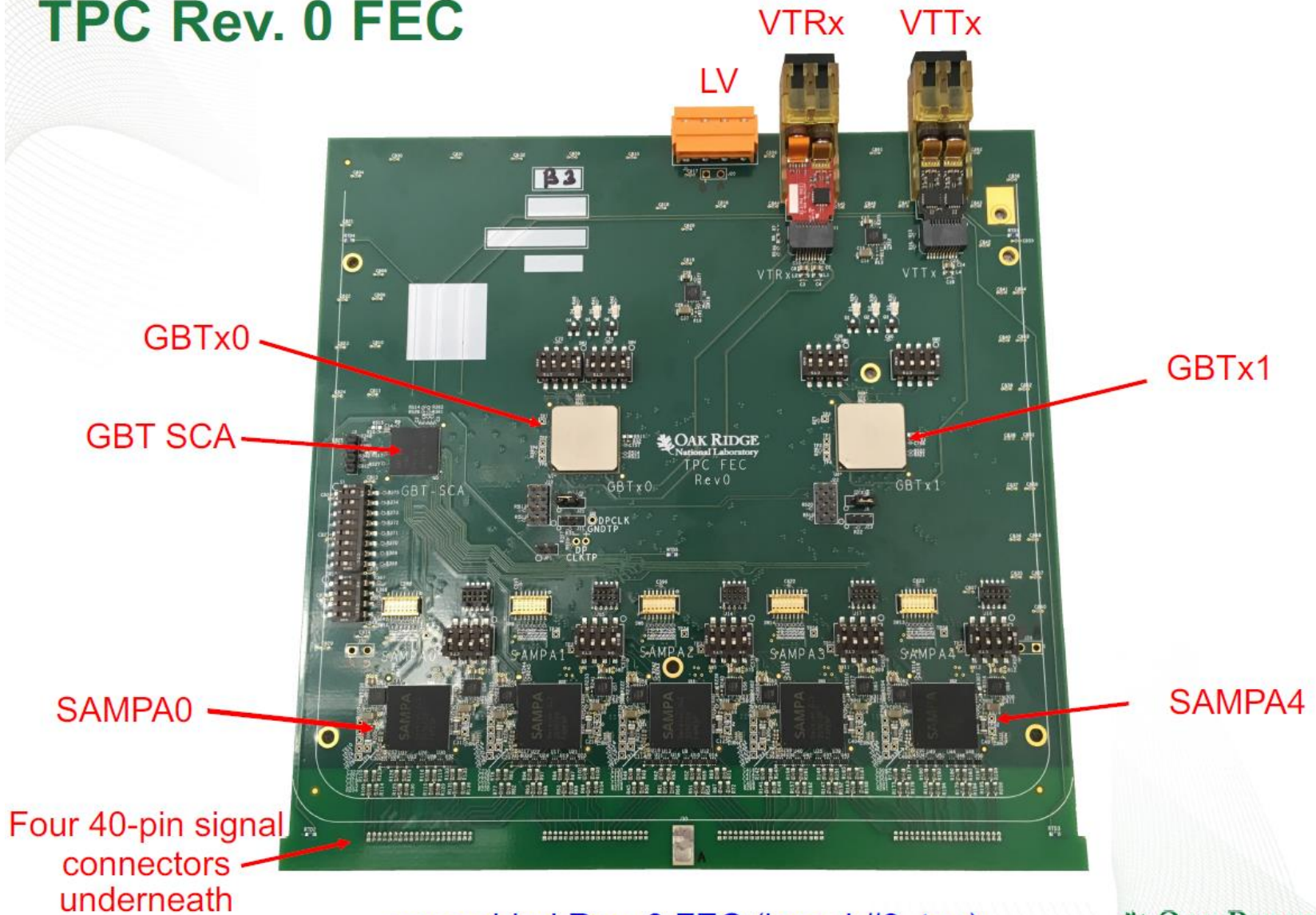
Recommendation

- Fast Track solution
- acquire ~6 FECs and 1 CRU

ALICE Front End Card (FEC)

- **Contact** - Chuck Britton, Oak Ridge National Lab (ORNL) (brittoncl@ornl.gov)
- **Plan**
 - ORNL will give us all manufacturing files and details necessary to duplicate FEC circuit board
 - We purchase the specialized components (SAMPA, GBTx, ...) and have the board assembled
 - Request ORNL to run our assembled FECs through their rigorous testing station (\$).

TPC Rev. 0 FEC



assembled Rev. 0 FEC (board #3, top)

FEC

- To use the ALICE FEC with prototype GEM detectors at JLab or UVA we need to carefully design a cable or flex circuit to map the FEC signal input connectors (4x, 2x20 ERNI, 1.27 pitch) to the detectors.
- Seek guidance from Kondo, Nilanga, and other detector experts for this.

Components

- **SAMPA**

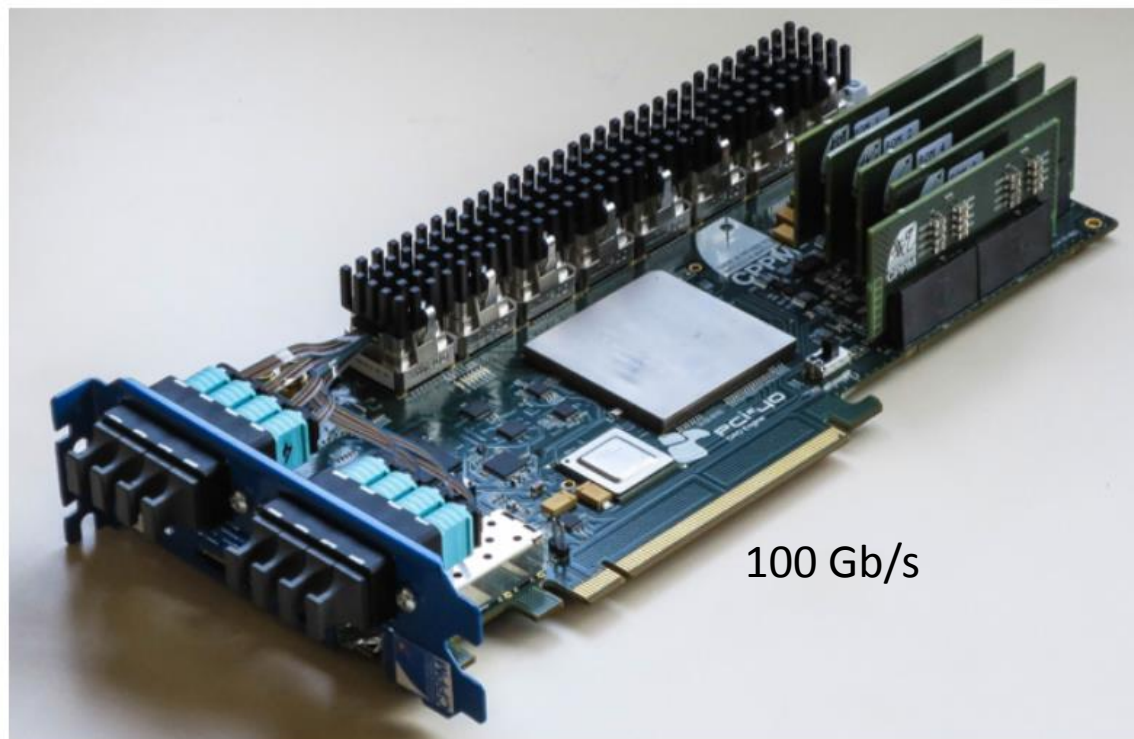
- **Contact** – Marco Bregant, University of São Paulo (USP), ALICE (bregant@if.usp.br)
- Available in small quantities (~25) directly from USP @ **\$30 per chip**
- All ALICE SAMPA chips are tested at Lund before mounting on FEC
- USP will help us connect with Lund for testing (~\$10 per chip)

- **GBTx, GBT-SCA, VTRx, VTTx**

- **Contact** – Philippe Farthouat, CERN, EP Department (Philippe.Farthouat@cern.ch)
- Available in small quantities directly from CERN (**\$ CONFIRMED**)
- GBTx (\$50), GBT-SCA (\$35), VTRx (\$200), VTTx (\$150)
- **\$485 per FEC**

Introduction to CRU (LHCb PCIe40)

- CRU = Common Readout Unit
- PCI Express Gen3 x 16 HBA (Host-Bus-Adapter)
- Based on an ALTERA ARRIA 10 GX FPGA (10AX115S4F45I3SGES)
- Up to 48 optical links via MPO breakout connectors for serial data transfer up to 10 Gb/s (GBT)
- 1 SFP+ serial link for Timing & Trigger (PON or GBT)
- Originally designed by CPPM for LHCb but will be used by ALICE as well
- https://indico.cern.ch/event/436451/contributions/1085380/attachments/1149137/1648703/PCIe40_status_report.pdf



Advantages of PCIe40

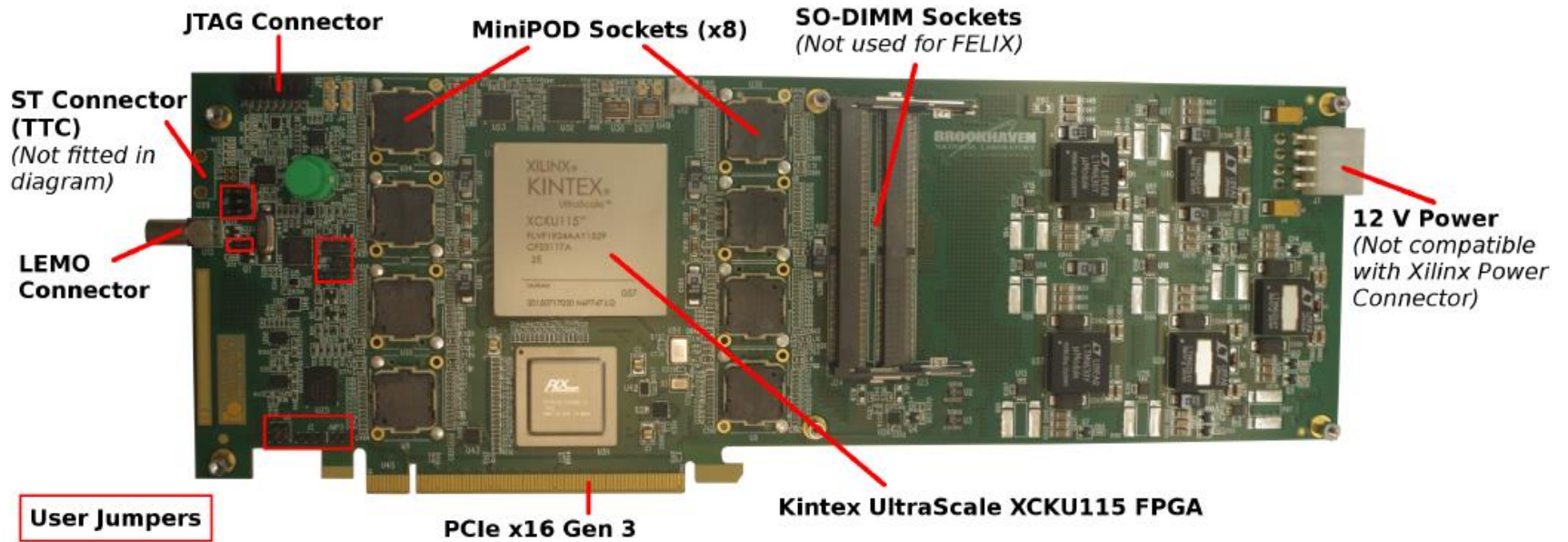
- ALICE development firmware for the PCIe40 available
- Firmware implements the custom protocol of the GBTx chips using the FPGA gigabit transceivers
- PCIe interface included (100 Gb/s)
- Remaining FPGA resources for data processing and formatting
- Software to configure and monitor SAMPA available

Negative – due to high demand within the collaboration, we won't be able to get one until **Sept. or Oct.**

Alternative to ALICE CRU

- ATLAS Readout Unit (BNL-711)
- **Contact** – Hucheng Chen, BNL, ATLAS (chc@bnl.gov)
- Part of their **FELIX** (**F**ront-**E**nd **L**ink **eX**change) system
- PCIe based – custom designed - identical in concept to ALICE CRU
- Firmware exists to implement GBTx custom protocol and PCIe interface
- Small quantity run upcoming – **MAY delivery (\$11,000)**
- We will order it
- Other options exist but are inferior to the **BNL-711**

BNL-711 V1.5



Timeline

- FEC
 - 1 week – get manufacturing files and specifications from ORNL (Gerbers, fab specs, PCB test procedure; bill-of-materials, pick & place file, inspection requirements)
 - 2 weeks – get quotes
 - 6 weeks – fabricate PCB, assemble + vendor inspection
 - 1 week – test FEC at ORNL
 - **Total = 10 weeks** (done by **May 1** if we start Feb 19 v)
- CRU (BNL-711)
 - Estimate **May 15** delivery
 - Acquire and integrate all available firmware and software from ALICE & ATLAS; develop new firmware and software; hooks to CODA

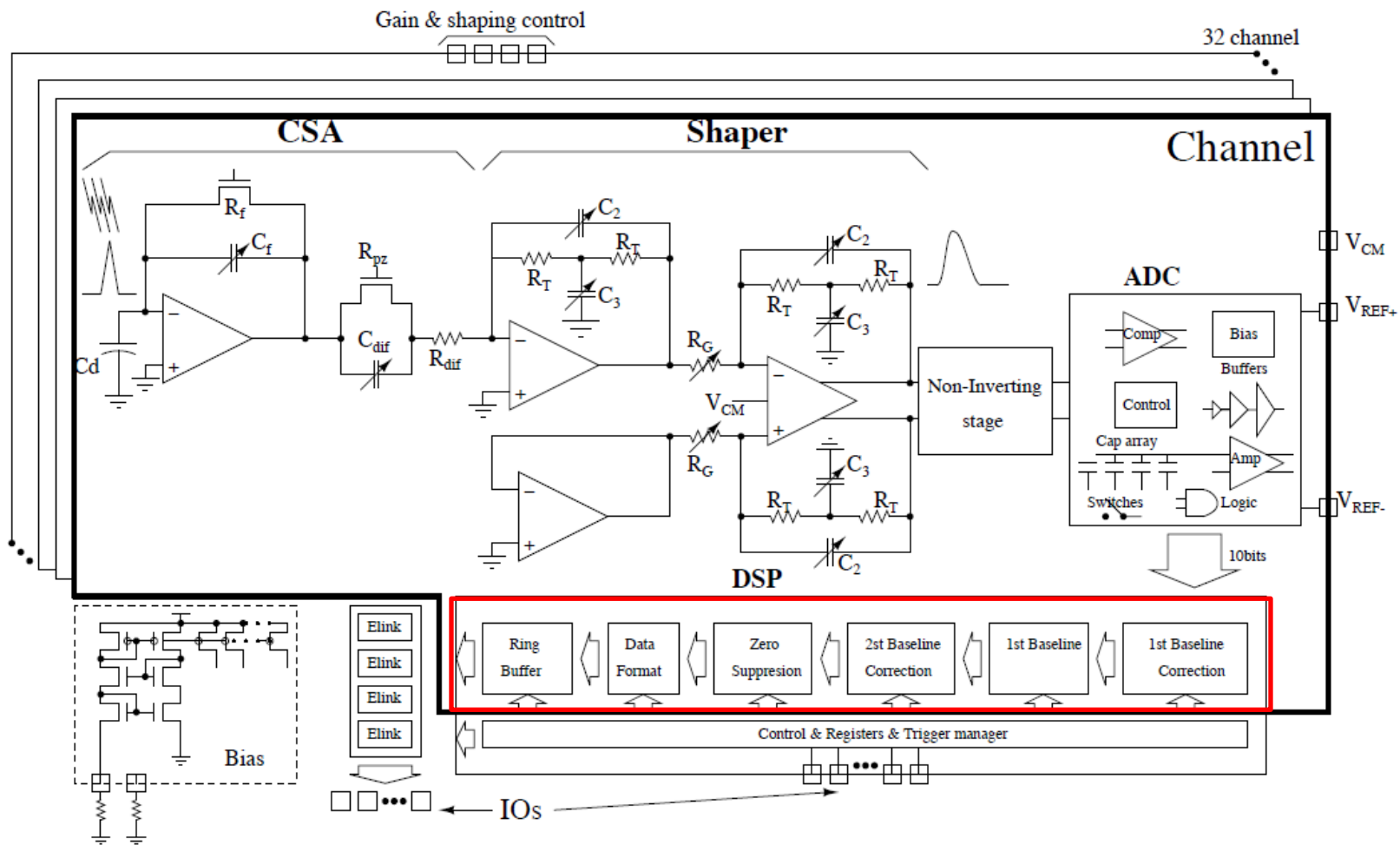
- Other

- PC and high-performance network card (40 Gb/s)
- Power supply for FECs
- Fiber optic cables

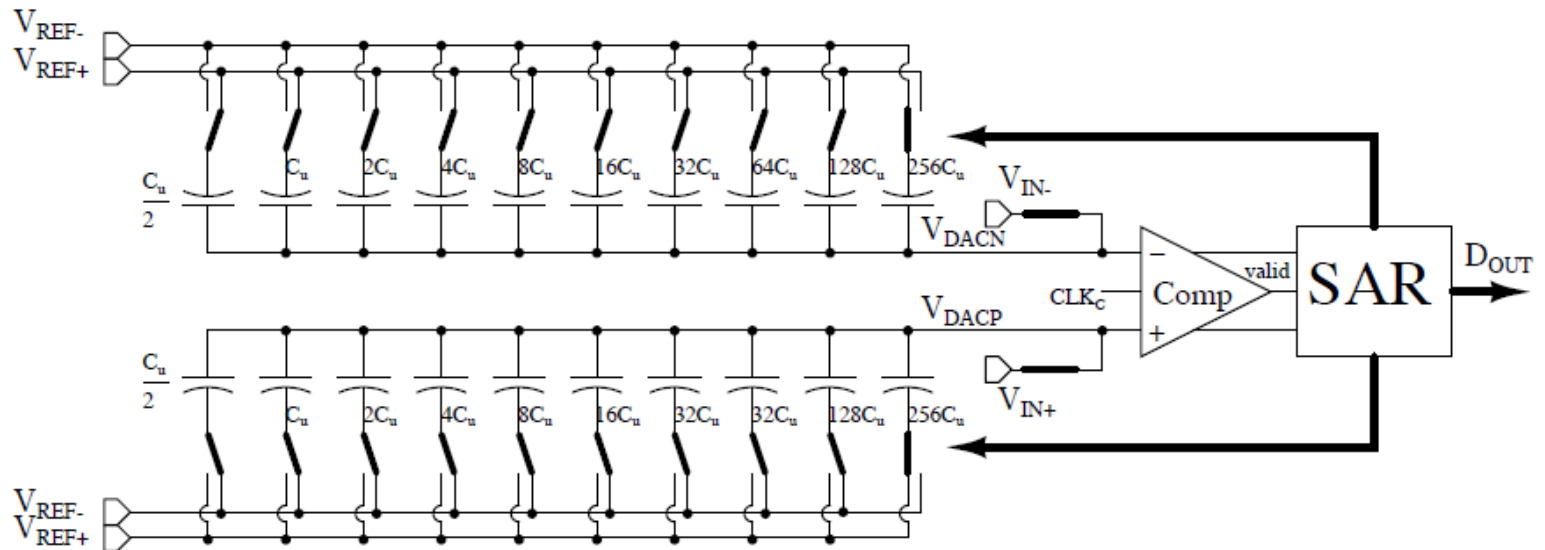
- **Target – June 1**

Extra Slides

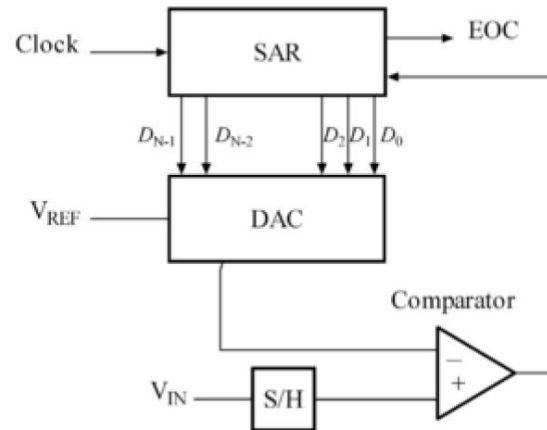
More Details



Switched Capacitor SAR ADC



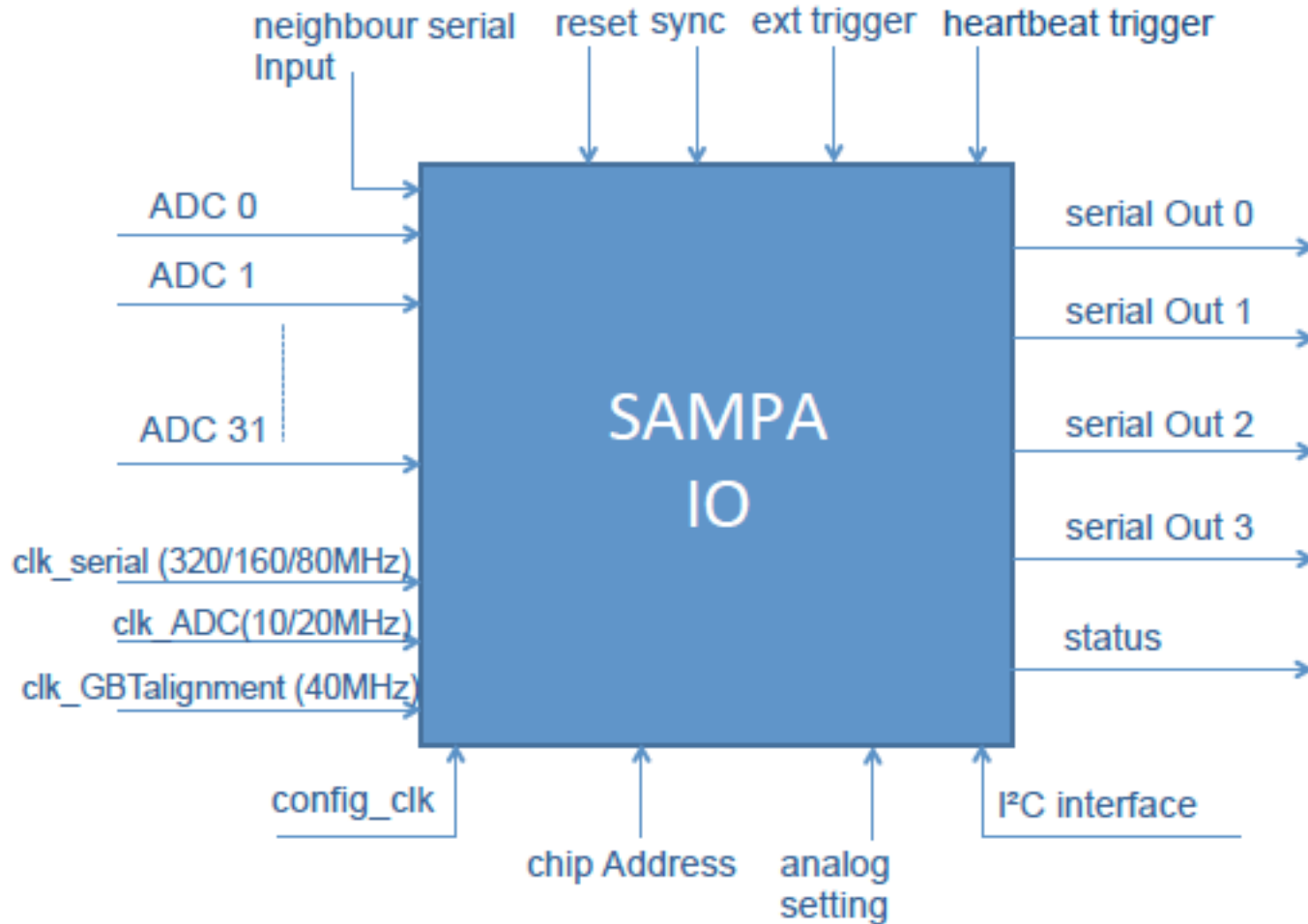
Successive Approximation ADC



Successive Approximation ADC Block Diagram

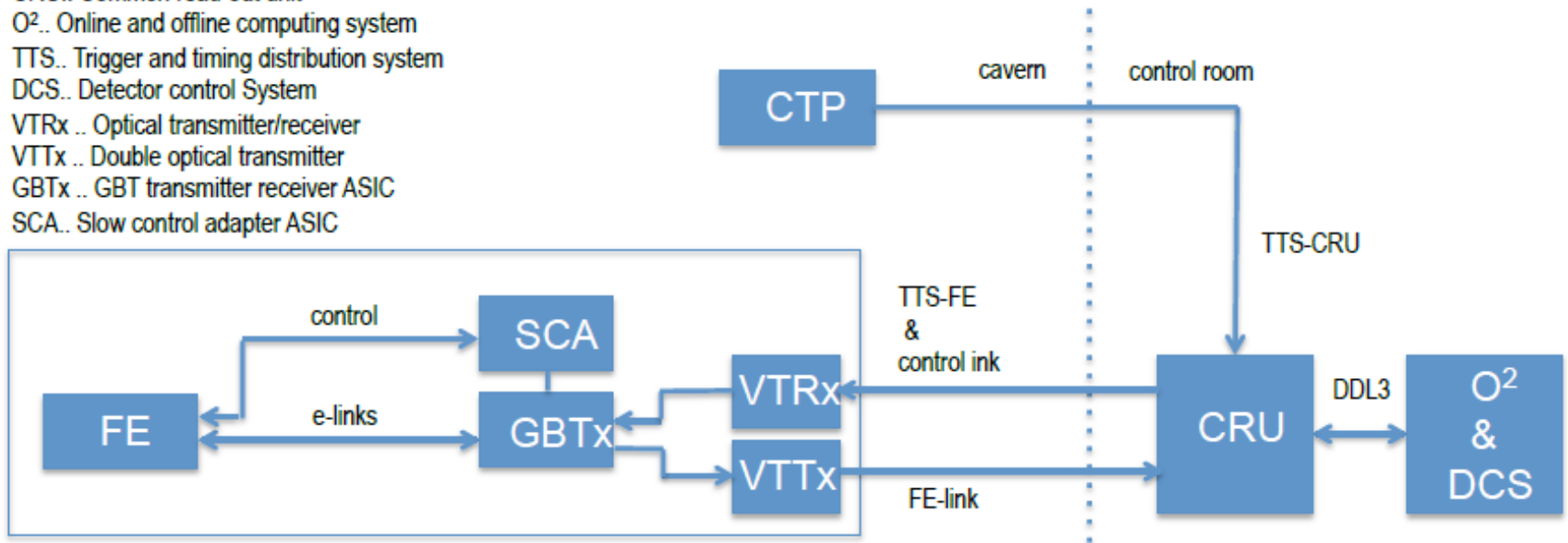
The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the SAR at the end of the conversion (EOC).

SAMPA I/O



Data and Control Flow

CTP.. Central trigger processor
CRU.. Common read-out unit
O².. Online and offline computing system
TTS.. Trigger and timing distribution system
DCS.. Detector control System
VTRx .. Optical transmitter/receiver
VTTx .. Double optical transmitter
GBTx .. GBT transmitter receiver ASIC
SCA.. Slow control adapter ASIC



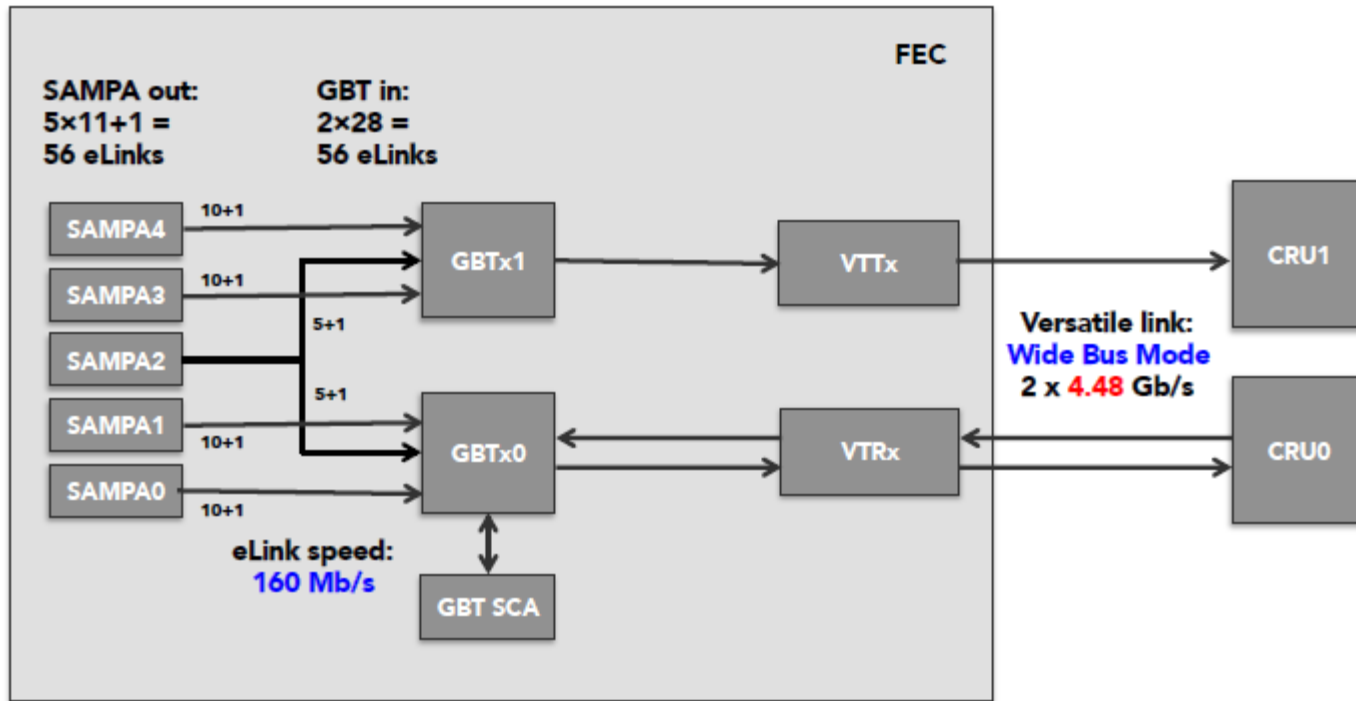


Fig. 7: Updated block diagram of the TPC FEC.

For the data multiplexing into optical links, the radiation-hard CERN GBT [8] and Versatile link components are used. This scheme has not changed with respect to the TPC Upgrade TDR. However, the SAMPAs are connected in a different way to the 2 GBTx ASICs located on each FEC. The GBT system is operated in the Wide Bus Mode where the total bandwidth for the uplink (from the detector to the CRU) is increased by 40% with respect to the standard GBT mode. In Wide Bus Mode the forward error correction is switched off. However, the radiation load at the TPC front-end electronics is comparatively, relatively low [9], such that no influence on the bit error rate is to be expected. In this mode, a total of 28 input eLinks at 160 Mbit/s are available per GBTx ASIC. The total available 56 input eLinks match nicely the 55 output eLinks from the 5 SAMPA ASICs. The data from SAMPA 2 is split such