The DAQ/Trigger Hardware Systems for
Jefferson Lab's 12GeV Experimental Programs

Chris Cuevas

Fast Electronics Group
Experimental Nuclear Physics Division

Outline

Focus of this talk will cover the front end readout electronics developed for use in all four experimental halls.

- **Front End Data Acquisition Hardware**
  - **Brief history**
  - **System Architecture**
  - **Circuit Board Catalog**
  - **Experiment examples**
- **Performance**
- **Future Looks *Faster***
- **Summary**

We've come a long way,

- **From first beam in 1994,**
  - **FastBus ADC and TDC used for experiment DAQ Front End**
  - **Custom Trigger applications used VXI and VME**
  - **Custom and commercial electronics for on-board detector electronics**

- **Moving to high speed serial backplanes**
  - **VME with Serial Extensions (VXS) – 2006**
  - **10Gbps links from each VME64x slot to VXS switch slots**
  - **Trigger information passed via crate backplane to Global Trigger**
  - **Detector signals stored in 8uS front end buffers**
    - **VME64x 2eSST readout - 200MB/s per crate when trigger received**
    - **Pipeline architecture with very low dead time**
  - **Extensive use of parallel fiber optic transceivers (4Tx/Rx) with 40Gbps aggregate capability**
    - **Transport front end crate Trigger information to Global Trigger**
    - **Trigger Interface uses fiber links for system SYNC, CLOCK, and Trigger Distribution**

12GeV CD3

Office of Nuclear Physics — *Exploring Nuclear Matter - Quarks to Stars*

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We've come a long way,

- **FPGA Technology has rapidly improved**
  - **Prototype Flash 250Msps used Xilinx Virtex 4 (2007)**
    - **PowerPC processor block**
    - **1Meg Block RAM**
    - **19K Logic cells – 320 I/O pins**
    - **16 high speed Gigabit serial transceivers on the chip**
    - **6.5Gbps maximum transceiver link speed**
  - **Virtex 7 has 80 serial transceivers on chip**
  - **13.1Gbps maximum transceiver link speed**
  - **42Meg Block RAM**
  - **550K Logic cells! – 600 I/O pins**
  - **Aggregate serial data I/O == 1Tbps**
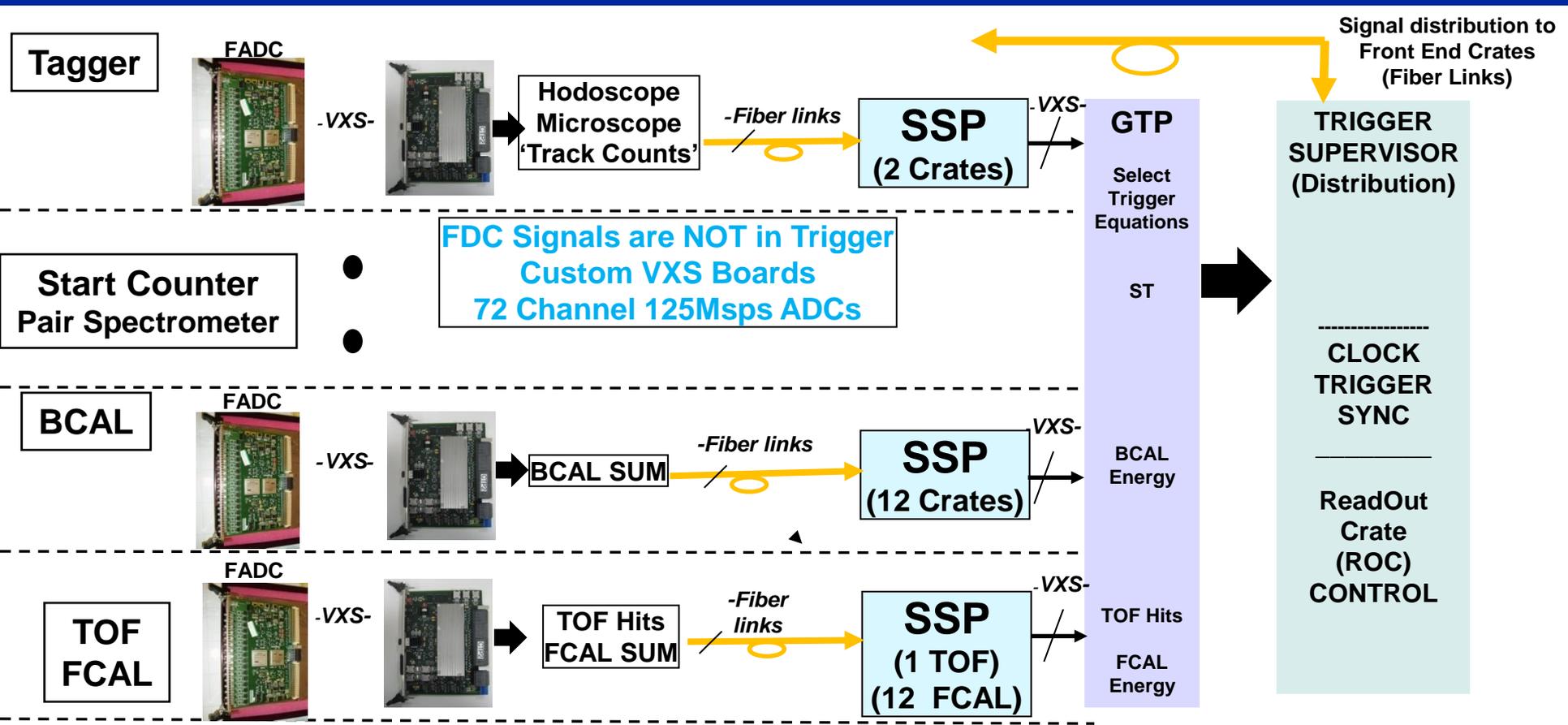
12GeV Trigger Design Requirements

- **200kHz average (Hall D) Level 1 Trigger Rate, Pipelined with up to 8µs front end digitizer memory**
  - **High Luminosity -> 10^8 photons/sec – Energy range $8.4 < E_\gamma < 9.0$ GeV**
  - **Initial data taking at low luminosity -> $\sim 10^7 \gamma/s$**

- **L1 trigger supports pipelined subsystem hit patterns and energy summing with low threshold suppression**

- **Scalable trigger distribution scheme (Up to 128 crates)**
  - **Hall D: 25 L1 Trigger crates, 52 total readout crates**
  - **Hall B: 38 L1 Trigger crates, 67 total readout crates**
  - **Hall A & C will each have ~1 L1 Trigger crates**
- **Low cost front-end & trigger electronics solution**
- **Strong FIRMWARE Features –**
  - **Hall B will use different programmable features than Hall D**
  - **Strong Partnership between Detector Groups and Firmware experts**
  - **Firmware "QA" control In Electronics/DAQ groups**
  - **Firmware can be remotely loaded to FPGAs from VME**

- **<u>ALL</u> Halls have benefited from new hardware design solutions**

System Architecture
Modern Method of Signal Capture
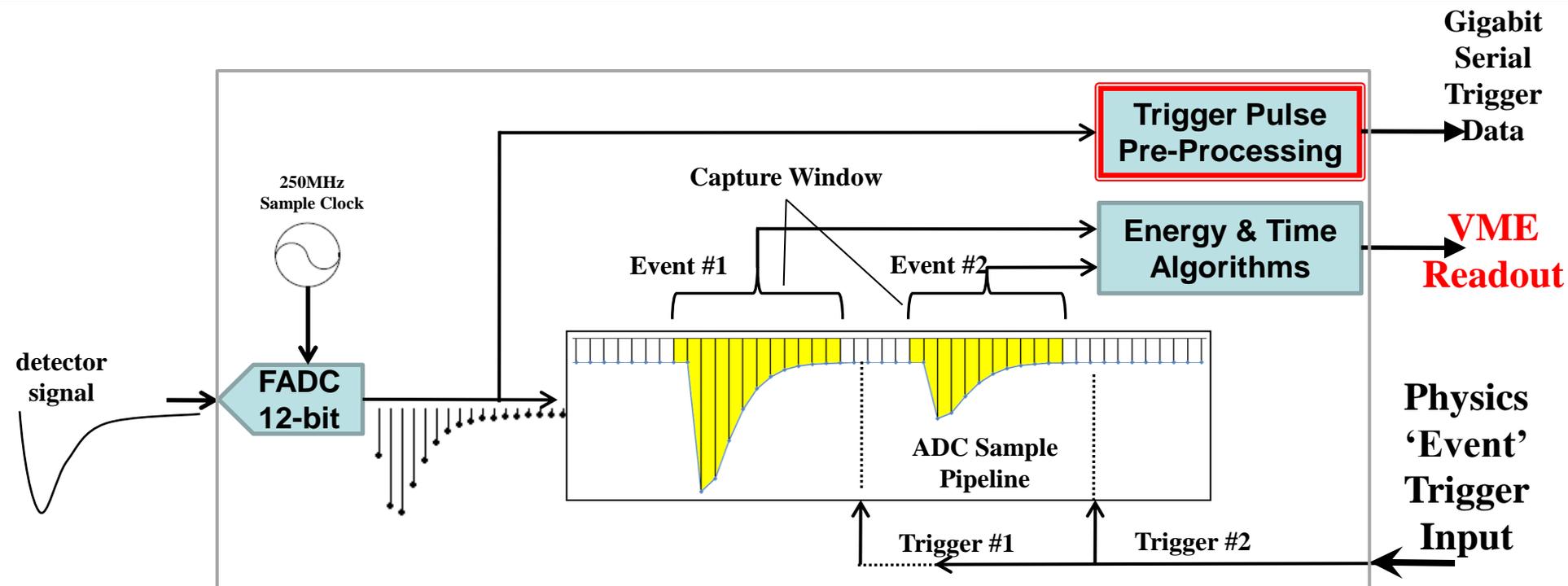
- **250MHz Flash ADC stores digitized signal in 8µs circular memory**

- **"Event" trigger extracts a window of the ADC data for <u>pulse sum</u> and <u>time algorithms</u>**

- **Trigger data contains detailed information useful for cluster finding, energy sum, etc.**

- **Hardware algorithms provide a huge data reduction by reporting only time & energy estimates for readout instead of raw samples**

Board → **Crate** → **Sub-System Processing** → **Global**

Tagger

FADC

-*VXS*-

Hodoscope Microscope 'Track Counts'

-*Fiber links*

SSP (2 Crates)

-*VXS*-

GTP

Select Trigger Equations

ST

BCAL Energy

TOF Hits

FCAL Energy

Signal distribution to Front End Crates (Fiber Links)

TRIGGER SUPERVISOR (Distribution)

CLOCK TRIGGER SYNC
_____

ReadOut Crate (ROC) CONTROL

Start Counter Pair Spectrometer

●
●

FDC Signals are NOT in Trigger Custom VXS Boards 72 Channel 125Msps ADCs

BCAL

FADC

-*VXS*-

BCAL SUM

-*Fiber links*

SSP (12 Crates)

VXS-

TOF FCAL

FADC

-*VXS*-

TOF Hits FCAL SUM

-*Fiber links*

SSP (1 TOF) (12 FCAL)

-*VXS*-

Block Diagram Example: Hall D Level 1 Trigger

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Production Board Quantities

Board ID	Hall D	Hall B	Halls A & C
FADC250	350	310	66
Trigger **I**nterface	64	82	12
Signal **D**istribution	60	53	2
Crate **T**rigger **P**rocessor(2009)	30	-	2
Sub-**S**ystem **P**rocessor	13	22	2
VXS **T**rigger **P**rocessor(2017)	1	30	-
Global **T**rigger **P**rocessor	2	2	2
Trigger **D**istribution	8	8	2
Trigger **S**upervisor	2	2	2

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More VXS Front End Boards

Board ID	Hall D	Hall B	Halls A & C
F1 TDC **2 Models** **32/48 Channel**	<u>110</u> Not in Trigger 48 CH – 115ps 32 CH – 57ps	-	-
FADC 125Msps 72 Channels 12 Bit	<u>201</u> Not in Trigger Mates with ASIC	-	-
VSCM **V**XS **S**ilicon **C**ontrol **M**odule	-	<u>41</u> Used for SVT FSSR ASIC	-
DCRB **D**rift **C**hamber **R**eadout **B**oard	-	<u>264</u> 96 CH 1ns TDC	-

A Glimpse of Future DAQ
Readout/Control of Front End ASIC

**RICH Group
Fast Electronics
DSG
Hall B**

- ## RICH (CLAS12) and DIRC (GlueX) examples
  - **ALL FPGA boards have been tested(Completed in May 2016)**
  - **Production ASIC board(s) [2-MAROC and 3-MAROC] completed**
  - **Detector will be installed in Hall B during 2018-January access**

32 LC Fiber Links

**391 -- H12700 Hamamatsu
64-anode PMT
Total anodes: 25,024**
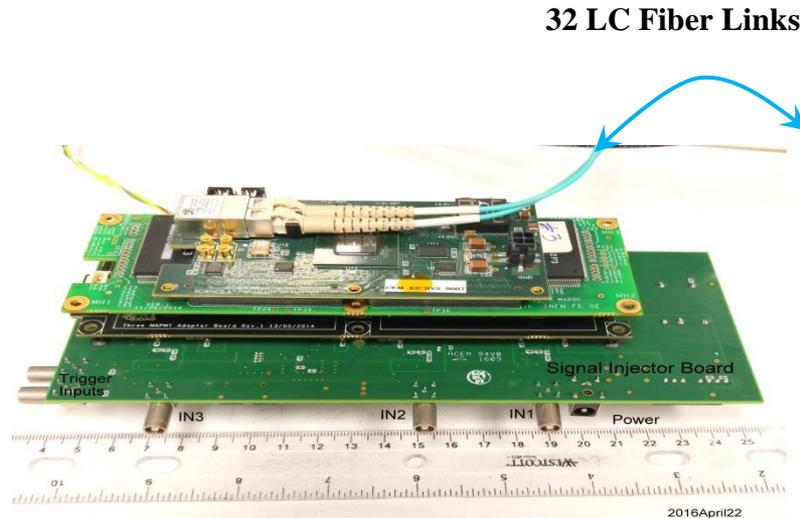
**On Board 192 channel FPGA Readout Board
MAROC3 ASIC mates to maPMT
Artix 7 FPGA drives LC fiber optic transceiver**

**VXS Sub-System Processor
32 - 2.5Gbps links to RICH
FPGA Readout Boards**

**More ASIC examples:
CLAS12 SVT
FSSR2 > 33K strips
CLAS12 MVT
DREAM > 20K strips**

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JLab – VTP (VXS Trigger Processor)

- CTP, developed for **GLUEX** evolved into VTP for **CLAS12**.

- Has the ability to read data from payload modules at faster than VME speeds using VXS serial lanes.

- FPGA supports trigger algorithms, zero suppression etc.

Front panel parallel fiber links to/from other VTP or SSP.

(4 Tx/4Rx 6.25Gb/s/fiber)

Readout data path. (40 Gb/s Fiber Ethernet as 4 x 10 Gb/s).

Control (10/100Mb Ethernet)

Console [RS232]
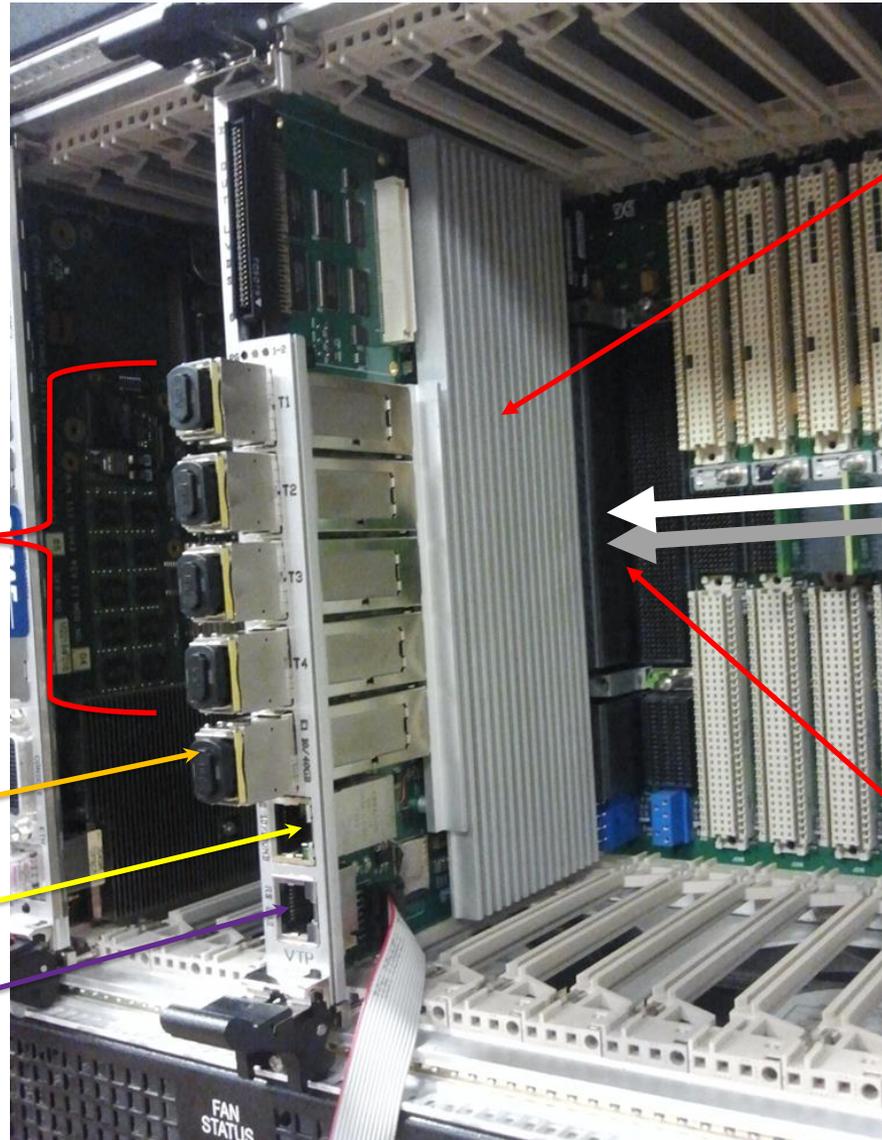
Virtex 7 FPGA
Logic and Algorithm Engine. Data transfer, pattern recognition, zero suppression etc.

Zynq SoC Processor running Linux OS & Coda 'ROC'

VXS Data path 10Gb/s from each 'payload' slot

VXS Trigger Path 10Gb/s from each 'payload' slot

VXS Switch slot 4 serial lanes from each 'payload' slot

Drift Chamber Segment Finding Trigger

B. Raydo

**Region 3 Wire Chamber
1344 Anode wires**

x14 DCRB

**70Gbps
(DC Hits)**

VTP:
- **VXS Trigger Processor**

- **Receives all DC hits from DCRB**

- **Searches for track segments and reports position/angle to next trigger stage**

- **Scope like interface on VTP allows real-time display of found segments by trigger logic**
  - **Cosmic event shown where only 1 segment was the trigger condition**
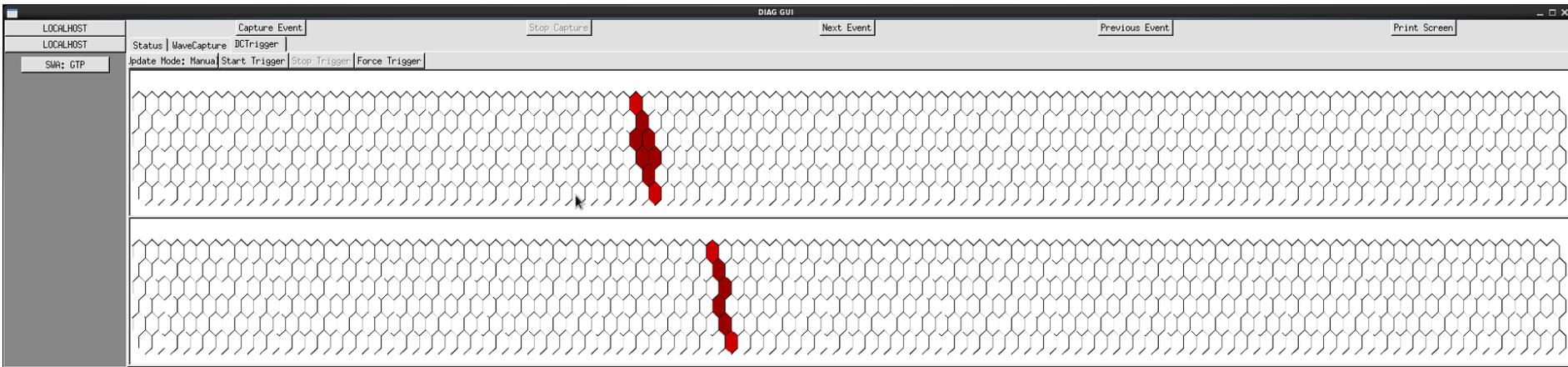
VTP – Pipeline Readout

- **ADC data used by the trigger is read by the VTP and passed to trigger crates to take part in the global trigger (blue lines).**

- **The full data to be read out is buffered in the ADCs.**

- **Once the trigger decision is made the global trigger is distributed back to the VTPs (brown lines).**

- **The data read by the VTP, zero suppressed and formatted then passed via a network switch to the event builder running on a Linux server (red line).**

- **Readout in this mode has the advantages of :**

  - **Zero or very low deadline.**

  - **High speed since the VME bus and CPU (green) are no longer in the data path.**

  - **Flexibility, since the system is built from standardized components that differ only in firmware and programming.**
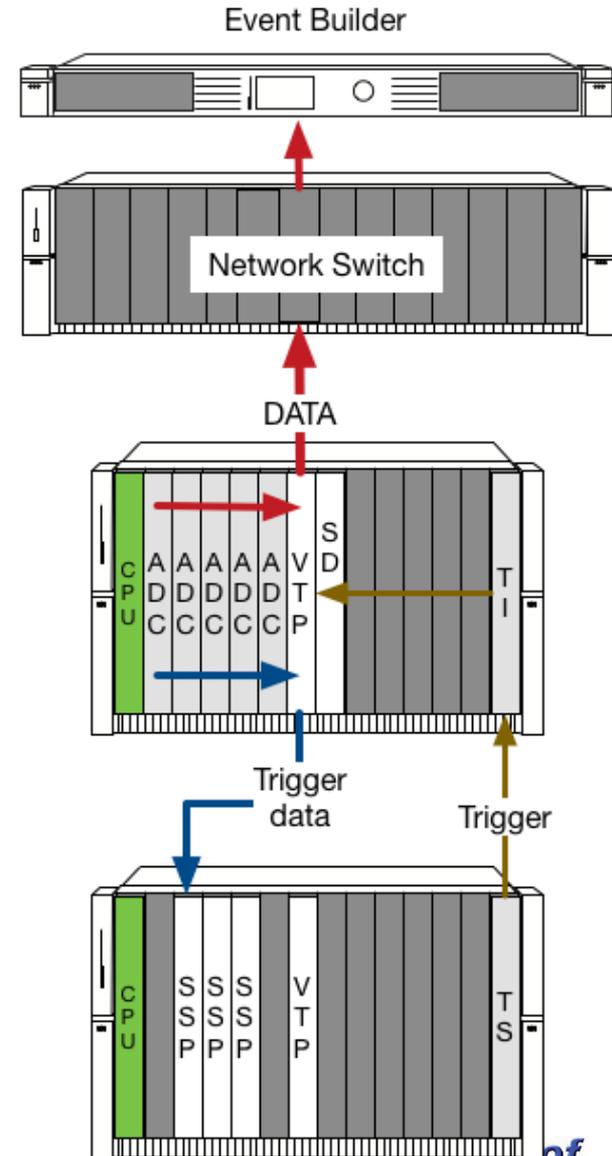
Summary

➤ **Delightful journey for the design of the new Front End Readout Electronics Pipeline electronics for all experiments is a dream come true.**

➤ **Successful DAQ operations with beam in Halls D, B, C and A**

  • **High intensity running in Hall D successful**

  • **Max trigger rate is below original design specification**

➤ **VXS decision a decade ago was a very good choice and offers a strong future for new applications.**

➤ **Keeping up with FPGA Technology with Virtex 7 on VTP boards used in Hall B Trigger is essential for future upgrades.**

➤ **Enormous Drift Chamber electronic system complete!**

➤ **FPGA control/readout boards ready for RICH detector assembly**

  - **SSPs ordered and new firmware for data transport protocol in progress**

  - **Will use same readout scheme for GlueX DIRC**

➤ **Many electronic topics not covered, and we maintain all legacy equipment too** ☺

➤ **Link to DAQ/Trigger Manuals:**

 https://coda.jlab.org/drupal/content/front-end-hardware

• **Questions?**

Backup slides
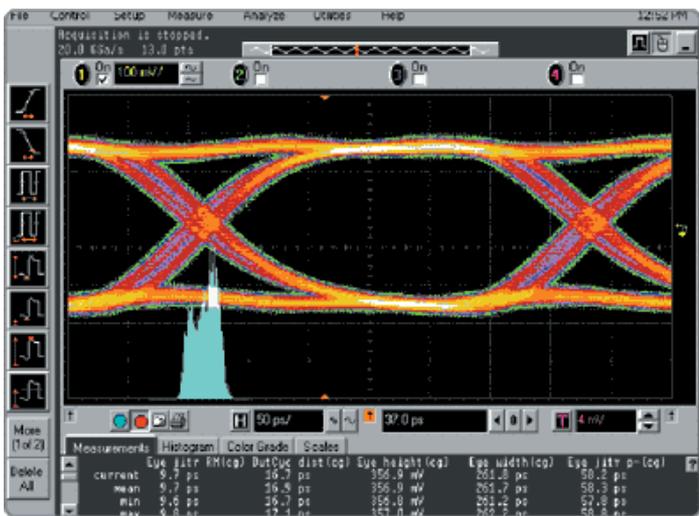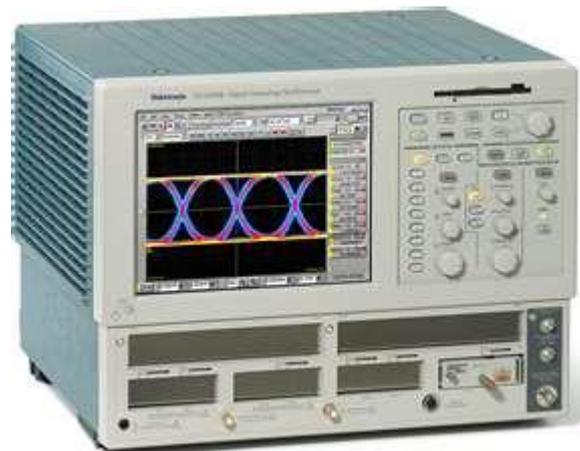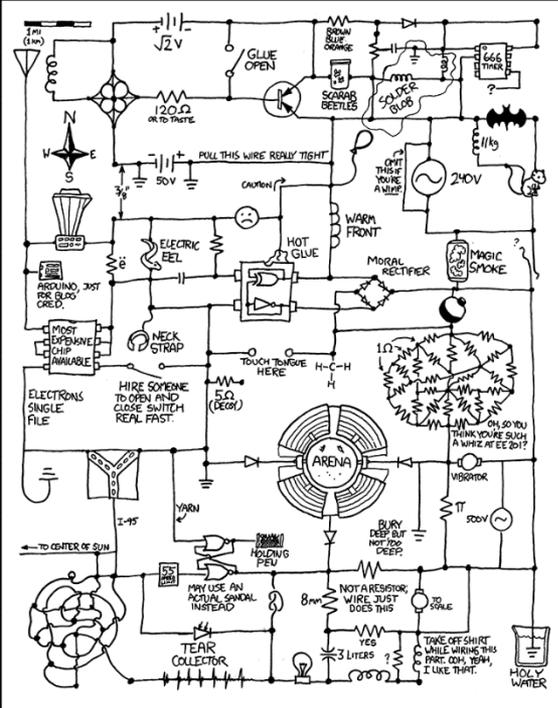
Crate Trigger Processor

- **4 Fully assembled are tested and in the lab!!**

- **2 newest units include VirtexV FX70T that supports higher serial speeds. (5Gbps) Matches FX70T on FADC250**

- **Crate Trigger Processor computes a crate-level energy sum (or hit pattern)**

- **Computed crate-level value sent via 8Gbps fiber optics to Global Trigger Crate (32bits every 4ns)**

CTP
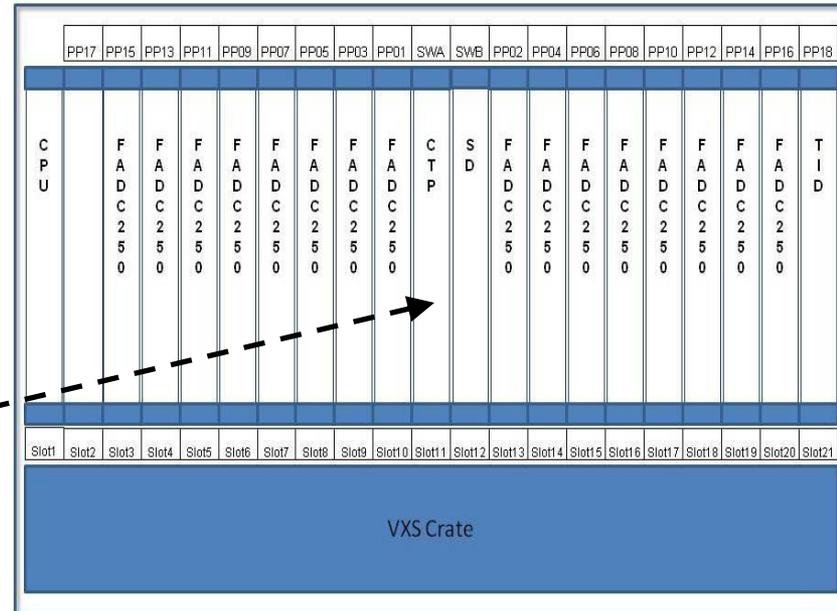
MTP Parallel Optics

8Gb/s to SSP

VXS Connectors Collect serial data from 16 FADC-250

- **Significant verification testing has been completed with 2 crate DAq configuration.**

- **Gigabit serial transmission fully tested**

- **2 CTP used in HPS beam test with new cluster finding trigger application**

Start Time
05/03/17 15:44:12

End Time
0

Run Parameters

Expid
hdops

Session
hdops

Configuration
hd_all.tsg_2ER_NoPs12Tf1B12_2dcfdcNF3

Output File
undefined [ERraid1]

User RTV %(config)
/home/hdops/CDAQ/daq_dev_v0.31/daq/config/hd_all/TRG_CDC_BUSY.conf

User RTV %(dir)
unset

Run Status

Run Number
31400

Run State
active

Event Limit
0

Watch Component
ER_class

Data Limit
0

Total Events
40,826,725

Time Limit (min.)
0

Name	State	EvtRate	DataRate	IntEvtRate	IntDataRate
ER_class	na	113520.0	2715270.7	109092.3	2605644.7
ERraid1	active	56640.0	1354456.6	54547.8	1302996.9
ERraid0	active	56800.0	1358841.1	54554.0	1303220.4
SEB_class	na	113920.0	2724955.9	109175.7	2599598.8
SEB0	active	56480.0	1351201.0	54574.7	1303639.4
SEB1	active	56920.0	1361160.2	54614.7	1296557.4
DCFDC	active	113383.3	245440.8	109284.4	235437.8
DCFDC2	active	113440.0	327618.3	109098.4	314159.0
DCFDC3	active	113223.4	282761.1	109326.2	272418.1
DCBCAL	active	113440.0	607844.9	109112.0	583362.4
DCCDCSTPS	active	113420.0	491736.0	109255.4	469159.4
DCFCAL	active	113480.0	763489.9	109165.5	732290.0
ROCFCAL12	active	2844.5	63245.8	2731.7	60332.9
ROCFCAL11	active	2846.0	65755.1	2732.7	63054.2
ROCFCAL10	active	2949.5	68774.9	2732.9	63490.1
ROCSTPSC2	active	0.0	0.0	0.0	0.0
ROCSTPSC1	active	2844.5	31455.5	2727.2	30031.2

Event Rate Data Rate Client Data Live Time LDRs InB OutB

Data Rates — 28 VXS Readout Crates
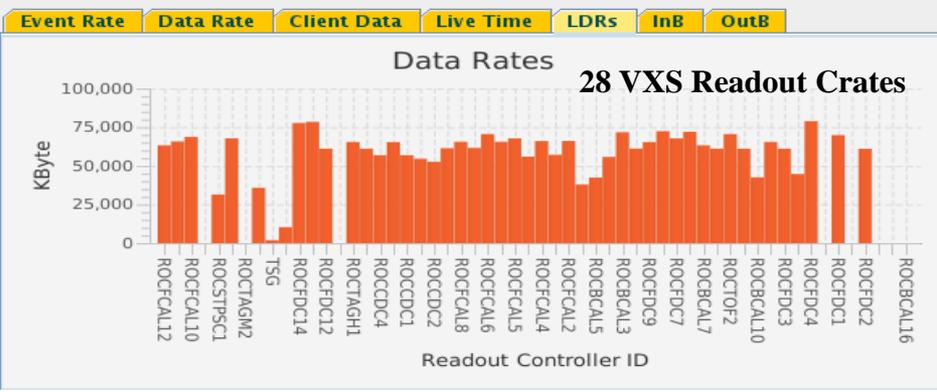
Live Time

- **>100kHz event rate performance**
- **2.7GB/s total data rate**
- **93% avg. live time**

- **Hall D High Intensity Review**
- **2017 May 11**

Slide from D. Lawrence

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Flash ADC 250MHz

Fast Electronics
DAQ Groups
23-Sept-2011
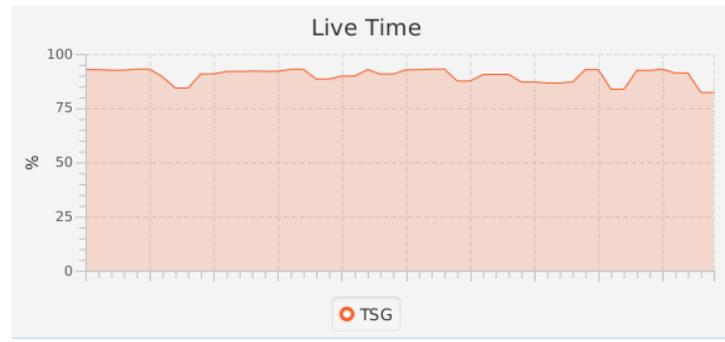
- **16 Channel, 12-bit**
  - **4ns continuous sampling**
  - **Input Ranges: 0.5V, 1.0V, 2.0V (user selectable via jumpers)**
  - **Bipolar input, Full Offset Adj.**
  - **Intrinsic resolution – σ = 1.15 LSB.**
  - **2eSST VME64x readout**
  - **Several modes for readout data format**
    - **Raw data**
    - **Pulse sum mode (Charge)**
    - **TDC algorithm for timing on LE**
  - **Multi-Gigabit serial data transport of trigger information through VXS fabric**
  - **On board trigger features**
    - **Channel summing**
    - **Channel coincidence**
    - **Hit counters**
  - **Automatic Test Station is complete**
  - **Production Boards**
    - **Deliveries on schedule**

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Fast Electronics Group

Roll the credits first,,,

Physics Division Support Group for over two decades

- **5 Engineers (Electrical/Electronics)**
  - **Chris Cuevas**
  - **Fernando Barbosa**
  - **Hai Dong**
  - **Ben Raydo**
  - **Cody Dickover**
- **6 Technical Staff**
  - **William (Bill) Gunning**
  - **Nick Sandoval**
  - **Chris Stanislav**
  - **Armen Stepanyan**
  - **Mark Taylor**
  - **Jeff Wilson**

Radiation Detectors and Imaging DAq

H. Dong
J. Wilson
A. Stepanyan

ETS V3

EFADC16

- **E**thernet **FADC**-250 boards still in use for several plant biology research applications.

- Plant Biology research

    - CRADA with PI Dr. Zisis Papandreou @U of Regina
    - Sylvia Fedoruk Canadian Centre for Nuclear Innovation
    - In June 2017 first experiments at the Saskatchewan Center for Cyclotron Science in Saskatoon.

    - Using latest Ethernet FADC – Version 3
        - Version 4 design will use Artix series for lower cost and higher performance.
    - Ethernet Trigger Supervisor (ETS) V4 in process of upgrade
        - Schematics complete
        - Board layout in progress
        - At least a month before fabrication and assembly

C. Dickover
B. Raydo

2.5Gbps line rate 16bit bus @ 125MHz for transmit and receive
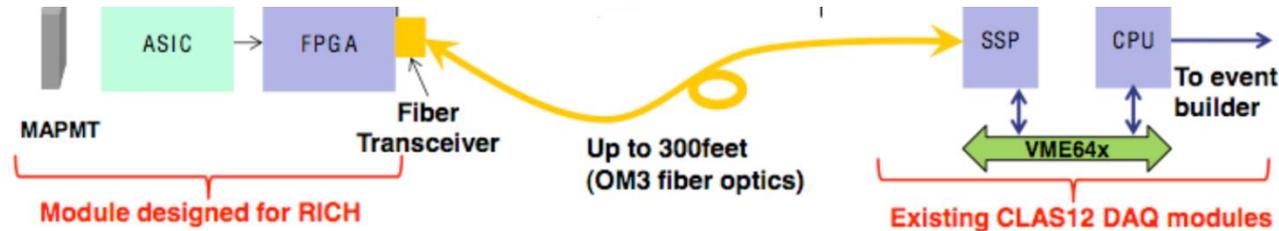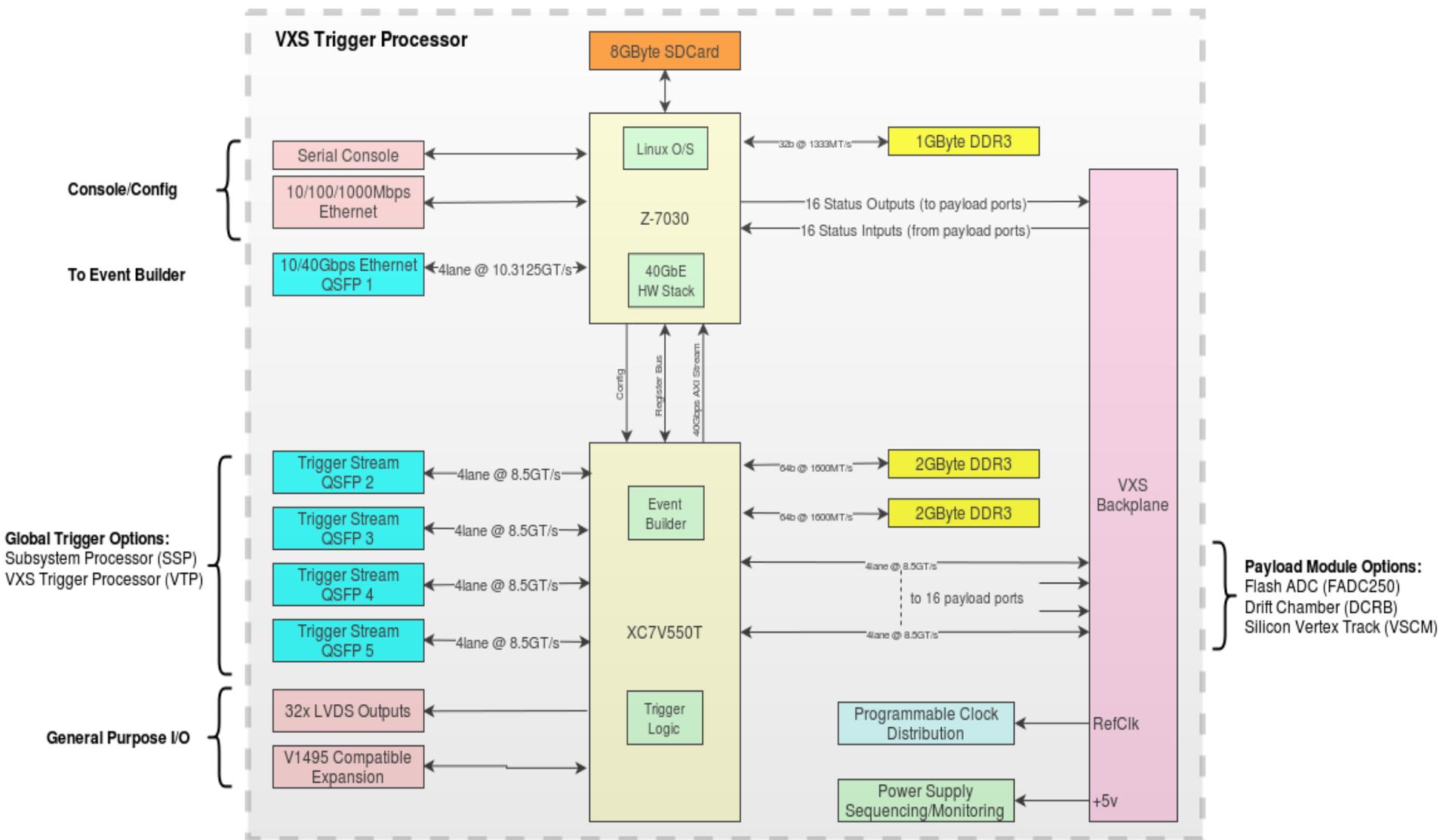

FPGA to SSP Data transfer firmware
Cody will develop and test firmware
Ben has provided project requirements and guidance

- **Firmware development is progressing nicely**
- **Test with single FPGA board will happen soon.**
- **Escalate testing to full 8 ports on the SSP will require significant testing and iterations.**
- **Existing top level blocks (VME, event builder, etc.) will be pushed together with new data transport protocol firmware.**
- **Plan for a few weeks of verification testing.**

- ❖ **Each SSP can manage 32 FPGA control/readout boards (LC Fiber)**
- ❖ **138 FPGA boards will connect directly to five (5) SSP boards**
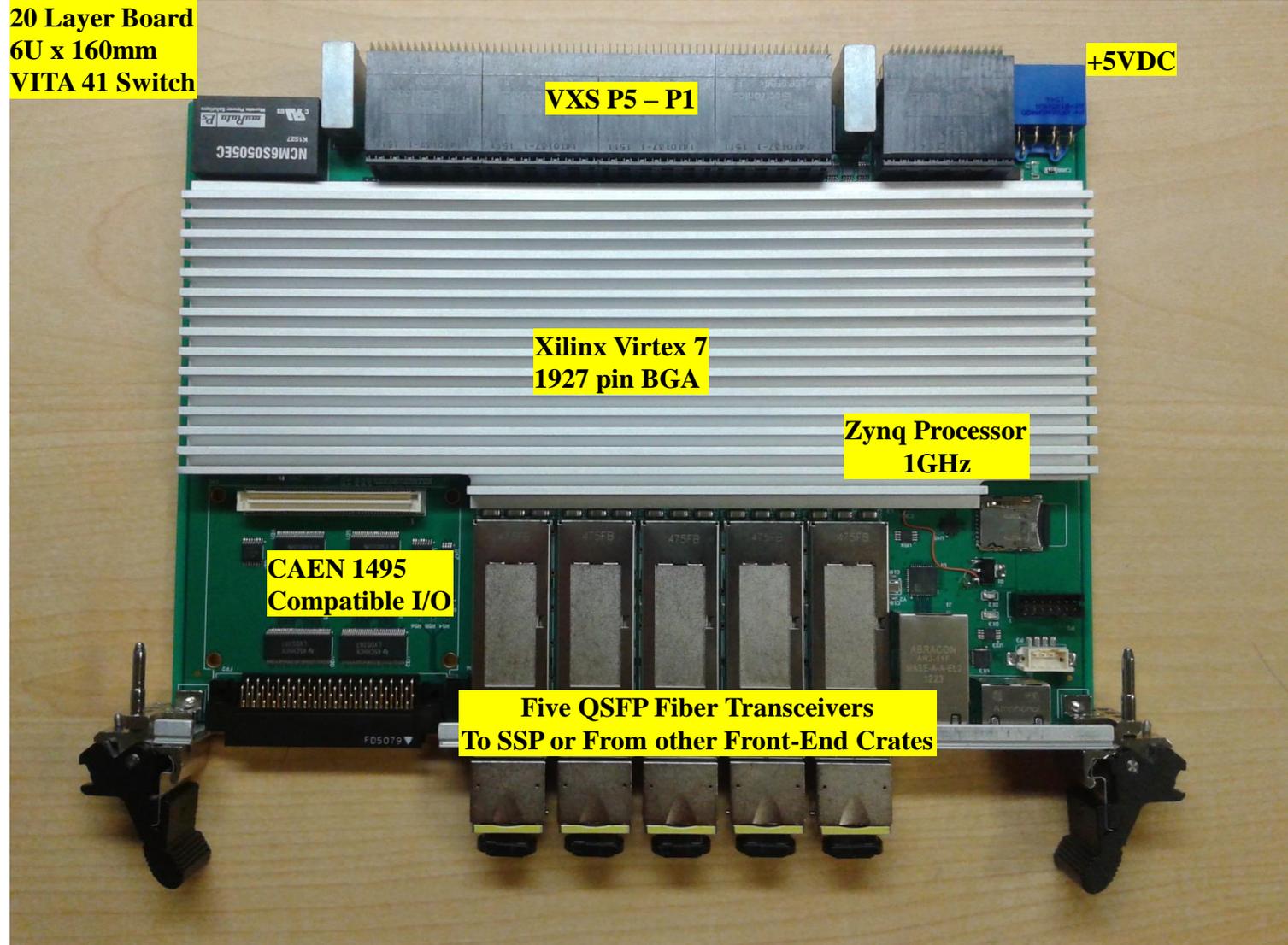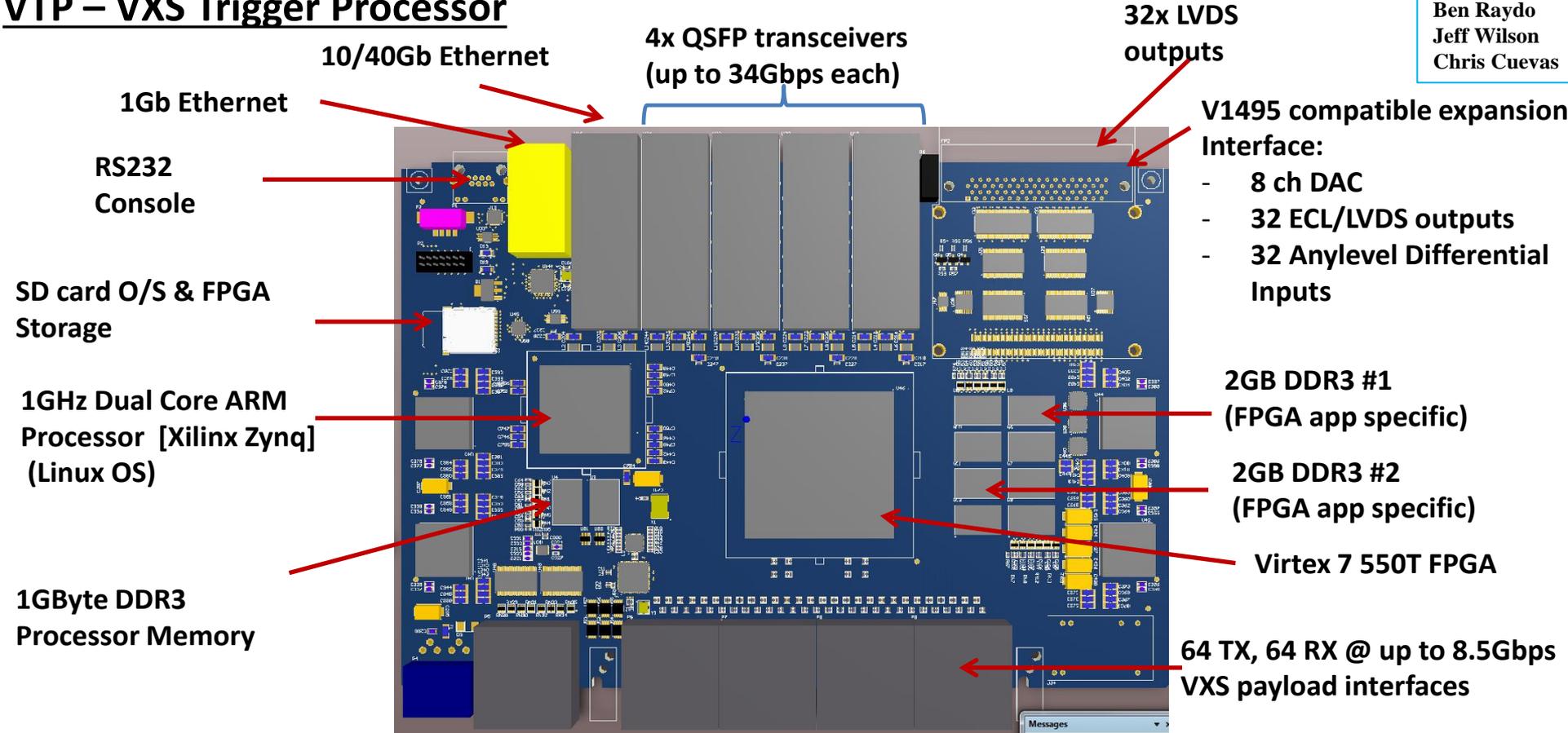- ❖ **Ten (10) new SSP boards have been ordered.**

Hall B – VTP
"The Art of Electronics Needs Cooling"

20 Layer Board
6U x 160mm
VITA 41 Switch

+5VDC

VXS P5 – P1

Xilinx Virtex 7
1927 pin BGA

Zynq Processor
1GHz

CAEN 1495
Compatible I/O

Five QSFP Fiber Transceivers
To SSP or From other Front-End Crates

VTP – VXS Trigger Processor

Ben Raydo
Jeff Wilson
Chris Cuevas

1Gb Ethernet

10/40Gb Ethernet

4x QSFP transceivers (up to 34Gbps each)

32x LVDS outputs

RS232 Console

V1495 compatible expansion Interface:
- 8 ch DAC
- 32 ECL/LVDS outputs
- 32 Anylevel Differential Inputs

SD card O/S & FPGA Storage

1GHz Dual Core ARM Processor [Xilinx Zynq] (Linux OS)

2GB DDR3 #1 (FPGA app specific)

2GB DDR3 #2 (FPGA app specific)

Virtex 7 550T FPGA

1GByte DDR3 Processor Memory

64 TX, 64 RX @ up to 8.5Gbps VXS payload interfaces
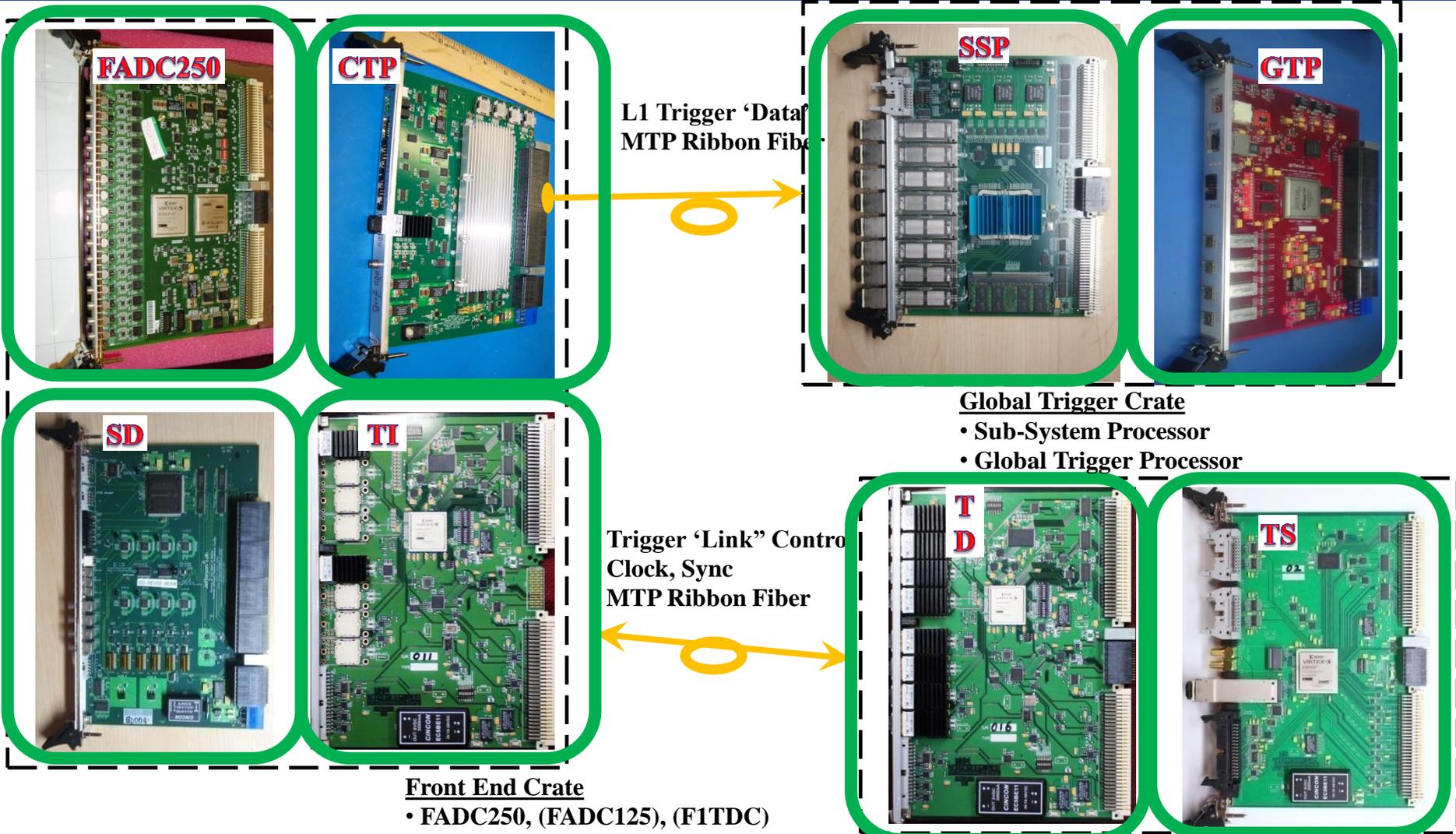
DDR3-1600 Trace/Package Deskewing:

DDR3-1600 byte eye before deskew:

**DDR3-1600 byte eye after deskew:**
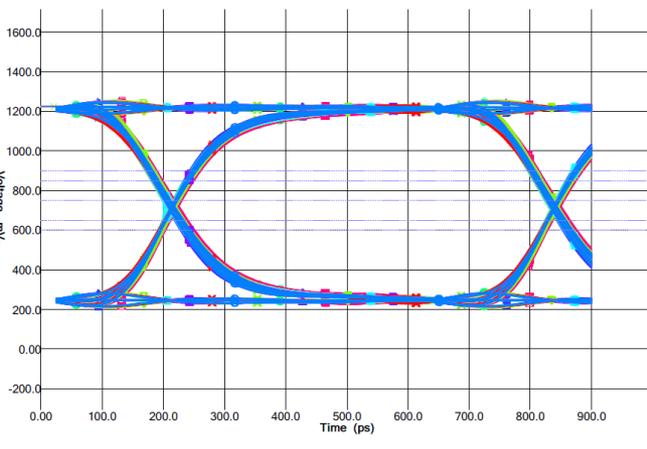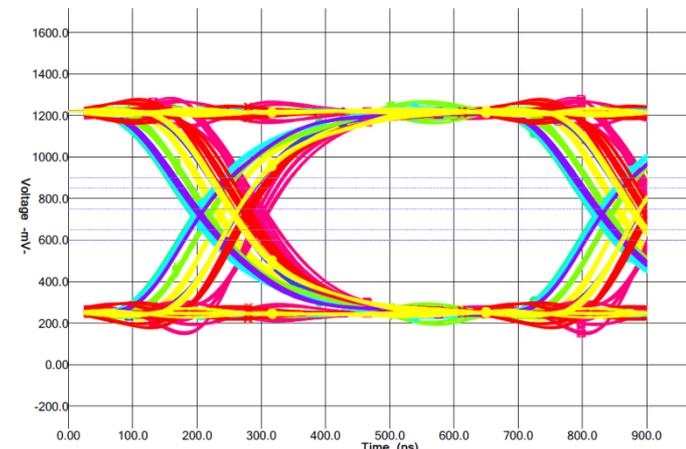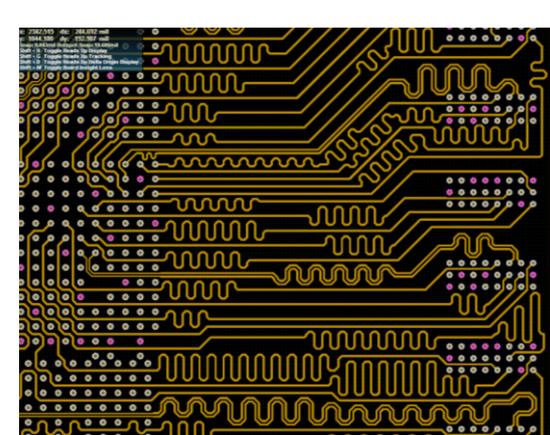
All Trigger Modules Delivered!

L1 Trigger 'Data'
MTP Ribbon Fiber

Trigger 'Link' Control
Clock, Sync
MTP Ribbon Fiber

Global Trigger Crate
- **Sub-System Processor**
- **Global Trigger Processor**

Front End Crate
- **FADC250, (FADC125), (F1TDC)**
- **Crate Trigger Processor**
- **Signal Distribution**
- **Trigger Interface**

Trigger Control/Synchronization
- **Trigger Supervisor**
- **Trigger Distribution**

Other Interesting Activities

- High speed serial output ADC – JESD204B
    - Non-Disclosure Agreement with Analog Devices for quad 500Msps ADC
    - Definitely the future of high speed ADC readout
    - Several manufacturers support this standard
    - Minimizes circuit board routing. FPGA transceiver count has increased including serial transmission speed and reliability
    - "No-Bus" designs will eliminate large expensive backplanes
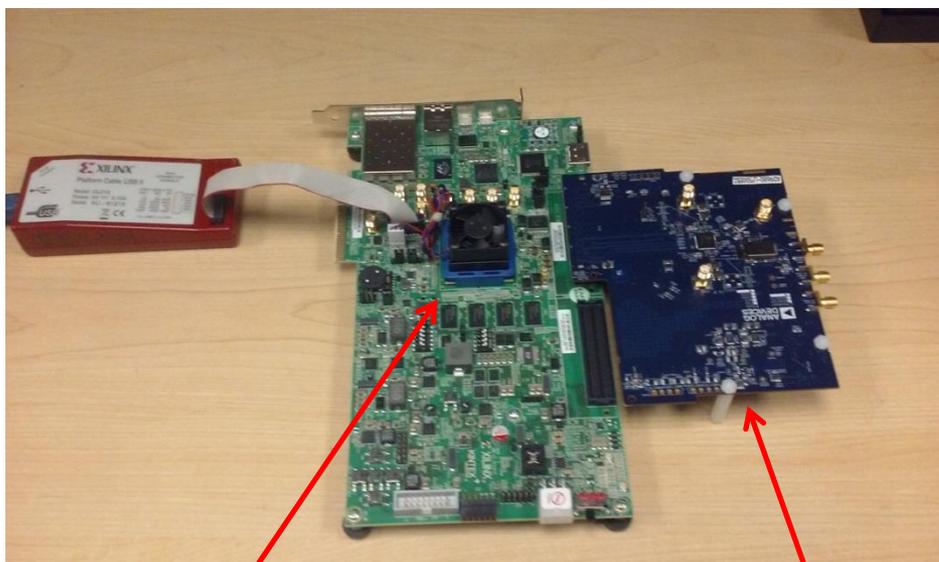
**Xilinx Kintex FPGA evaluation board
Analog Devices 2 channel 500Msps serial ADC**

What is the JEDEC Standard 204 (JESD204B)

- JESD204B (August 2011) – 2nd revision utilizes a device clock and adds measures to ensure deterministic latency
    - Supports *multiple* aligned serial lanes for *multiple* converters at speeds up to *12.5 Gbps*

ANALOG DEVICES

Drift Chamber Readout Board
96 channel TDC [1ns]
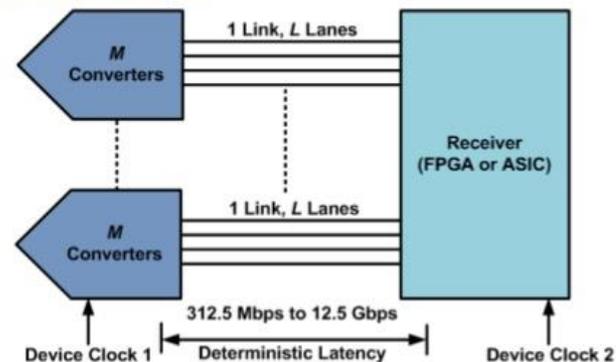
6U x 160mm
VXS payload format

- **14 first article boards delivered in February**
- **Excellent quality and no issues with assembly**

- **Acceptance test setup developed and will be Used for future debug and repair.**

- **Region 1 chamber is running with new DCRB's in EEL-125**
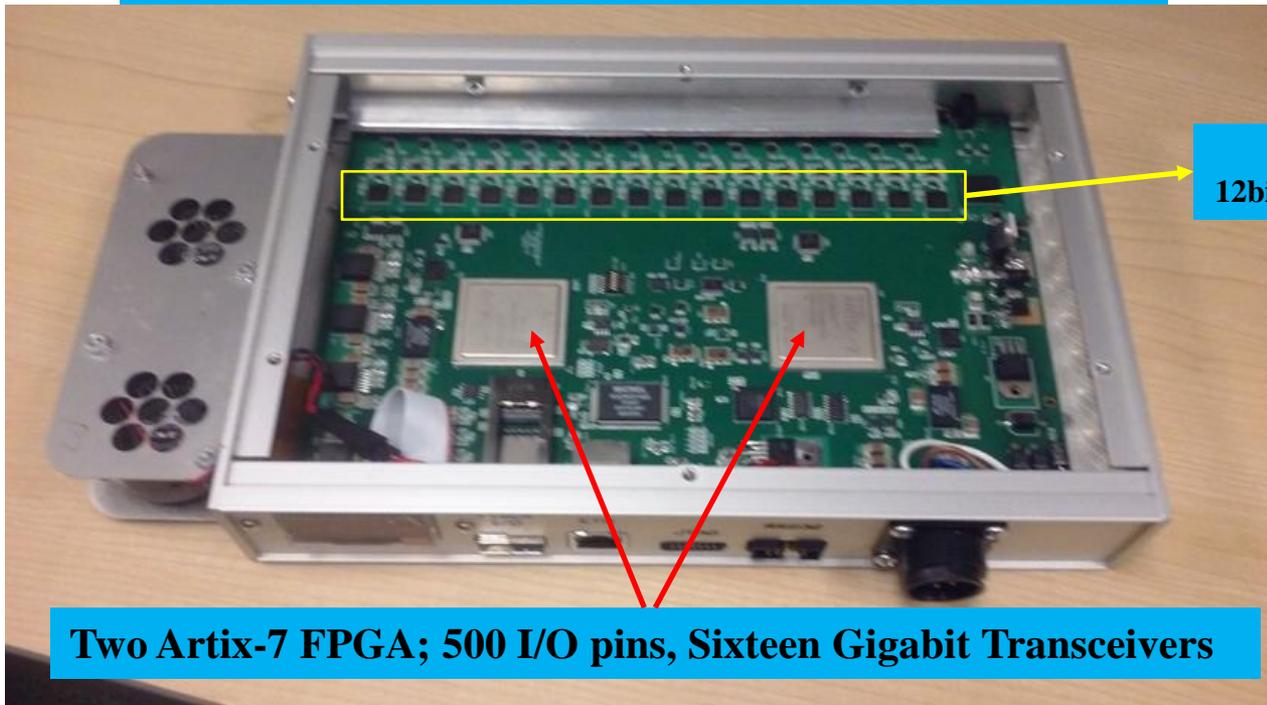
- **All 266 DCRB have been received and pass Acceptance testing. [August 2015] 252 DCRB required for CLAS12 Drift Chamber System.**

- **20 VXS (6U) crates received in October 2015 and pass acceptance testing. These units are installed in Hall B**

Other Interesting Activities

- Ethernet Stand-Alone Digitizers
  - ✓ Version 3 of the E-FADC250 is ~$2K less than original
  - ✓ Faster, less power than original version because of newer Xilinx Artix-7 parts
  - ✓ Parallel fiber optic output option for combining with additional units

1Gb-Ethernet Flash ADC; Version 3 – 250Msps; 12-bit

16 Each
12bit Parallel output ADC

Two Artix-7 FPGA; 500 I/O pins, Sixteen Gigabit Transceivers

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