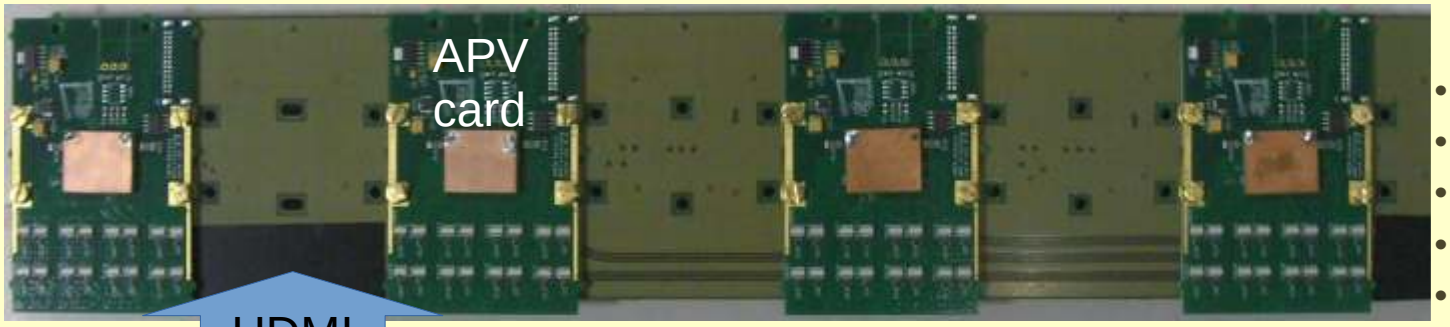
uRwell APV25 Readout
(electronics developed and used for the SBS GEM trackers)

E. Cisbani, P. Musico, …

JLab Integration: Cris Cuevas, Benjamin Raydo,
Alexandre Camsonne, ...

APV-MPD Electronics for SBS



Backplane (bus distribution)

- rigid or flexible
- up to 5 APV cards
- one digital HDMI cable
- one analog HDMI cable
- 3.5 V / 0.7 A power supply line

HDMI



MPD Main Block

Arriga GX FPGA
128 MB DDR2-RAM
Firmware V4.0 (74% resources):

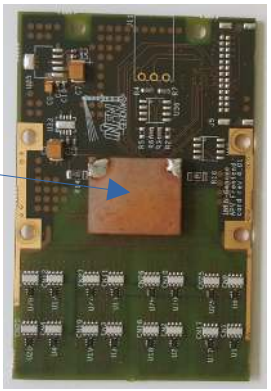
FIR Filter (16 pars)
Zero Suppression
Common mode and pedestal subtraction
 # 12 bit ADC
 # ≈2 ns trigger time resolution
 # up to 16 APV cards

MPD optical Interface → SSP/Aurora Protocol → **Optical Fiber** → SSP/VTP

MPD-VME Interface → VME-Protocols → 2eSST, 2eVME, VME32 …, VXS → **VME (64x)** → VME Master (Intel SBC)

Designed and developed by Paolo Musico/INFN used by the GEM trackers of the SBS program and adopted by the upcoming MOLLER

APV25

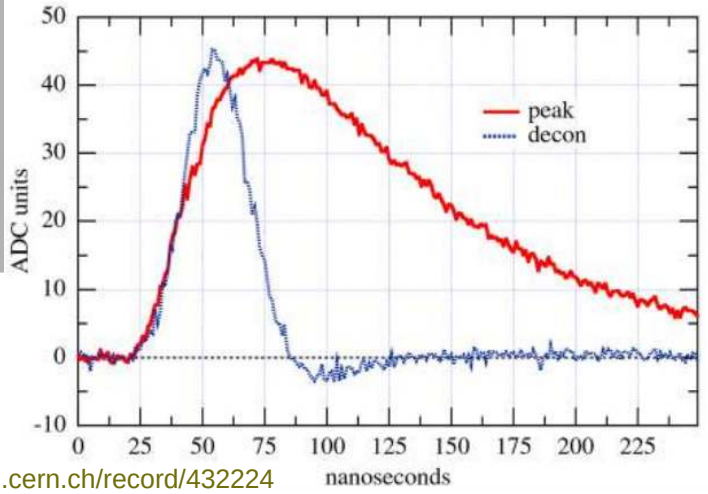


- 128 analog channels / APV25 ASIC
- Capable of sampling signal at up to 40 MHz (25 ns)
- Pipeline with up to ~160 analog samples/ch → up to 4 µs trigger latency
- Multiplexed readout (128 signals in sequence transferred to MPD back-end)

no specific cooling required

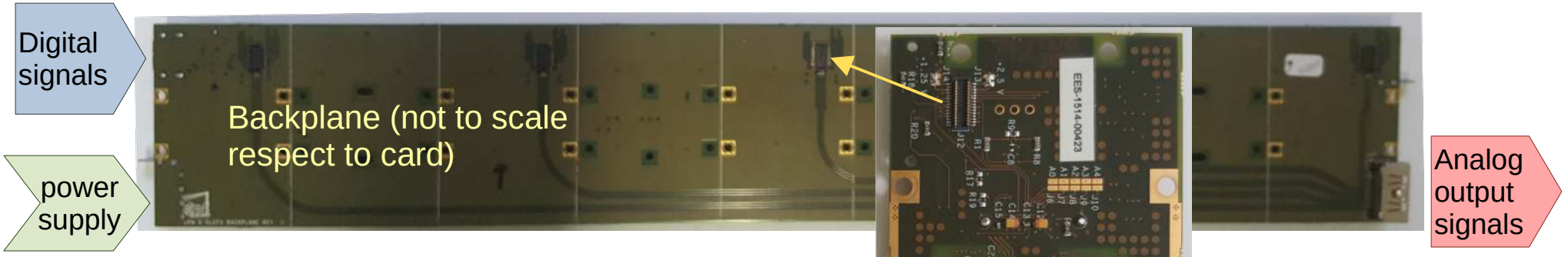
Ipre = 85; // 98
Ipcasc = 45; // 52
Ipsf = 30; // 34
Isha = 30; // 34
Issf = 30; // 34
Ipsp = 48; // 55 FIR Filter
Imuxin = 30; // 34
Ispare = 0;
Vfp = 30; // 30
Vfs = 60; // 60
Vpsp = 25; // 40 analog baseline
	// calibration/test pulses
	
	Ical = 160; // **calibration pulse value**
	Cdrv = 0xDE;
	Csel = 0;
	CalPulse = 0; // 0=off, 1=on
		Latency = 90; // 0..191, suggested less than 160
		Muxgain = 4; // 1(-20%), 2(-10%), 4(0), 8(+10%), 16(+20%)
		Polarization = 0; // 0=non-inverting, 1=inverting
		ReadOutMode = 1; // **0=Deconvolution, 1=Peak**
		AnalogBias = 1; // 0=Off, 1=on

several configurable parameters



L.L.Jones et al. https://cds.cern.ch/record/432224

APV front-end card for SBS



One APV25 on card → 128 chs

APV can store up to 192 analog samples for each channel (up to 160 considered safe) with sampling time down to 25 ns

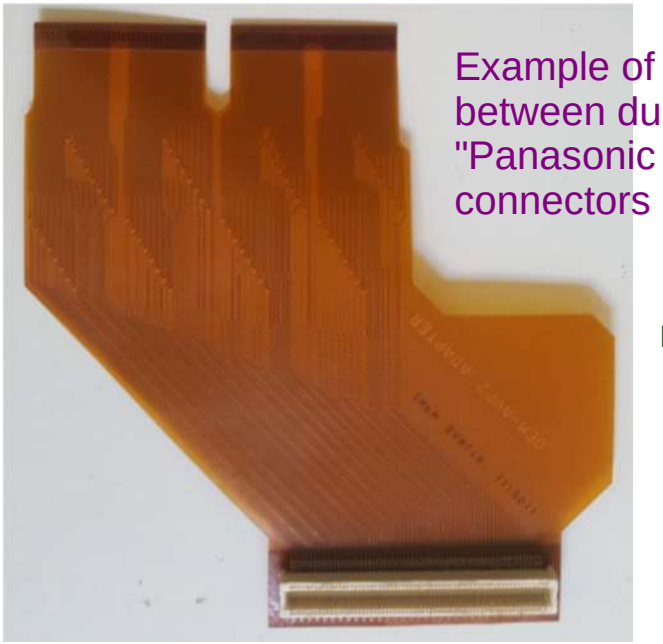
Typical trigger latency (in SBS) <1 us (up to ~4.0 us available at 25 ns)

Channel signals are multiplexed on the card and transferred to the MPD in series at up to 40 MHz

Time required to transfer one sample of 128 chs (include header and footer bits): ~3.5 us

Signals from different cards are sent in parallel

Power: 1.25 V and 2.5 V provided by the rad. hard. voltage regulators on the rigid backplane

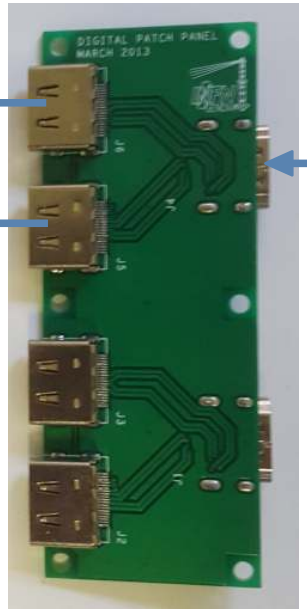


Example of adapter between dual ZIF and "Panasonic 130 pin" connectors

Does not introduce noticeable noise

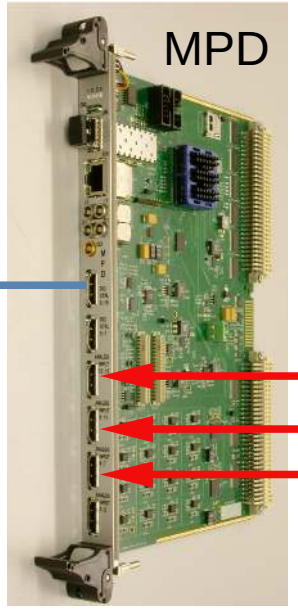
Backplanes and Patch Panels

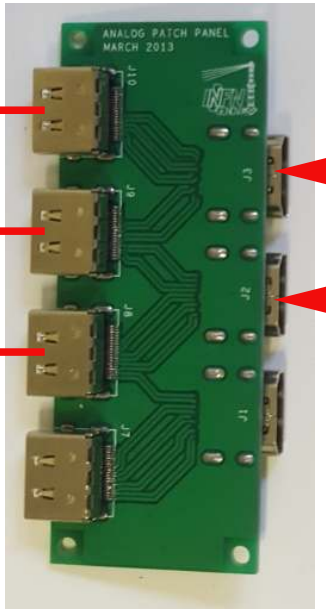




digital signals

clock, trigger, control signals

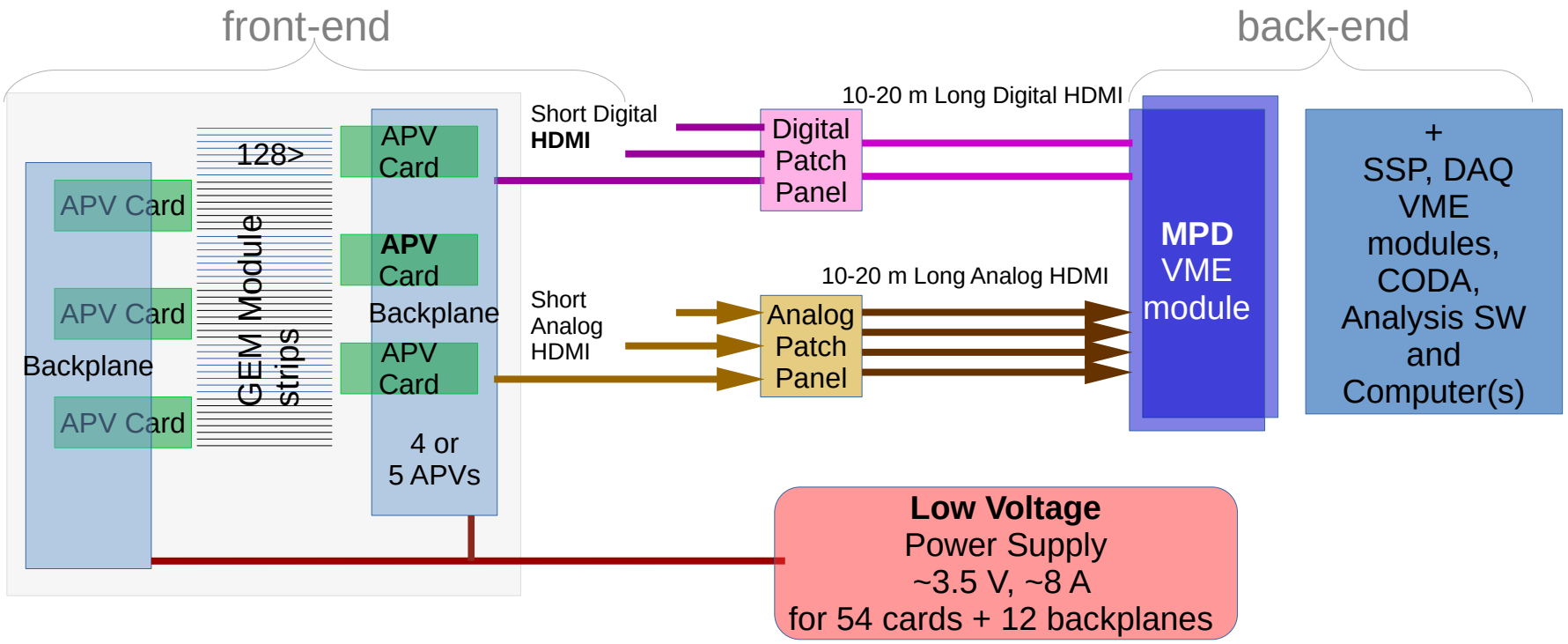




analog signals

not to scale

Electronics Schematic View



up to 16 front-end Cards	up to 3 Backplanes	3 Digital Cables	1 Digital Patch Panel	2 Digital Cables	1 MPD	Optical Link, VME/SSP/ VTP ...
		3 Analog Cables	1 Analog Patch Panel	4 Analog Cables		

How it looks like



~7000 channels
54 APV cards
4 MPDs



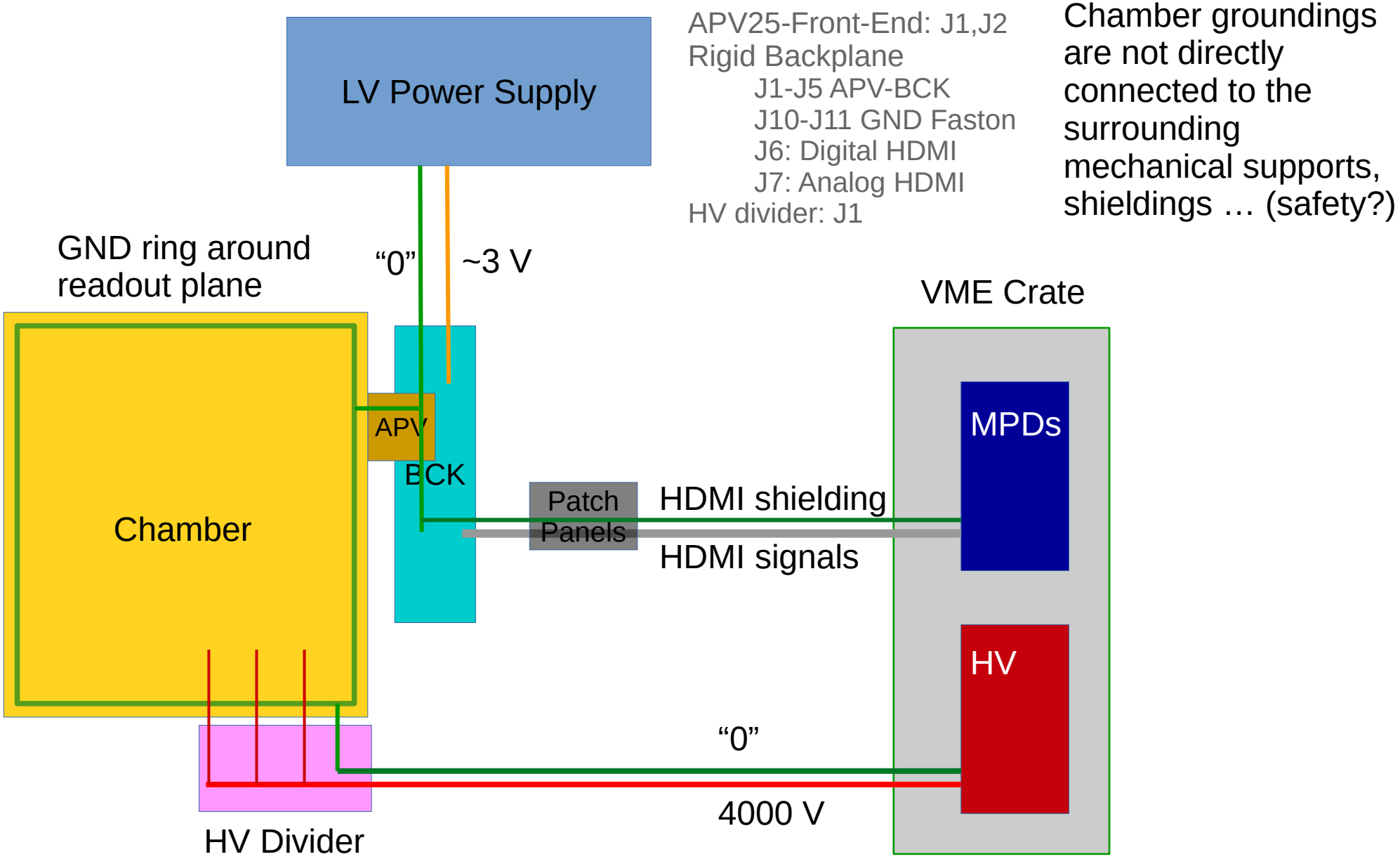
VME crate
(without optical link)

Grounding Scheme (in cosmic test area)

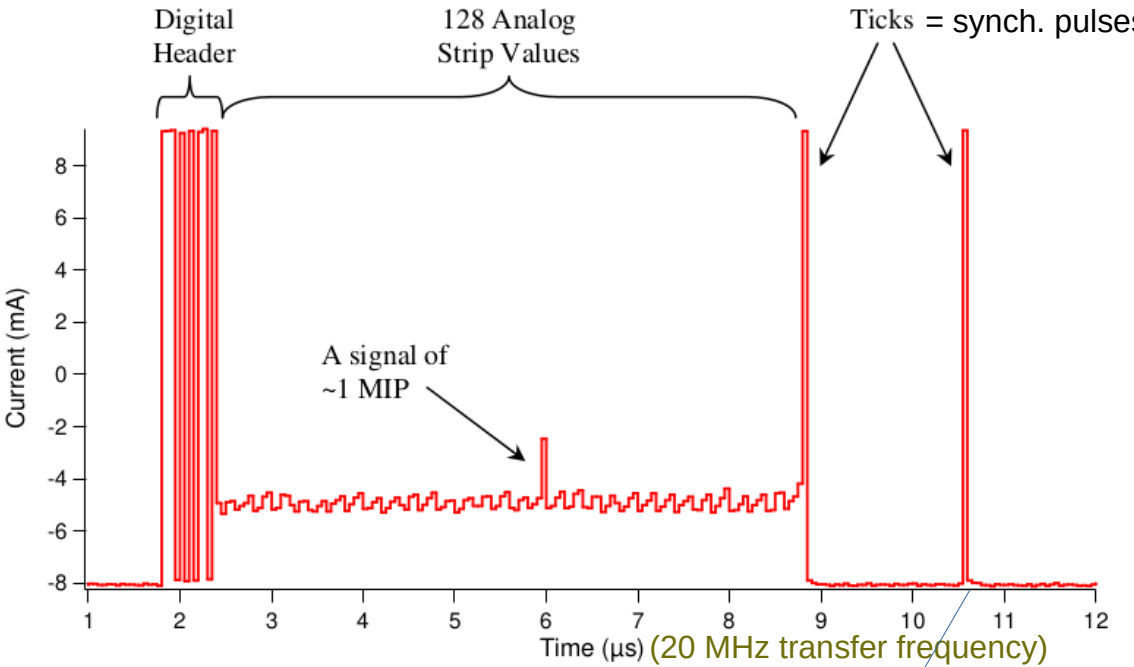
Green lines represent the grounding

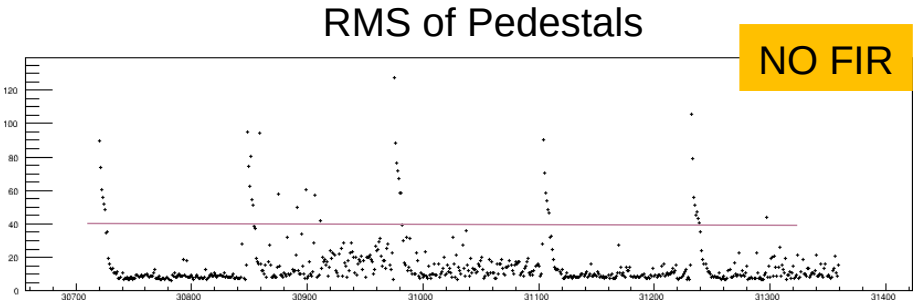
Connectors involved:
APV25-Front-End: J1,J2
Rigid Backplane
J1-J5 APV-BCK
J10-J11 GND Faston
J6: Digital HDMI
J7: Analog HDMI
HV divider: J1

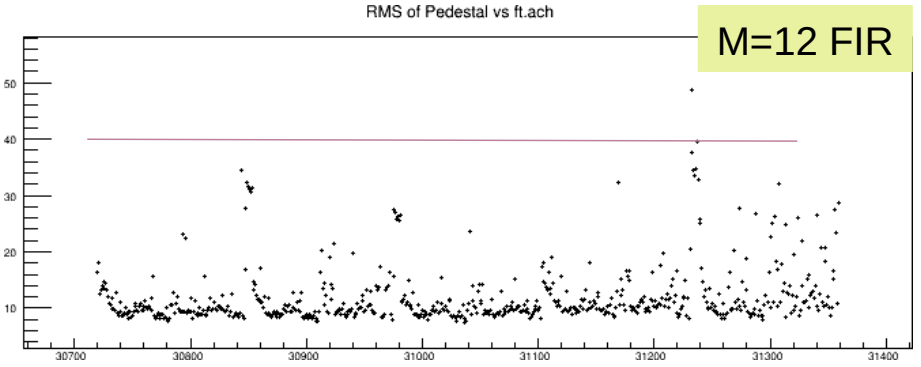
Chamber groundings are not directly connected to the surrounding mechanical supports, shieldings … (safety?)

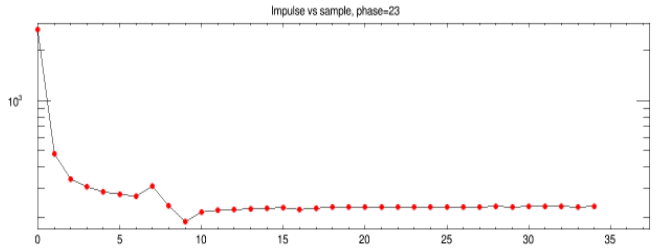


APV25 data frame









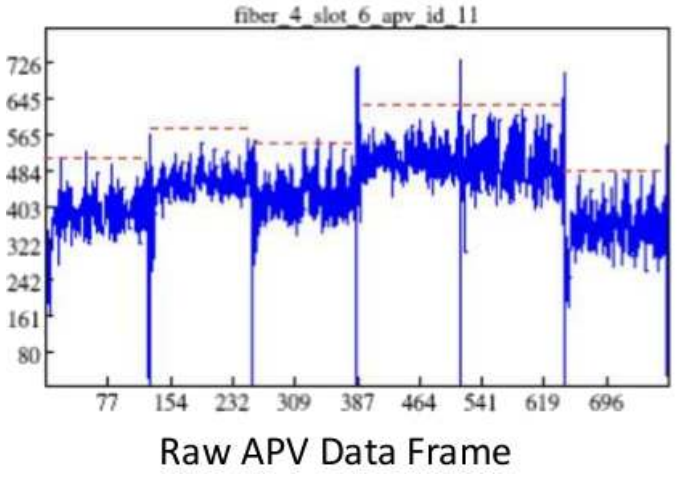
Due to cable impedence mismatch the digital header tails influence the first analog signal levels →FIR filter required (Belle, 2012 JINTS 7 C01082) for online suppression (offline analysis provides better mitigation)

Longer the cables larger the effect

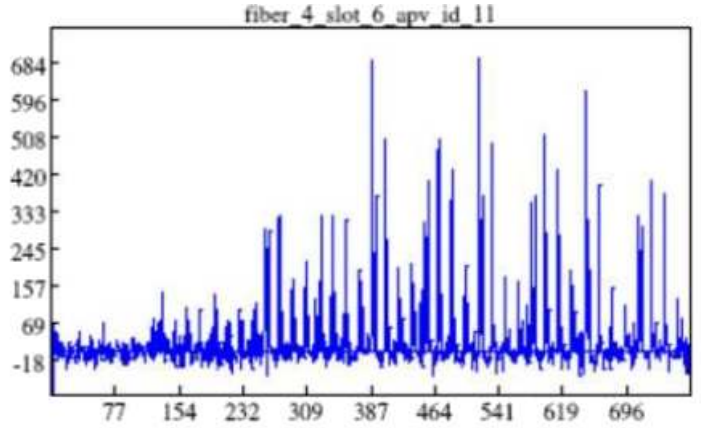
Online Zero Suppression

Shall take into account at least 2 APV25 specific aspects:

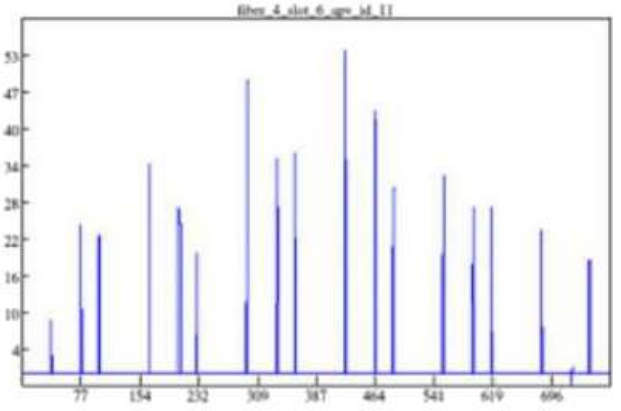
- Digital header impact on analog signals
- Common noise (random offset common to each sample of all channels of a single card)



Raw APV Data Frame



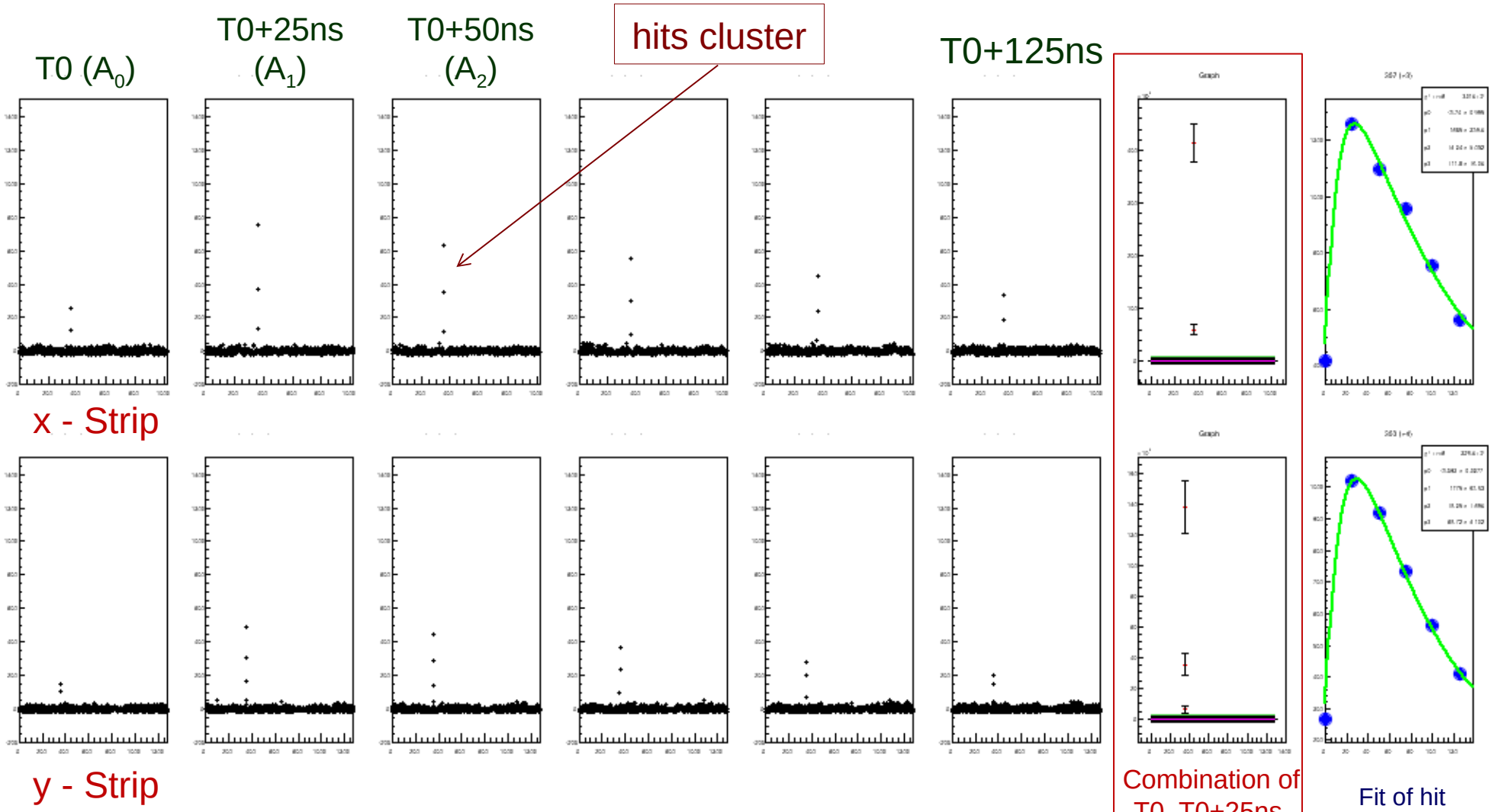
Offset & Common Mode Correction


Zero Suppression

adapted from X. Bai – UVa, 2023

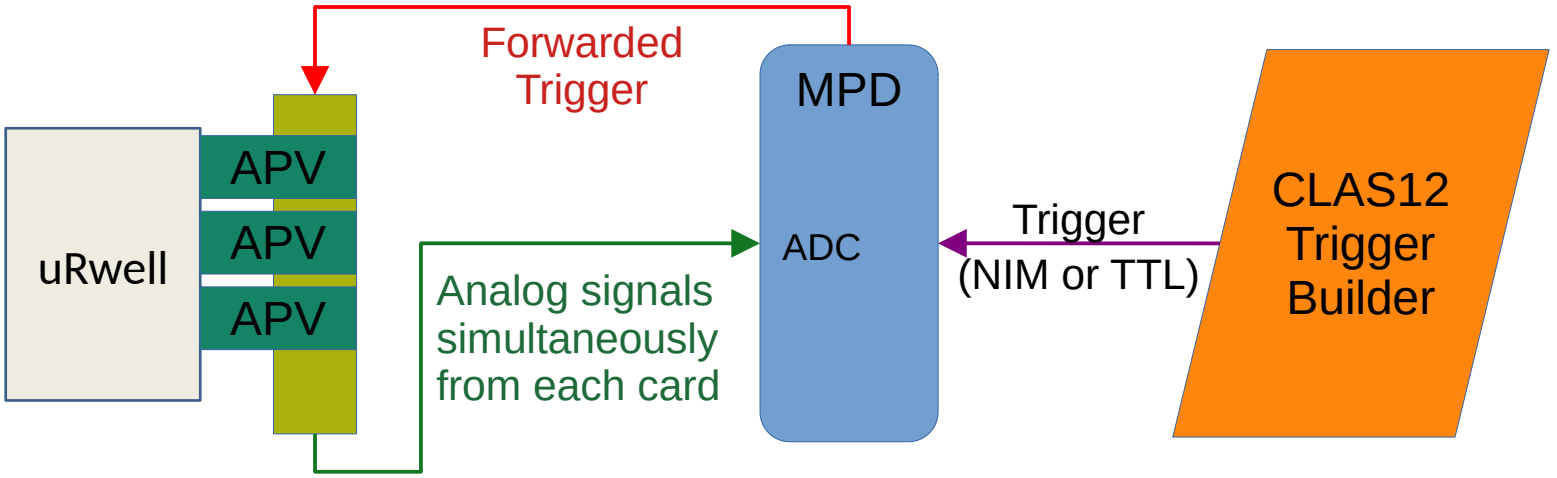
Example of sampled event

6 samples



Desirable 9 samples readout / event

Trigger and APV readout



Trigger to APV shall be provided within ~4 us (max latency) after passage of particles on uRwell (160 pipeline registers x 25 ns)

- MPD add few tens of ns (~1 clock cycle) to the Forwarded Trigger
- Need to add also the propagation time on the cables (~4.5 ns/m)
- Parallel analog readout from APV and conversion to digital require:

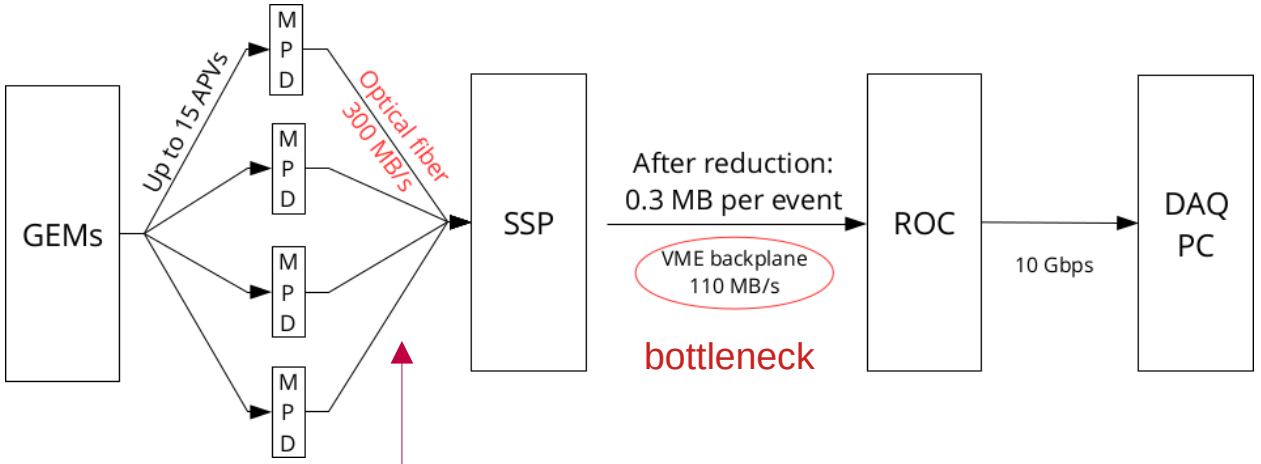
  ~3.5 us/sample, 6 samples → ~21 us

  one event size from one MPD ~ 50 kB (4 byte * 128 * 6 * 16)

Max data rates (in SBS)

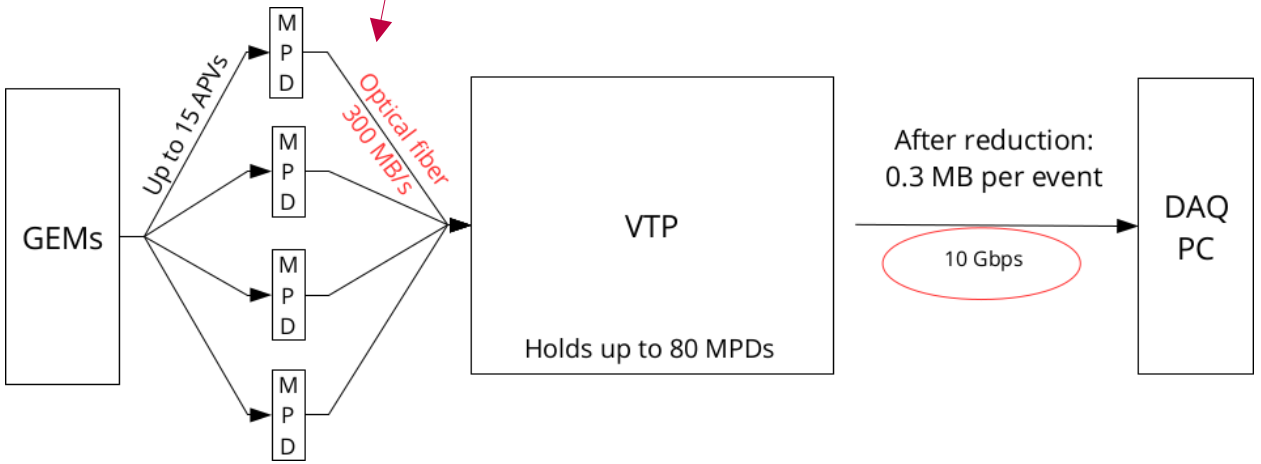
~1200 APV 6 samples/channel/event
raw data volume: ~3.6 MB/event (32 bits/channel)

Ben and Danning/2020



max event rate ~6 kHz

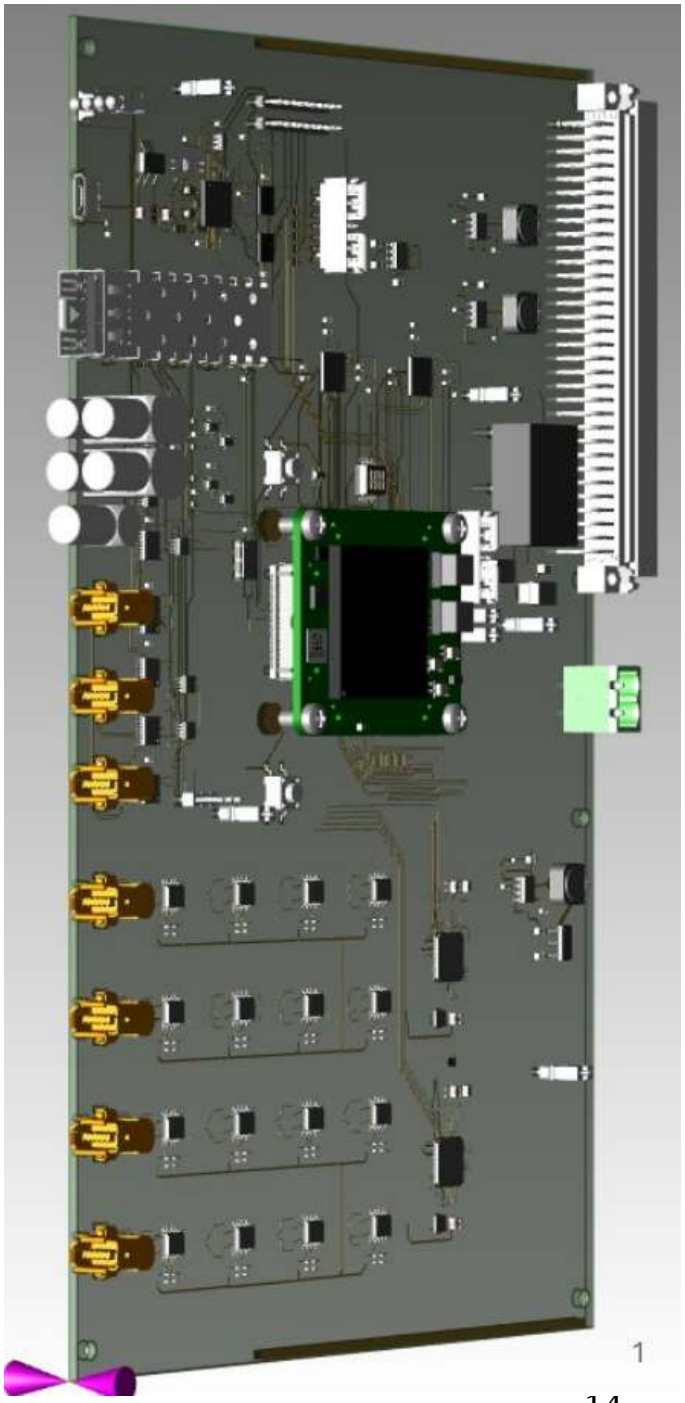
sustained event rate in GEp5 SBS ~ 5 kHz



adapted from P. Musico presentation

MPD new version

work in progress by Paolo Musico



Why:

- Increase data rate
- Obsolete FPGA in current MPD
- DELAY25 is an old CERN device

New:

- New (more powerfull) FPGA
- VME moves to Ethernet (1Gb/s or 10 Gb/s)
- Move to trigger rate up to 30 kHz
- Larger number of samples
- New cabling toward front-end APV25

Keep:

- Cost competitive
- Same form factor of previous version
- Reuse most of the current DAQ software

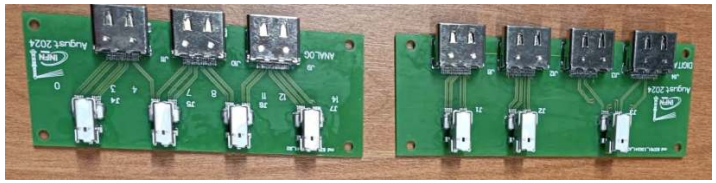
MPD_Eth functional blocks

Trigger rate (16 APVs, 6 samples, no on board processing):

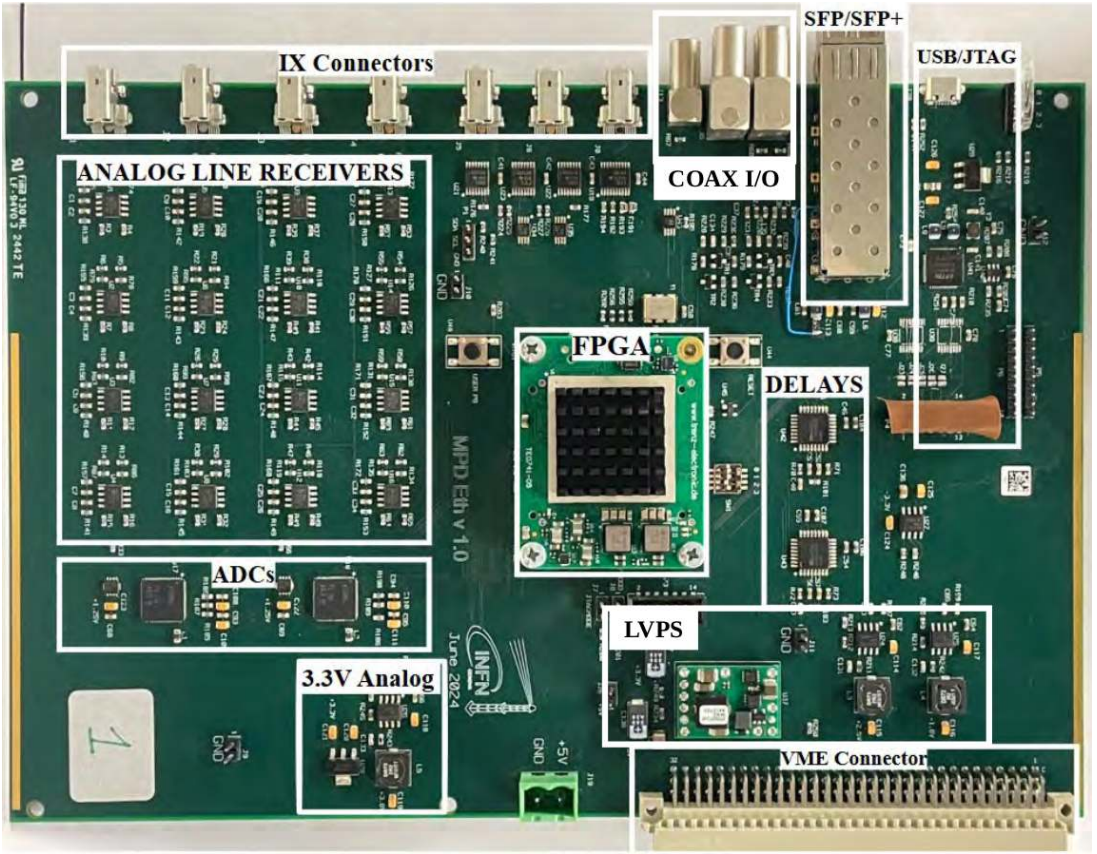
- 5 kHz with 1 Gbps interface
- up to 40 kHz with 10 Gbps interface; current FPGA implementation support 25 kHz but can be improved

VME crate can be used for housing and power (no data interface)
Power can be provided also independently from VME

HDMI cable replaced by **Harting IX** more manageable than HDMI (similar to Ethernet cable but shielded and specific locking connectors) → new patch panels



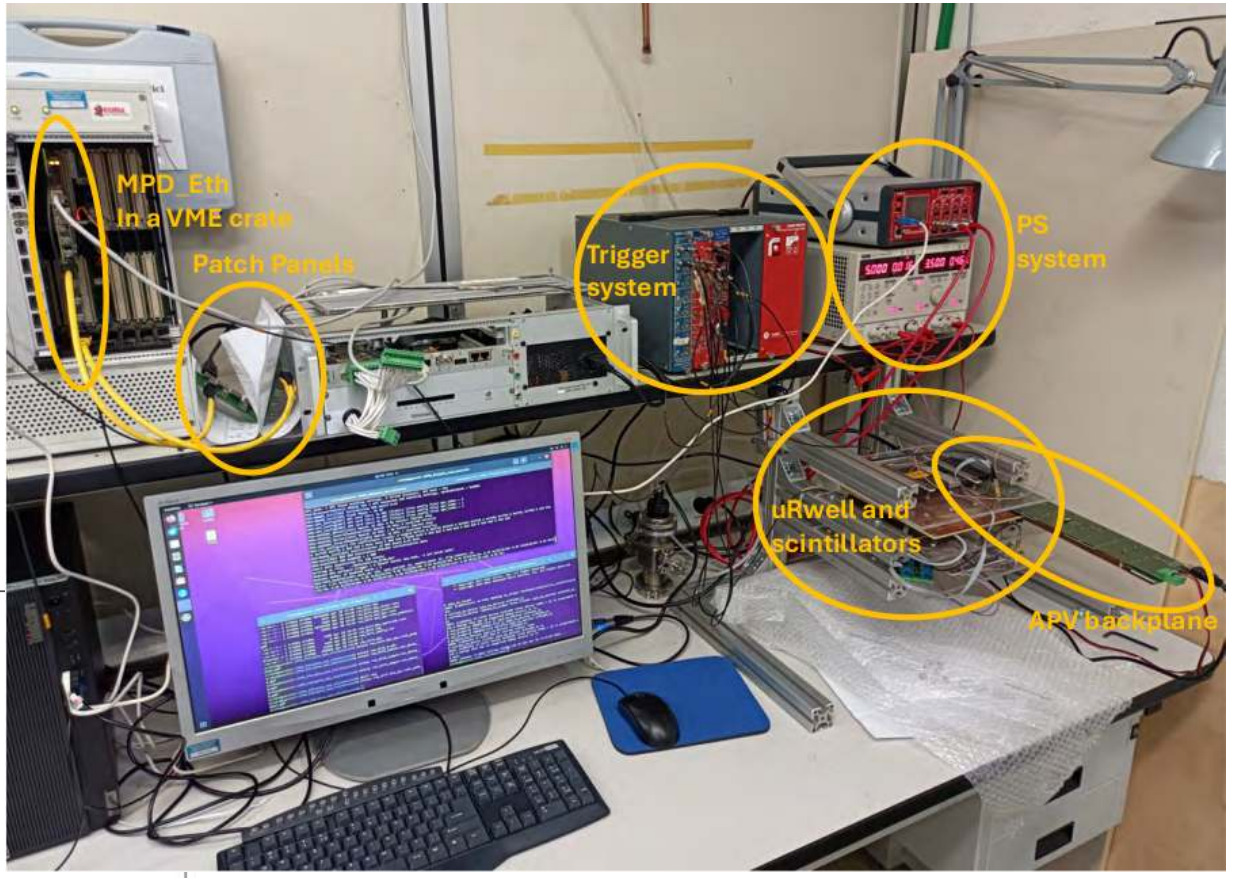
Same backplanes and APV cards



New MPD tested on uRwell

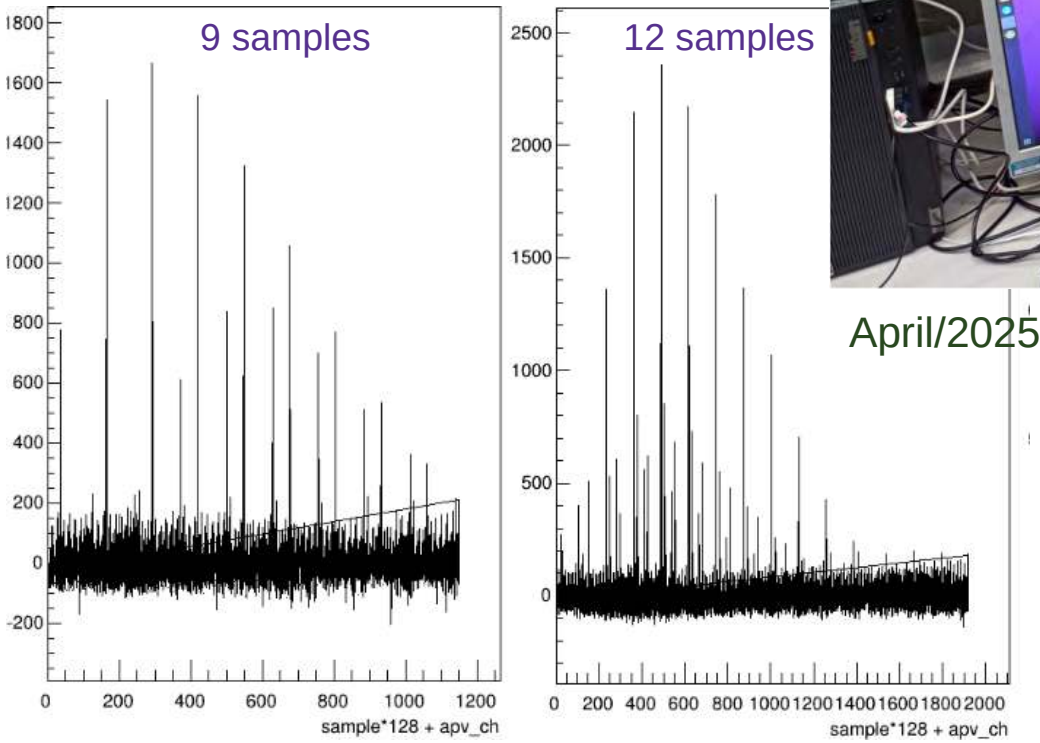
Reused most of the DAQ code except low level I/O and delay setting routines

Adjusted address map, FIFO sizes, output function to create data files compatible with the analysis code (not modified)



April/2025

adapted from P. Musico presentation



Software available on INFN git server:

git@baltig.infn.it:musico/gdaq_mpd_eth.git