HPS SVT · JLAB TEST STAND

SVT DAQ commissioning

Both COBs now take CODA data on the test stand, one at a time. Next: both together, then the first FEB and module.

M. Gignac (SLAC) · HPS collaboration meeting · [2026/10/19]

Where we stand

Software rebuilt

One install, deployed from git. Host, boards and CODA readout all on the same version

COB 0 in CODA

TI triggers reach all 7 data DPMs and CODA; every event delivered, no DAQ errors (9 Oct)

COB 1 in CODA

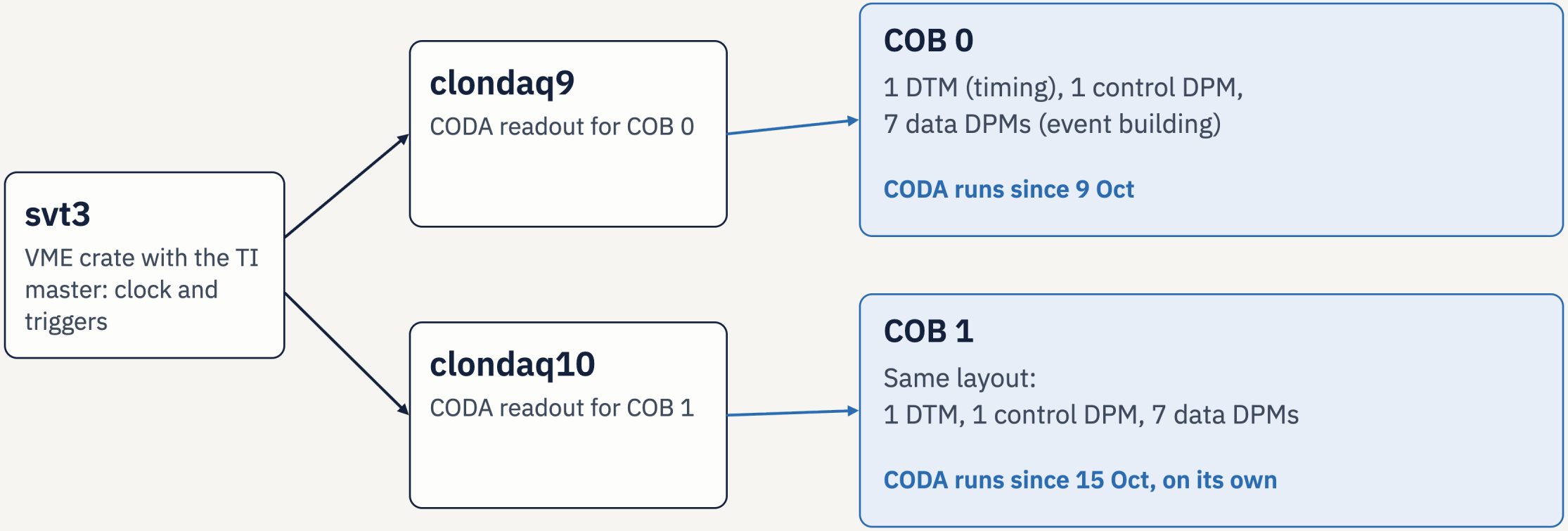
Same result on the second COB, run on its own (15 Oct)

Not yet

Both COBs at the same time; FEBs and modules

Still open: errors reported by the downstream data decoder, while the DAQ's own counters are clean.

The test stand



Arrows: timing fibers. Both COBs sit in one ATCA crate. No FEBs or modules yet, so every event carries SVT headers only.

Timeline, 4 September to 15 October

4 Sep	Work starts on the first COB at JLab.
10 Sep	All networking for the first COB in place.
22 Sep	Second COB shipped from SLAC to JLab.
24 Sep	Second COB received by S. Boyarinov; adapted to boot via TFTP and NFSv3.
5–9 Oct	Install rebuilt from git; board software matched to the host; DTM firmware updated.
9 Oct	Self-trigger test on COB 0, then the first CODA runs on COB 0.
13 Oct	Status review with the SVT DAQ experts.
14 Oct	Crate investigation for running both COBs: crate manager and backplane links.
15 Oct	CODA runs on COB 1, on its own.

S. Boyarinov on site for the boot server and CODA; B. Reese on firmware. On site at JLab 18–27 October.

Self-trigger test, without CODA (9 Oct)

Script daq_selftest.py on COB 0: the DTM sends software triggers, the 7 data DPMs build events, and the host writes them to a file. Run in stages, each adding one kind of action.

Stage	What it does	Result
1 · Configure	Load the configuration and read it back; register writes only	Settings as configured; TI clock 125.003 MHz
2 · Data file	Also open and close the host data file	File written with the configuration record
3 · 1 and 5 triggers	Full run sequence, exactly 1, then 5, software triggers	Every DPM: N triggers in, N events out; no errors
4 · Full run	Software trigger for 30 s; counters checked every 5 s	87 triggers; all 7 DPMs built and sent all 87; zero errors

Tested: trigger distribution in the crate, event building on every DPM, network transport, host file. **Not tested here:** TI triggers and CODA, shown next.

CODA runs: every trigger reaches every DPM

1 · Set up
TI master on svt3 plus one readout PC for the COB. No FEBs.

2 · Prestart
SVT configuration loaded; readout connects to the 7 data DPMs and clears old data.

3 · Go
TI random trigger, nominal 15 Hz, for about a minute.

4 · End and check
Register snapshots at Go and End: TI triggers vs events built on each DPM; error counters.

COB 0 · run 2044 · 9 Oct · 72 s

952	7/7	0
TI triggers	DPMs with every event	DAQ errors

COB 1 · run 2051 · 15 Oct · 47 s

479	7/7	0
TI triggers	DPMs with every event	DAQ errors

Board settings match the June 2024 EEL run, apart from the DTM firmware and that run's FEBs.

NOTICED AND FIXED DURING BRING-UP

The test-stand boards were set up with a 2019 software version

What we saw

The board server loaded rogue v3.7, while the host runs 5.9.3. Checked in the running process.

Why it mattered

As we read the code, this pairing would report errors on the boards as success.

Now

Boards and host both run 5.9.3, and every run shown here was taken that way.

> Earlier runs did not use v3.7 on the boards, so they are not affected.

Next steps

1	**Both COBs together:** on site 18–27 October, with hands at the crate.
2	**Decoder errors:** check them on a short data file; they may come from the header-only events.
3	**Longer CODA runs** on both COBs.
4	**First FEB and module:** agree a cooling and interlock plan first (FEBs on an MPOD, no chiller on the test stand); then power, sync and baseline.

Procedure: clonwiki0.jlab.org, ATCA page. Software, configurations and status: github.com/mgignac/hps-svt-jlab-install.

Outstanding issues

Two-COB operation

Symptom

Each COB boots and takes data on its own. With both in the crate, the second one does not come up.

Checked so far

Backplane links between the COBs are off (seen from COB 0). The crate manager's backplane network port is down.

Suspects

A network loop through the external switch, as seen at SLAC (fixed there with spanning tree); COB 1's switch setup; boot order.

Did two COBs ever run together in this crate, and how was the network set up?

Decoder errors

Reported downstream; DAQ counters are clean. Possibly header-only events.

2024 config files

The June 2024 EEL configuration directory is missing. Does anyone have a copy?

FEB power and cooling

Plan and sign-off needed before the first FEB: MPOD, no chiller.

BACKUP

Technical details

Crate findings · software and firmware versions · DTM firmware · standalone test · how CODA finds the SVT configuration · configurations

Crate findings, 14 October

Item	What we found	Read with
Backplane	5 slots; fabric full mesh, base dual star with hubs in slots 1–2. The COBs (slots 1, 2) link directly on fabric ch 1, base ch 2, update ch 1	clia shelf ppc, address_table
E-Keying, COB 0	All 4 fabric channels reported disabled	PICMG Get Port State
COB 0 switch	Backplane ports 12–15 "Not Connected"; ports 0–8 to the RCEs (1G); port 23 uplink (10G)	cob_dump_bsi --switch
Shelf manager eth1	Down, no carrier; not in any startup file	ifconfig on the shelf manager
Hot swap	After crate restarts, both COBs sat in M1 (unpowered) and never asked to activate	clia board, clia sel

Not read yet: COB 1's switch setup and port states; spanning tree on the external switch. Shelf manager SSH (dropbear 0.48) is too old for RHEL9 clients; use telnet.

Software and firmware versions

Component	Running now	Notes
Host environment	rogue 5.9.3, Python 3.7 (conda)	5.9.3 package gone upstream; archived in the kit
DAQ code	heavy-photon-daq jlab-teststand-2026	origin/Run2021 + test-stand changes
Board server	rogue 5.9.3, built on dpm0 (ARM)	/mnt/hps = 2.1.0/slac_svt/rce_daq
CODA readout	rogue_lite 5.9.3 + rogue_coda, from source	CODA 2.1.0, RHEL9; same API as 2024 libraries
DTM firmware	PcieTiDtm a46cb251 (2021-09-01)	2024 ran 56a18b7 (+ TiSyncTimer debug register)
DPM firmware	ControlDpm 4167438, DataDpm ee4c4eb	Unchanged; same as 2019 and 2024

Branch: github.com/slaclab/heavy-photon-daq, jlab-teststand-2026 · install kit: github.com/mgignac/hps-svt-jlab-install

Firmware: DTM moved to a46cb251

Board	Image now	Built	Before
DTM	PcieTiDtm a46cb251	2021-09-01	56a18b7 (2024), af99a24 (2019)
Control DPM	ControlDpm 4167438	2019-06-19	unchanged
Data DPM	DataDpm ee4c4eb	2019-06-28	unchanged

Why a46cb251

Ben's recommendation: newest DTM build on the Run2021 line. 56a18b7 is the same plus a TiSyncTimer debug register.

Software matched

Branch reverts TiSyncTimer, so it equals origin/Run2021 plus our changes; works with either image.

Loaded and checked

Same part and size as 56a18b7, checksummed; Sergey loaded it. dtm0 reports a46cb25; all register blocks answer.

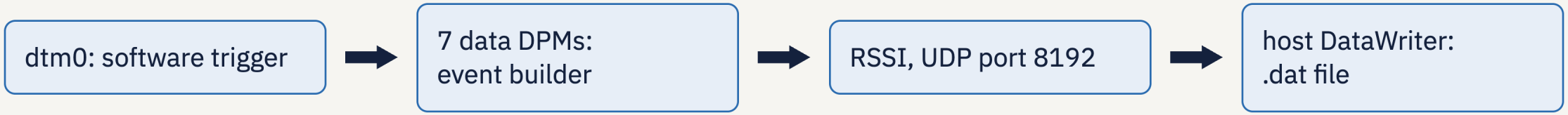
Data path demonstrated on COB 0

87
triggers sent

7
data DPMs in lockstep

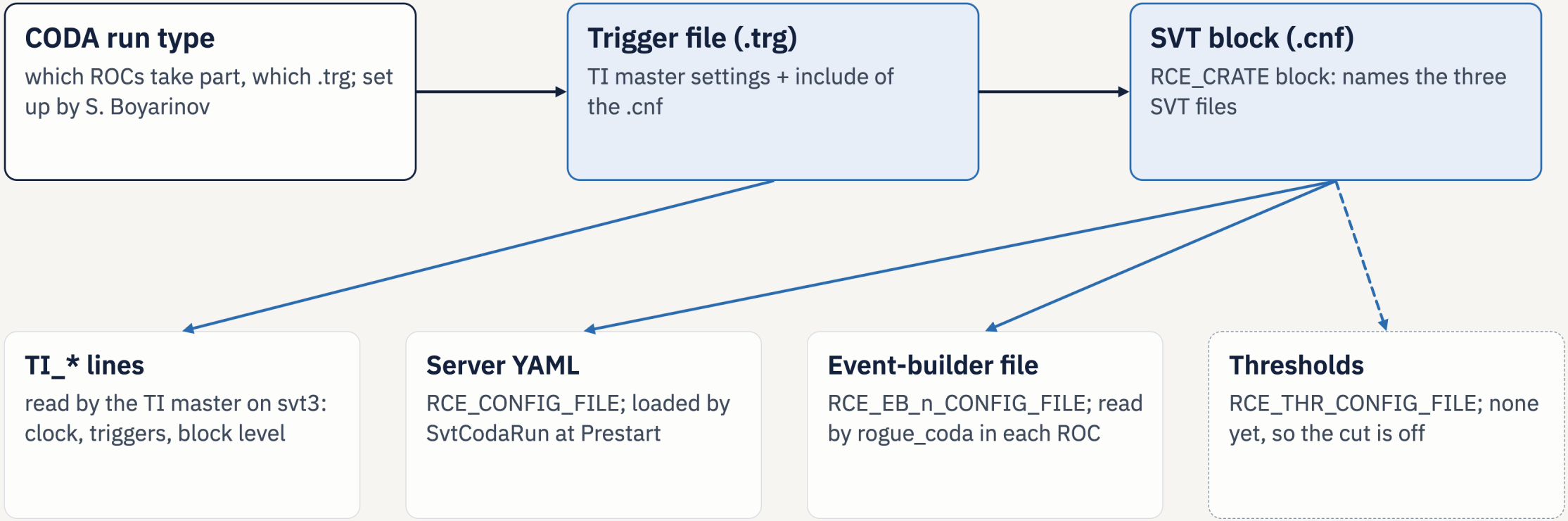
609
events in the file

0
burn, header or sync errors



No FEBs, so every event is headers only (BlankHeads = TriggersIn on each DPM). The DTM's TiTriggerCount stays 0: it counts TI triggers, which software triggers bypass. TI triggers through CODA followed the same day.

How CODA finds the SVT configuration



.trg and .cnf: parms/trigger/HPS/TestStand2026 (deploy_coda.sh). YAML and event-builder files: server/install/configs (deploy_svt.sh).

Configurations, one set per setup

Setup	Server YAML	CODA trigger file	Status
COB 0, no FEBs	svt_single_cob.yml	hps_cob0_noThr_svt3.trg	Used: selftest, CODA
Both COBs, no FEBs	svt_cobs_only.yml	hps_teststand_noThr_svt3.trg	Ready
COB 0, one FEB, one module	svt_cob0_1feb.yml	hps_cob0_1feb_noThr_svt3.trg	Template
Full detector, 10 FEBs	svt_full.yml	hps_full_noThr_svt3.trg	Template

Where the values come from

2024 EEL Run 28 state dump (Old and Layer0 hybrids); 2019 JLab file for New hybrids and the FEB list. The 2024 files themselves (rce-test-eel-topcob.yml) are missing.

2024 vs 2019, to confirm

Latency 0x90 vs 0x83 · mux gain 1.0 vs 1.2 mA · ADC clock phase 110 vs 60 · AVDD and A29V trims

No configuration sets hybrid power: it is switched by hand. No thresholds yet (threshold cut off). CODA chain and file snapshots follow.