Hardware Status

HPS Collaboration Meeting

Matthew Gignac & Tim Nelson

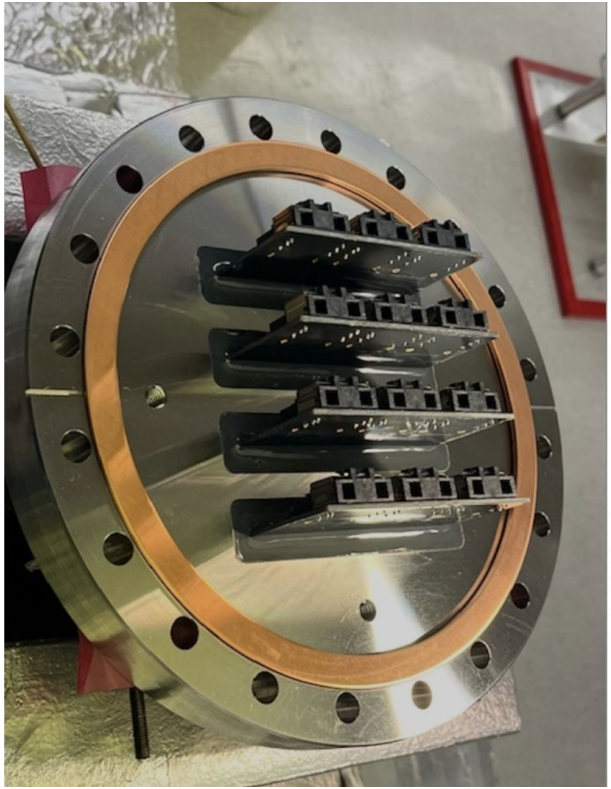
2026/10/19

Introduction

- Lots of work over the last several years to rebuild modules for the SVT and corresponding readout hardware:
  - Rebuilt a second data flange
  - Front End Readout Boards (FEBs)
  - Repaired LV power supplies
  - L0 and L5-7 hybrids
  - Slim-edge sensors
- Future assembly plans (as they stand now)
- Plans for our JLab trip following this collaboration meeting

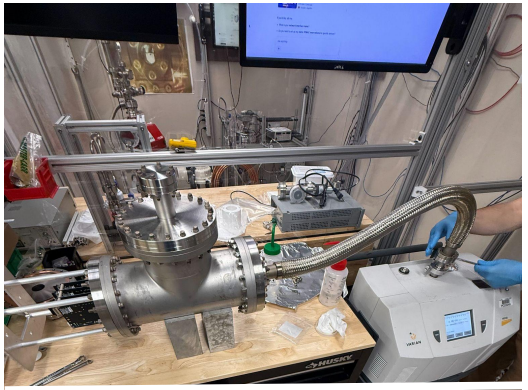
HPS Data Flange

- Extensive electrically testing of the flange boards prior to data flange assembly
  - Fully loaded board with three FEBs powered
  - Operated for ~1h and monitored for link errors
  - All 4 flange boards passed with zero link errors



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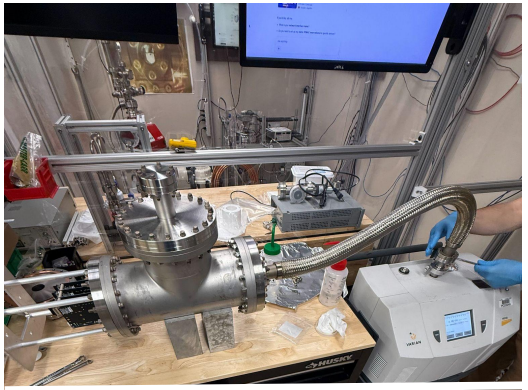
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  - Used two different leak test systems and performed helium leak checks confirming epoxy holds well





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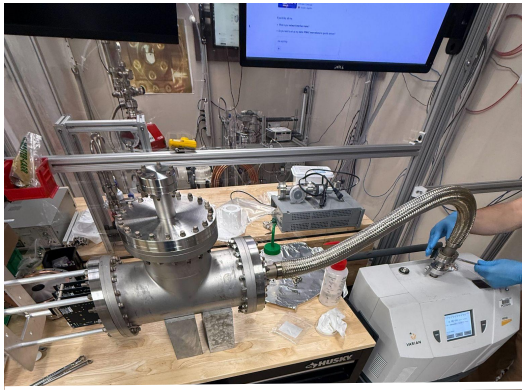
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- **Aiming to readout SVT detector through this new Data Flange later this week**





Front End Boards

- Changes with respect to C02 (confluence):
  - Replace 3.3V Regulator
    - C00-C01 used ISL80113, Not rated for 5.5V Vin
    - Replaced with LT1963A
    - Add TLV803E voltage supervisor to create INIT_B power on reset (U53)
    - 1.8V now powers up before +3.3V instead of simultaneously.
  - Fix FPGA Power-On Reset
    - Final VR PGOOD pin now tied to FPGA INIT_B instead of PROGRAM_B
- All boards have been tested:
  - 13 GOOD boards (3 spares), cleaned in ultrasonic bath, quick re-test and shipped to JLab last week



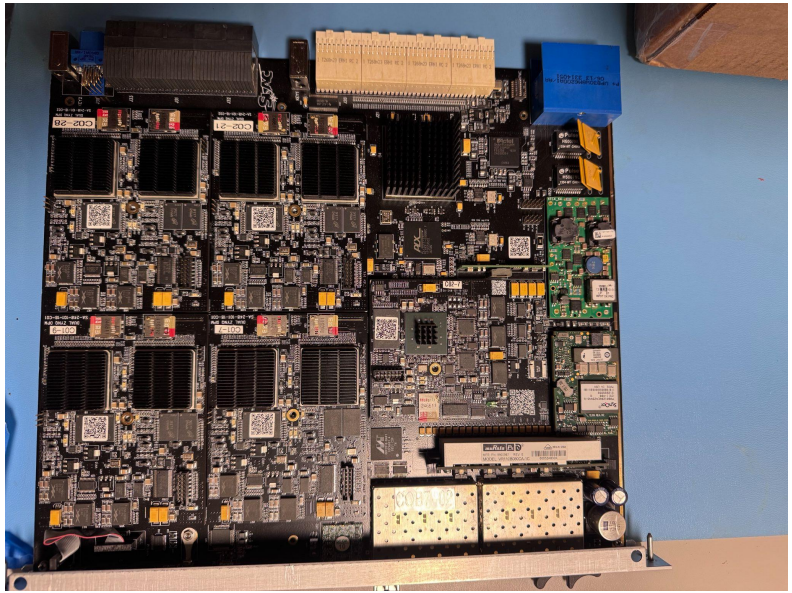
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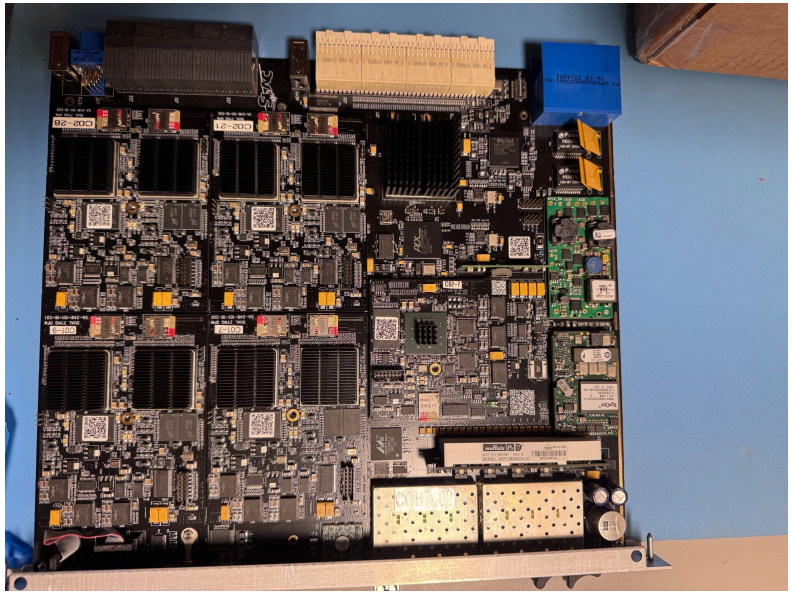
COB repairs

- SVT detector readout by 2 Cluster on Boards (COBs) – second COB had issues with control DPM from last trip in 2024
- Received proto-DUNE spares back from CERN (after much fun organizing export & property control for ~1 year)
- Reconfigured their DPMs/DTM to boot in a similar (diskless) fashion to HPS
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- **Both COBs (individually) boot at JLab and will be used to readout entire SVT**



Migrating away from NFSv2

- Diskless boot of COBs currently requires NFSv2, but it's an obsolete file-sharing protocol and most modern systems have dropped support
- With recent mandatory OS upgrades across DOE compute, this issue has been encountered at both SLAC & JLab: a solid solution is needed!
- Our version of U-boot (<2014) does not support NFSv3
  - However, the Linux operating system kernel *does* support NFSv3
  - And U-boot *does* support Trivial File Transfer Protocol (TFTP)

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  - However, the Linux operating system kernel *does* support NFSv3
  - And U-boot *does* support Trivial File Transfer Protocol (TFTP)
- **Solution**: Use TFTP during U-boot process and NFSv3 for mounting the root filesystem where all our software resides

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- With red… has bee…
- Our ver…
  - How…
  - And…
- **Solutio…** …ne root filesystem where all our software resides

```
TFTP from server 192.168.2.10; our IP address is 192.168.2.194
Filename 'dataDPM/boot/uImage'.
Load address: 0x3000000
Loading: ##################################################################
         ##################################################################
         ##################################################################
         ##################################################################
         ###
         3.7 MiB/s
```

- Tested on COB at SLAC → worked!
- Successfully rolled out at JLab too! (notes)

Power supply repairs

- Several (3 out of 5) LV cards (MPV8008I) had long standing issues that needed to be addressed:
  - SLAC ID: 18055346; Failure: Bad Channel 5; Repair: Update Firmware, Load Factory Configuration,
  - SLAC ID: 18055347; Failure: Bad Channel 4; Repair: Update Firmware, Load Factory Configuration
  - SLAC ID: 18055351; Failure:Interlock Issue; Repair: Replace F1, Update Firmware, Load Factory Configuration
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Power supply repairs

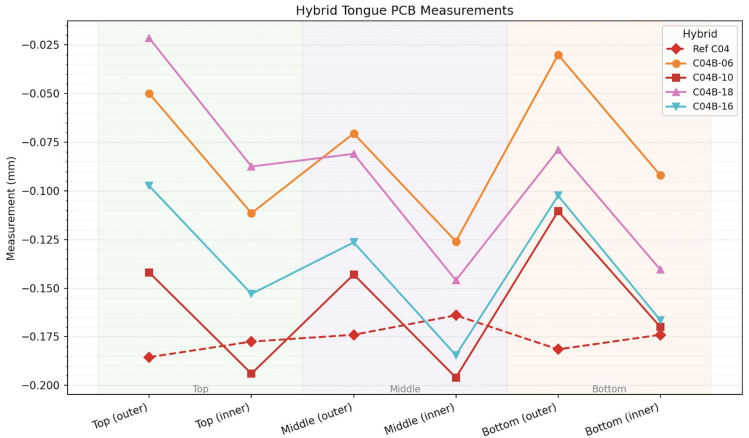
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- Shipped back to JLab earlier this month
- **Need additional sources for our JLab trip, since HV in use at SLAC. Borrowing 1 LV and 2 HV from CLAS / Nathan for our trip**

Hybrid assembly & testing status

- Working with UC Santa Cruz for ASIC attachment wire-bonding
- **Innermost L0 hybrids:**
  - 20 hybrids assembled, tested, and healthy (need 8, leaving 12 spares)
    - 5 found from previous efforts. A few with some bend back-end wire-bonds, but otherwise functional (will use these as spares)

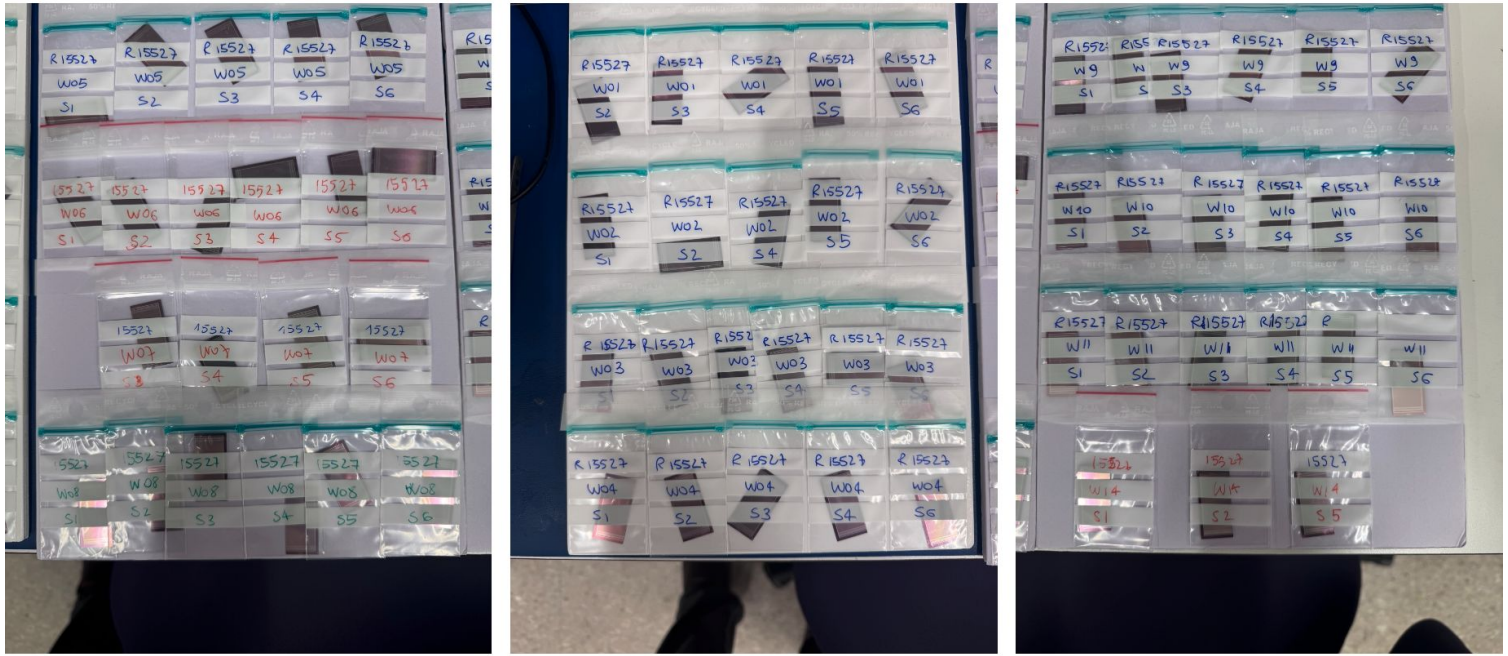
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- **Outer layer L5-L7 hybrids:**
  - 20 C04B version boards (with kapton layer) found, cleaned & populated with components
  - Loading APVs and back-end wirebonds (12/16 finished, next batch almost done)
  - Keeping 4 spares without APVs; will load on an as-need basis to preserve APVs
- Sensor “tongue” a bit thicker than expected, mostly from board bow



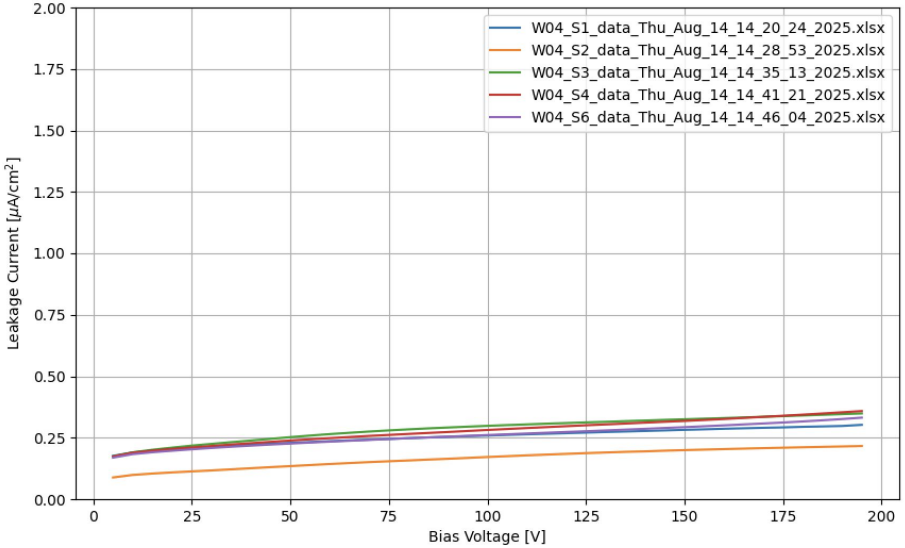
Slim edge sensors

- Slim-edge sensors for L0 & L1 received last year and characterized

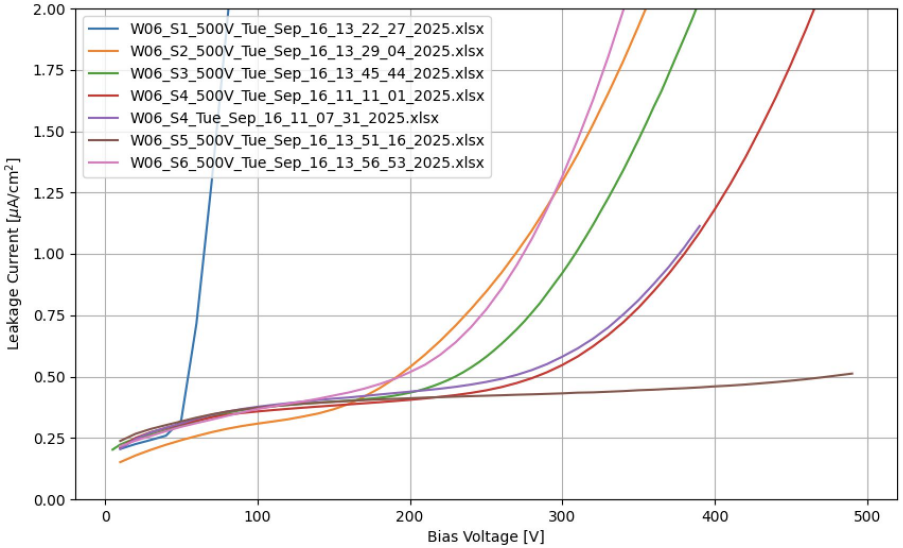


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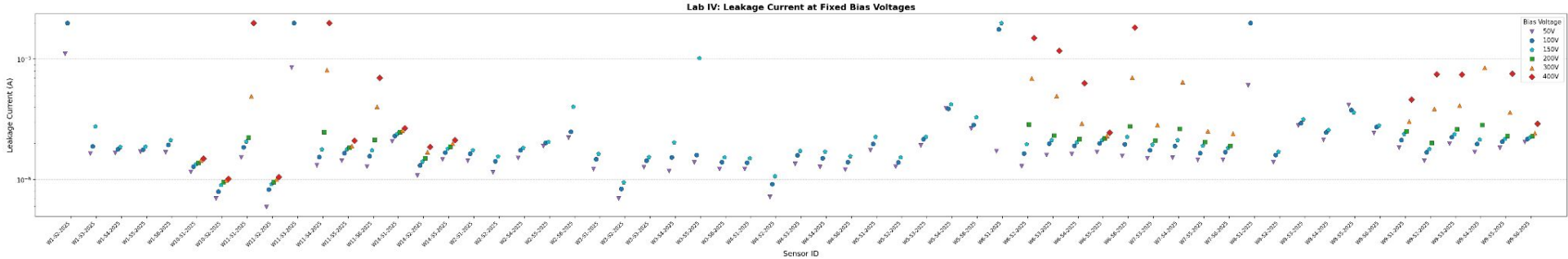
Tested to 200V



Tested to 500 V

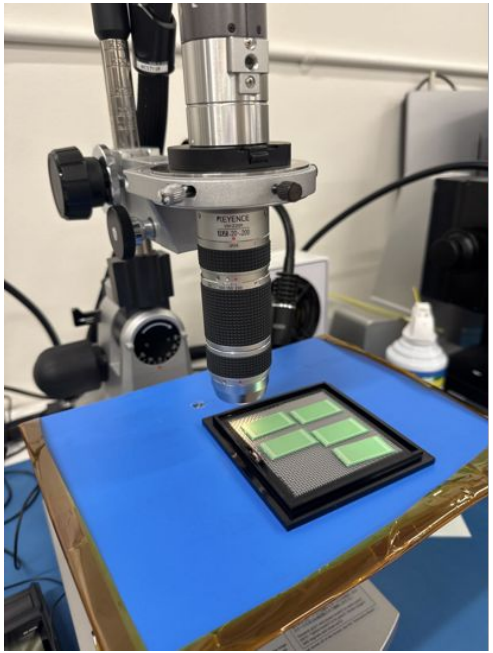
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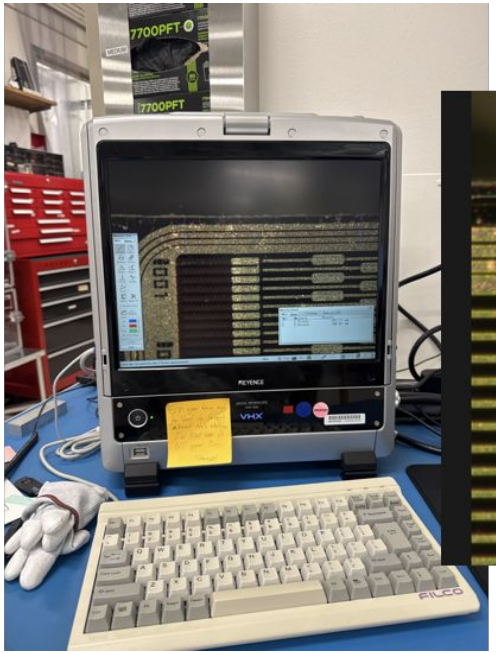
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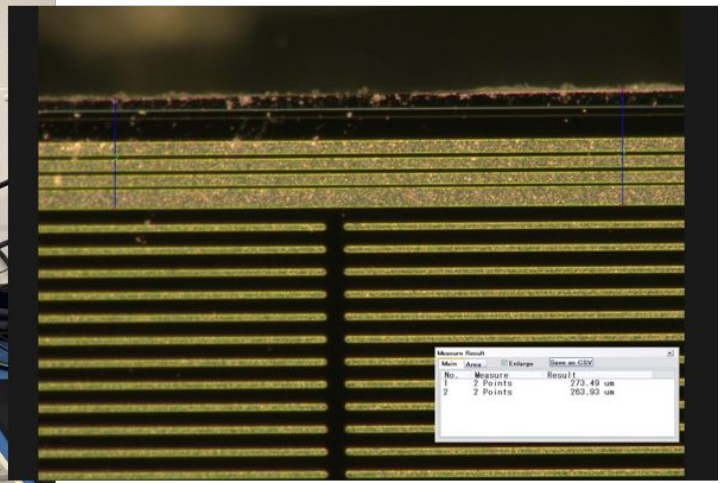


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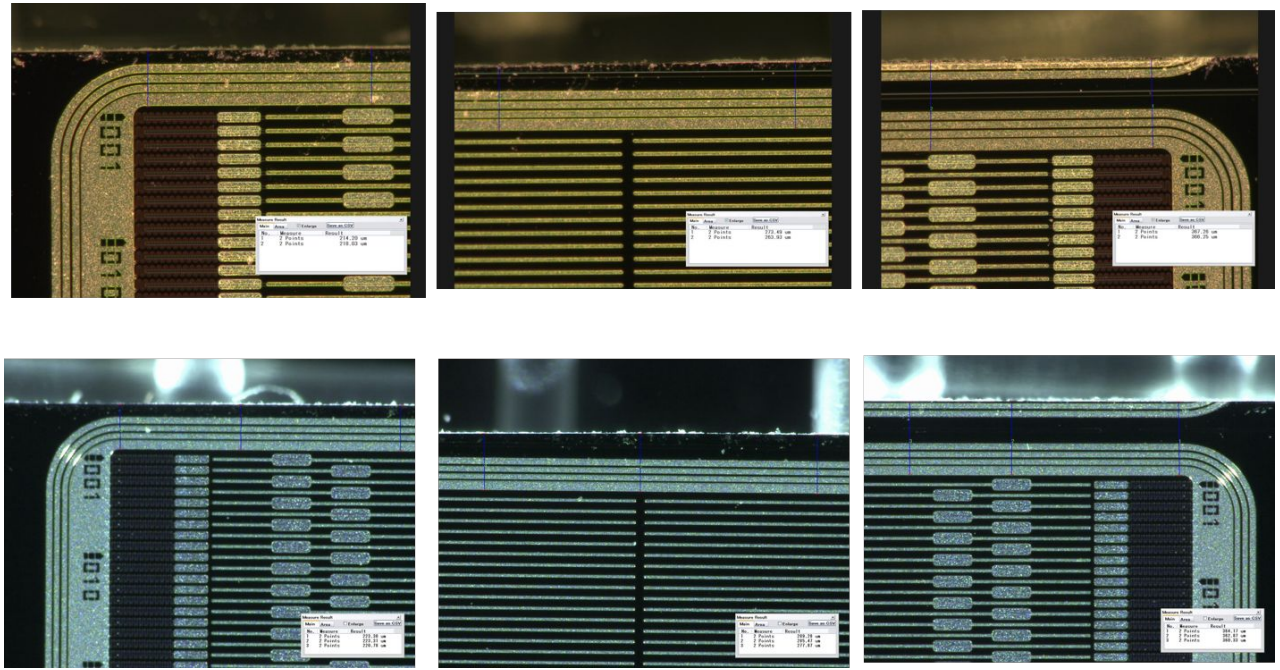






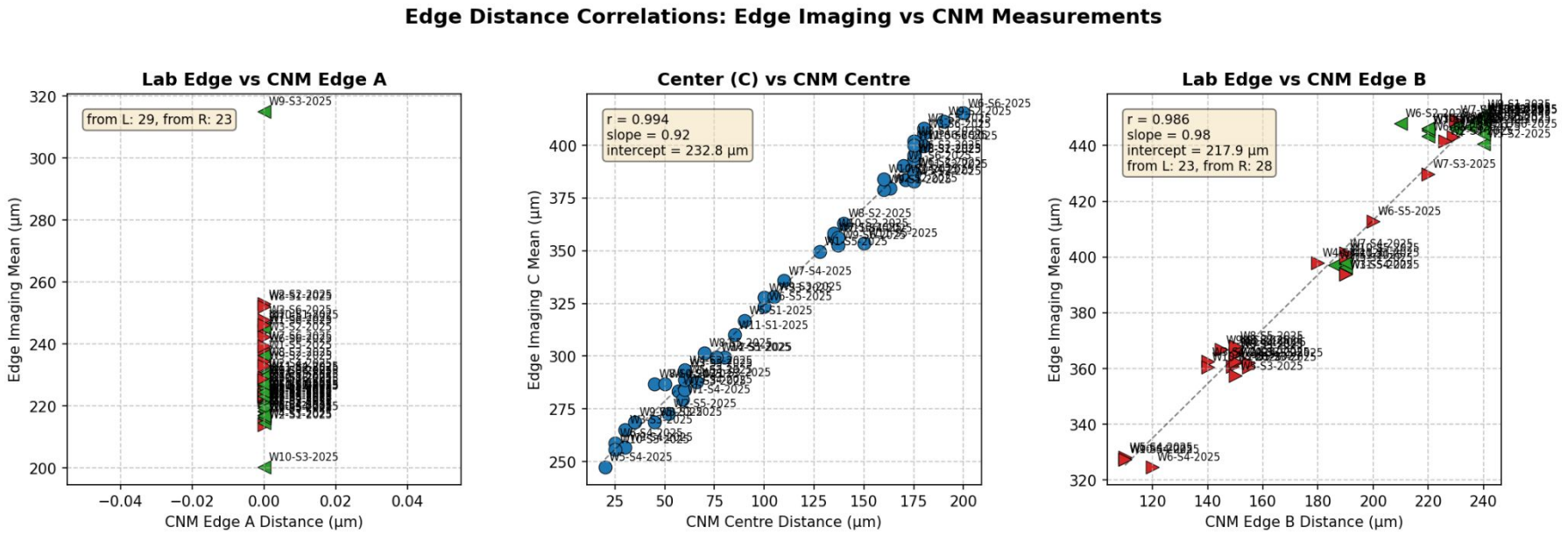
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Slim edge sensor performance

- At least 20 sensors available with good IV characteristics, similar slim edge slopes, and a center slim-edge gap around 250-300um

63 sensors total | 48 shown | 56 with flags | Show fully-tested only

Rank	Sensor	Edge Slope Score	Edge Slope	Center Gap Score	Center Gap	i@100V	IV Slope	IV Score	Max V	Pinholes	Flags
#3 ★	W5-S4-2025	**0.723**	2.72	**0.601**	247.4	**0.633**	3.88e-06	-1.45e-09	**0.886**	195V	1	PINHOLES:1 IV_LIMITED
#4	W3-S3-2025	**0.702**	3.54	**0.481**	265.2	**0.566**	1.44e-06	1.67e-09	**0.973**	195V	0	IV_LIMITED
#5	W9-S3-2025	**0.693**	1.40	**0.794**	328.2	**0.328**	2.25e-06	5.97e-08	**0.815**	490V	1	PINHOLES:1 IV_EXTREME_SLOPE
#7	W11-S5-2025	**0.689**	—	–	353.6	**0.232**	1.66e-06	4.60e-10	**0.966**	490V	0	–
#8	W3-S4-2025	**0.675**	3.56	**0.478**	284.2	**0.494**	1.53e-06	1.55e-08	**0.946**	195V	0	IV_LIMITED IV_EXTREME_SLOPE
#9	W5-S3-2025	**0.674**	3.49	**0.487**	288.9	**0.477**	2.17e-06	1.56e-09	**0.946**	195V	0	IV_LIMITED
#11	W9-S4-2025	**0.660**	3.23	**0.527**	256.8	**0.598**	1.98e-06	6.74e-08	**0.792**	390V	1	PINHOLES:1 IV_EXTREME_SLOPE
#12	W6-S4-2025	**0.657**	3.21	**0.529**	258.7	**0.590**	1.92e-06	8.22e-08	**0.748**	490V	0	IV_EXTREME_SLOPE
#16	W8-S3-2025	**0.634**	4.42	**0.351**	268.7	**0.553**	2.94e-06	1.06e-08	**0.910**	195V	0	IV_LIMITED
#17	W1-S4-2025	**0.631**	4.33	**0.365**	279.6	**0.512**	1.79e-06	5.69e-09	**0.956**	195V	1	PINHOLES:1 IV_LIMITED
#18	W2-S5-2025	**0.631**	4.22	**0.381**	272.8	**0.537**	2.02e-06	1.57e-09	**0.951**	195V	2	PINHOLES:2 IV_LIMITED
#20	W8-S4-2025	**0.611**	4.42	**0.351**	286.9	**0.484**	2.48e-06	9.46e-09	**0.928**	195V	1	PINHOLES:1 IV_LIMITED
#23	W9-S5-2025	**0.596**	4.50	**0.340**	268.7	**0.553**	2.08e-06	6.60e-08	**0.796**	490V	0	IV_EXTREME_SLOPE
#24	W5-S1-2025	**0.592**	4.40	**0.355**	316.8	**0.371**	1.98e-06	-6.66e-11	**0.955**	195V	1	PINHOLES:1 IV_LIMITED
#25	W8-S5-2025	**0.592**	4.53	**0.336**	301.6	**0.429**	3.79e-06	-2.65e-09	**0.891**	195V	0	IV_LIMITED
#26	W4-S3-2025	**0.574**	5.47	**0.197**	293.3	**0.460**	1.60e-06	2.79e-09	**0.966**	195V	0	IV_LIMITED
#28	W6-S5-2025	**0.572**	4.86	**0.287**	323.6	**0.346**	2.00e-06	3.71e-09	**0.950**	490V	0	–
#29	W11-S1-2025	**0.559**	5.20	**0.237**	310.0	**0.397**	1.86e-06	-4.00e-12	**0.959**	490V	1	PINHOLES:1
#30	W2-S1-2025	**0.557**	5.47	**0.198**	299.4	**0.437**	1.64e-06	1.60e-09	**0.965**	195V	1	PINHOLES:1 IV_LIMITED
#31	W11-S4-2025	**0.545**	4.90	**0.281**	356.1	**0.223**	1.54e-06	0.00e+00	**0.970**	490V	0	–

Plans for JLab trip

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- ***Overall goal***: end-to-end testing of entire SVT detector using the new vacuum flange, repaired COBs, & radiation tolerant C03 FEBs

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- Planning to do some hardware work as part of this trip
- ***Overall goal***: end-to-end testing of entire SVT detector using the new vacuum flange, repaired COBs, & radiation tolerant C03 FEBs
- Major tasks for a successful trip:
  - Establish basic DAQ setup (network boot both COBs)
  - Extract SVT detector from freezer and warm to room temperature
  - Extract and re-assemble FEB cooling with updated C03 FEBs
  - Connect complete readout system: COBs → Flange → FEBs → SVT detector
  - Readout & characterize entire SVT detector

Conclusions

- Hardware needed to rebuild SVT in good shape
- Readout & powering hardware ready to be exercised in this trip:
  - C03 FEB boards → rebuild FEB cooling plate
  - New Data Flange → all channels functional
  - Repaired LV PS → able to power entire SVT
  - Repaired COB → able to readout both top and bottom detectors
- Hybrid (and module) assembly in late stages:
  - Hybrid assembly will be completed by next month
  - Module assembly intentionally planned closer to next run period
- This trip will help us to get a read on the state of SVT and concretely allow us to know which modules need to be replaced

Backup slides

Hybrid stack-up

