SBS DAQ GMn/GeN/GEp

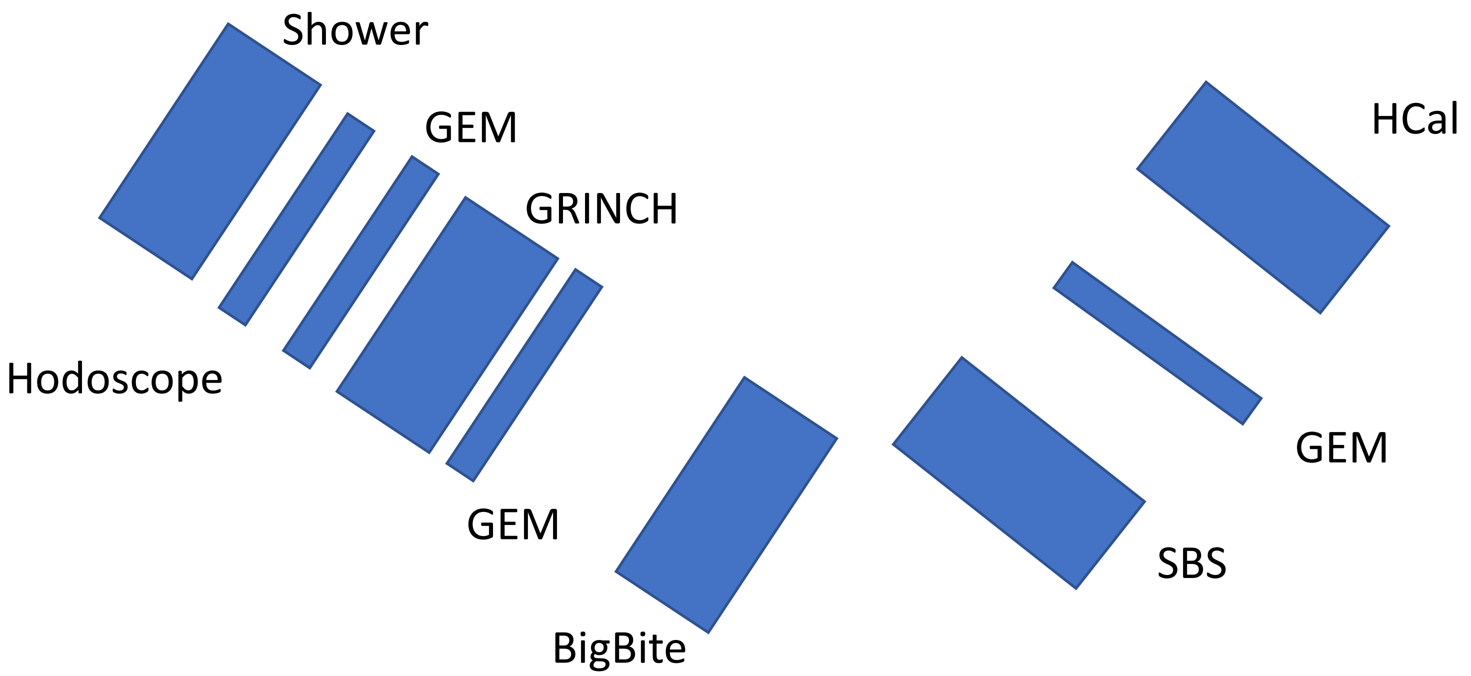
March 4th 2026

SBS collaboration meeting

Alexandre Camsonne

GMn/Gen/Gen RP

BigBite



Bigbite

- Shower
  - 1 VXS crate , 16 FADCs + 2 FADCs for sums + TDC
- Hodoscope
  - 1 VME 64X crate
  - 2 CAEN V1190
  - 4 FADC for calibration
- GRINCH
  - 1 VXS crate
  - 6 VETROCs
  - 4 FADC

- GEMs
  - 3 VXS crates with VTP readout
  - Optical to VXS adapter on hand
  - 3 crates : 1 BigBite 2 for SBS
  - VTP firmware done
  - CODA VTP readout on going
  - 22 MPDs = 6 fibers

HCal

- 288 channels
- 2 VXS crates
- 18 + 1 FADC
- 4 F1 TDC (1 spare)

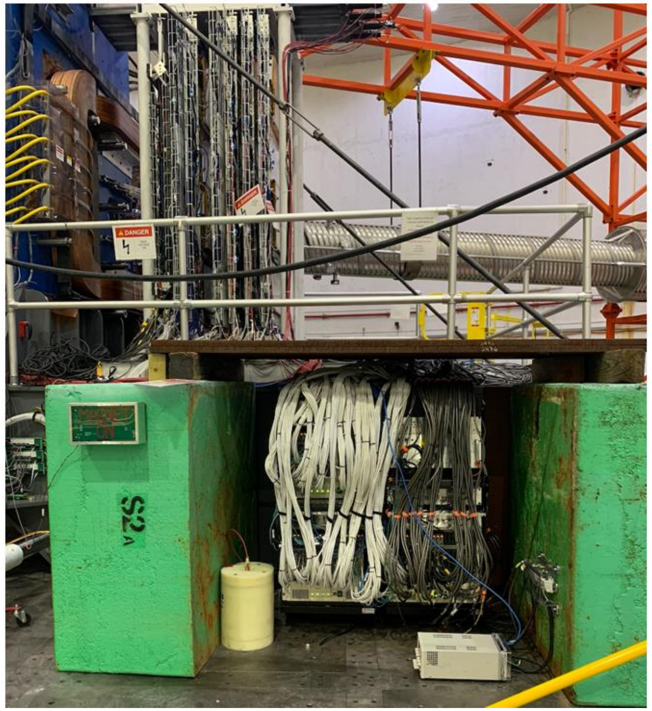
- VTP readout

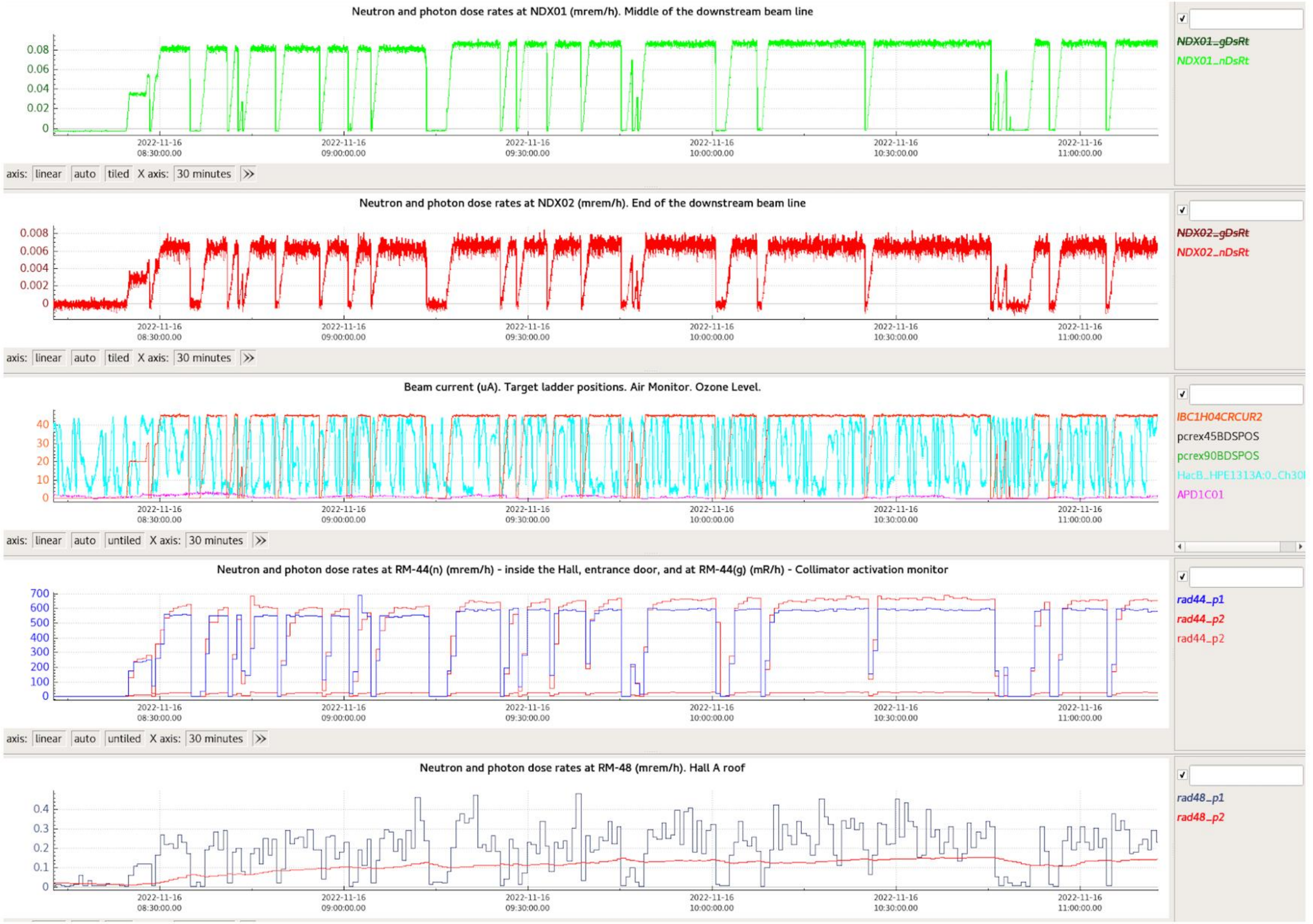
Radiation at the SBS bunker

80 mrem/hr at 40 uA beam
(100 mrem/hr at same current in BB bunker)

Maximum in GMn, sbs-14, 180 mrem/hr at 10 uA

250 mg/cm^2 material in beamline
-> x9 in GEp





GMn, GEn, GEn RP

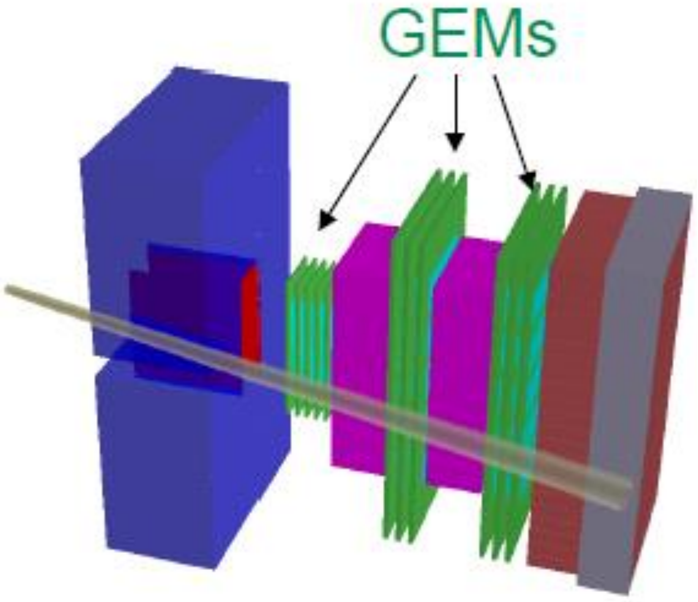
- GMn
  - 1 st experiment
  - Lots of debugging at beginning with new system with CODA3 (TI-TS connection)
  - Inefficiency of HCAL F1 TDC (suggest full replay on farm while experiment running) – Thresholds were too low on discriminators
  - GEM worked but many DAQ crashes : implemented many diagnostics in end of run to locate APV errors
  - Up to 700 MB/s with one event recorder
- GEnII
  - Power balancing issue between phases in bunker
  - 2nd experiment : BB GEMs pretty stable
  - Implementation DAQ with 3 streams give 2 GB/s capability all software adapted to use the future
  - Tried implementation of SBS GEMs in parasitic
    - 1st INFN chamber had issues with electronics, not clear why (maybe magnetic field)
    - SBS GEMs fairly unstable so where often taken out from readout – Most likely not as much time for debugging as BigBite and large number
    - GUI for rebooting GEMs
  - Inefficiency on HCAL trigger side

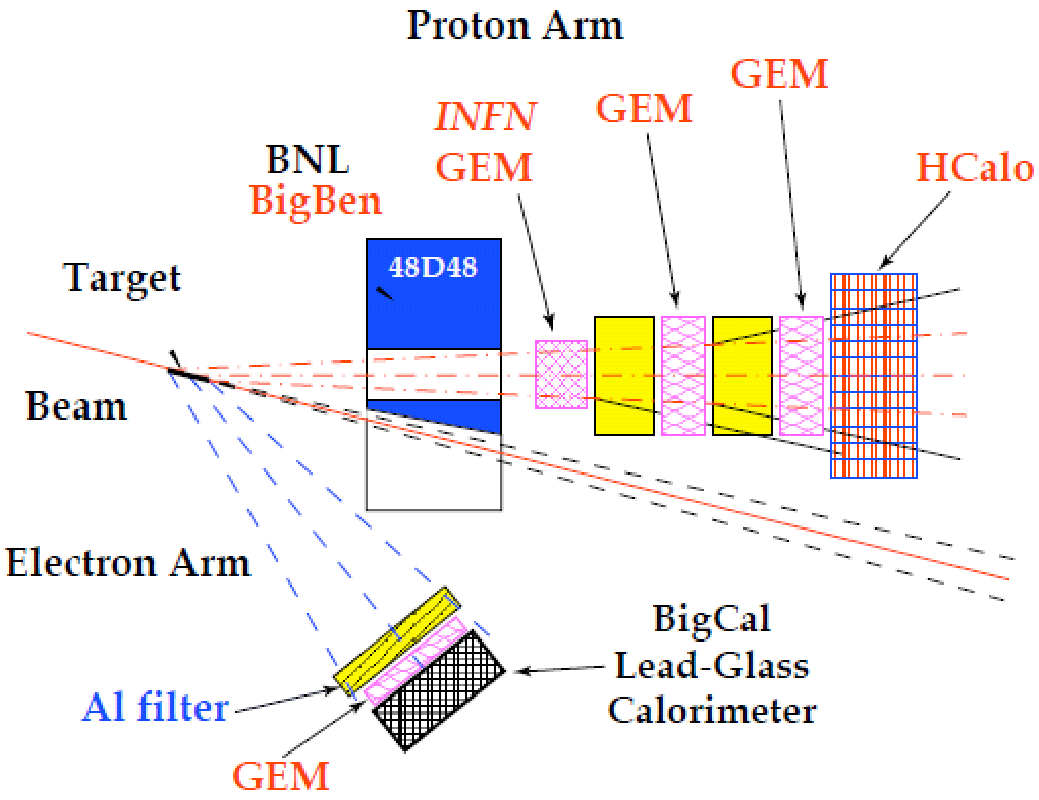
GMn, GEn, GEn RP

- Gen RP
  - Issue with GEMs at beginning : tried to run DAQ with lower threshold
  - Trigger inefficiencies mainly because of HCAL HV too low (some block noisy at higher)
  - Trgger rate maxed out at 4 KHz : bottle neck VTP first layer (spread out layers across VTP crates)
  - DAQ unstable above 4 KHz and with radiator
    - Suspect single event upsets in MPD : will reload firmware of MPDs at each run
    - Additionnal shielding might be helpful (might be more stable with hydrogen than deuterium target)
    - Some MPD optical transceiver might have suffered from radiation damage
  - SBS arm more stable during Gen RP more time for cabling and debugging
  - 2 or 3 down time for LV connector melting

Conclusion : DAQ working – Gen RP with large number of channels – Many GEM DAQ hang-ups

SuperBigbite Spectrometer
Focal Plane Polarimeter setup for GEp



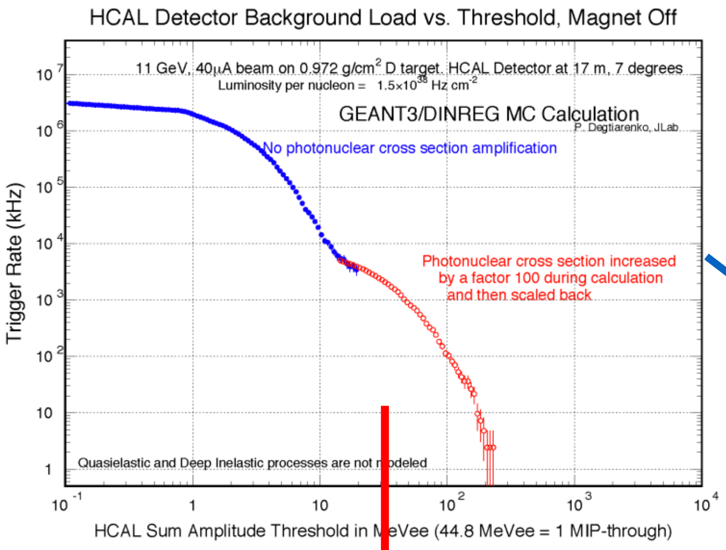


Calorimeter Rates

(CDR section 5.1.7) Most demanding

HCAL

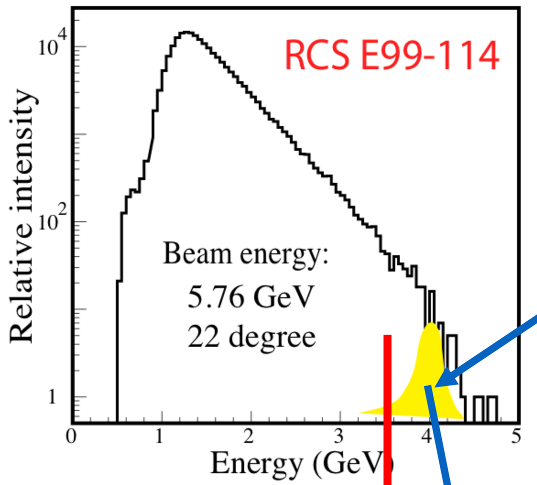
Hadron rate estimate using SLAC & DESY data, Wiser code:
w/4.5 GeV threshold: ≈ 1.5 MHz



Background rate vs. cut on deposited energy (MC studies in progress)

ECAL

From Hall A Real Compton Scattering experiment

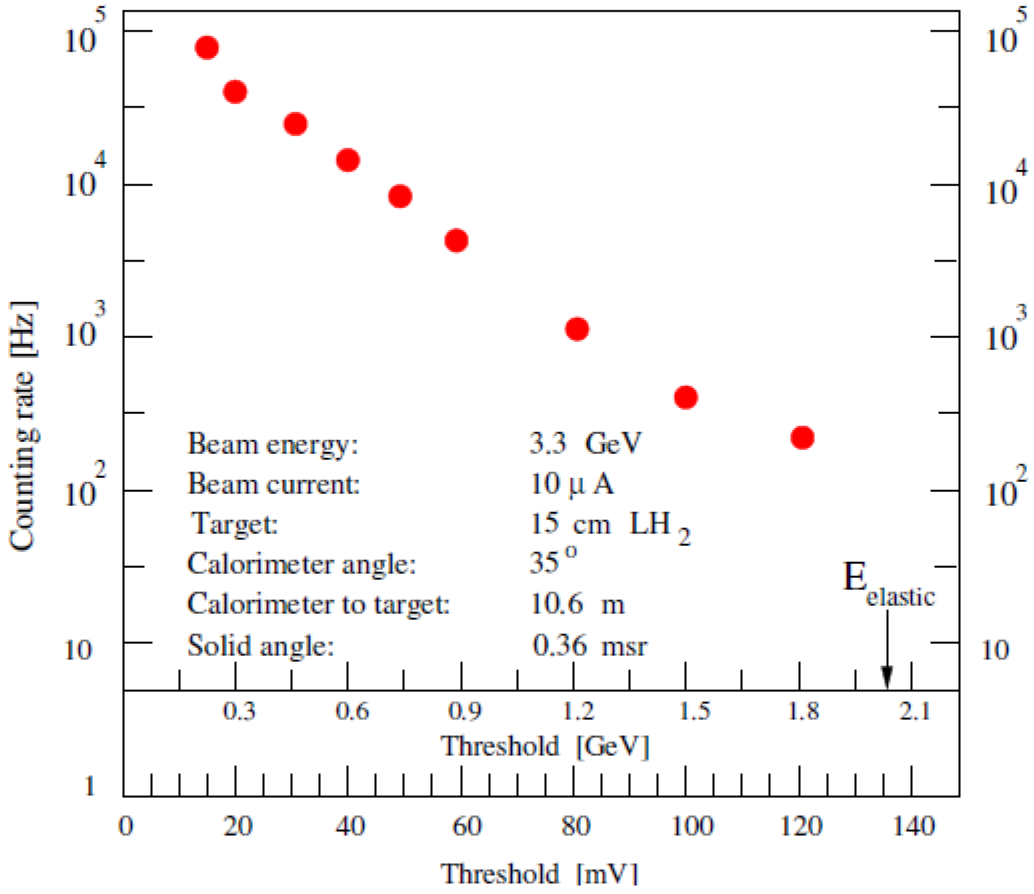


NB: Good resolution ≈ 16%/√E

Electron rate estimate w/2.5 GeV threshold (73% of E_{elas}): ≈ 200 kHz

≈ 9 kHz coincidence rate w/ 30 ns window

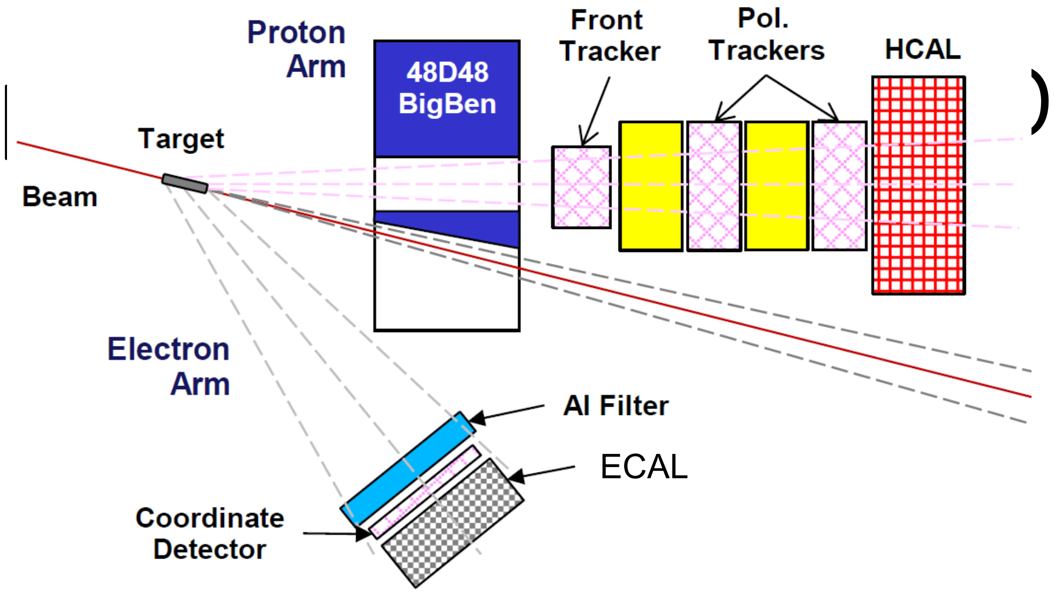
Electromagnetic calorimeter BigCal readout



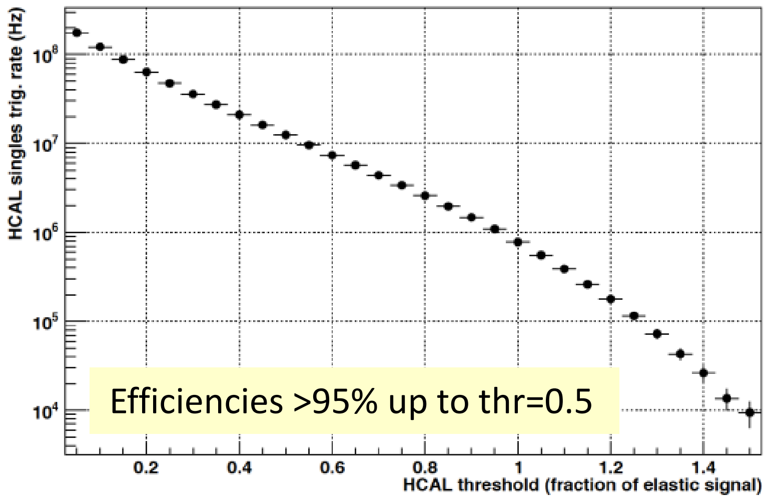
E_{thr}/E_{max} %	50	73	85	90
Rate, kHz	1400	203	60	38

2.5 sigma cut
Calorimeter BigCal resolution
16 %/sqrt E

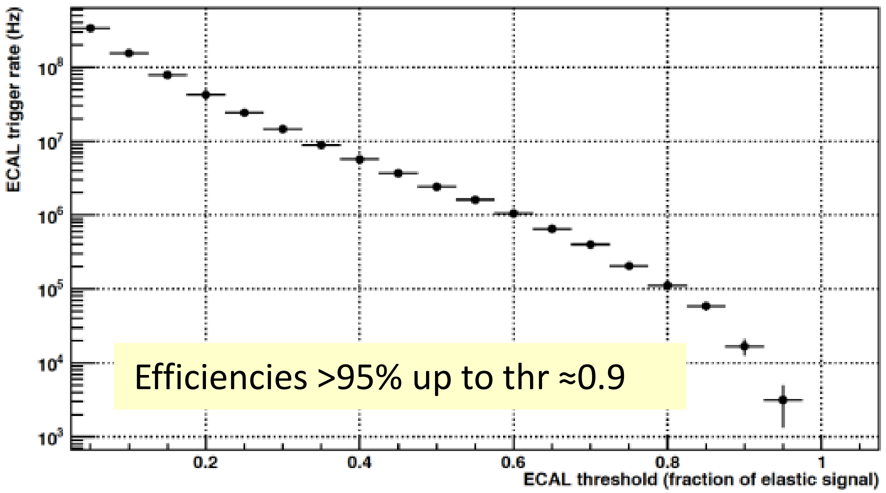
GE



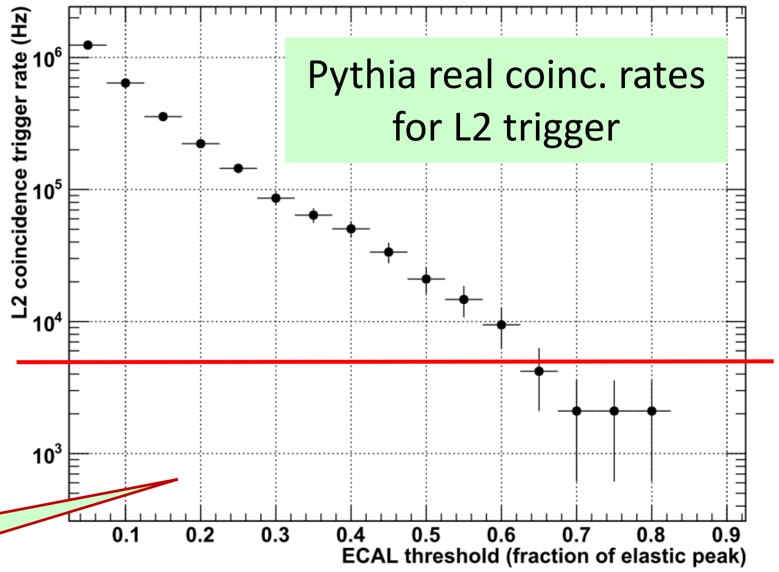
HCAL Singles: SLAC+DESY data in Wiser Code



ECAL Singles: from tuned GEANT4

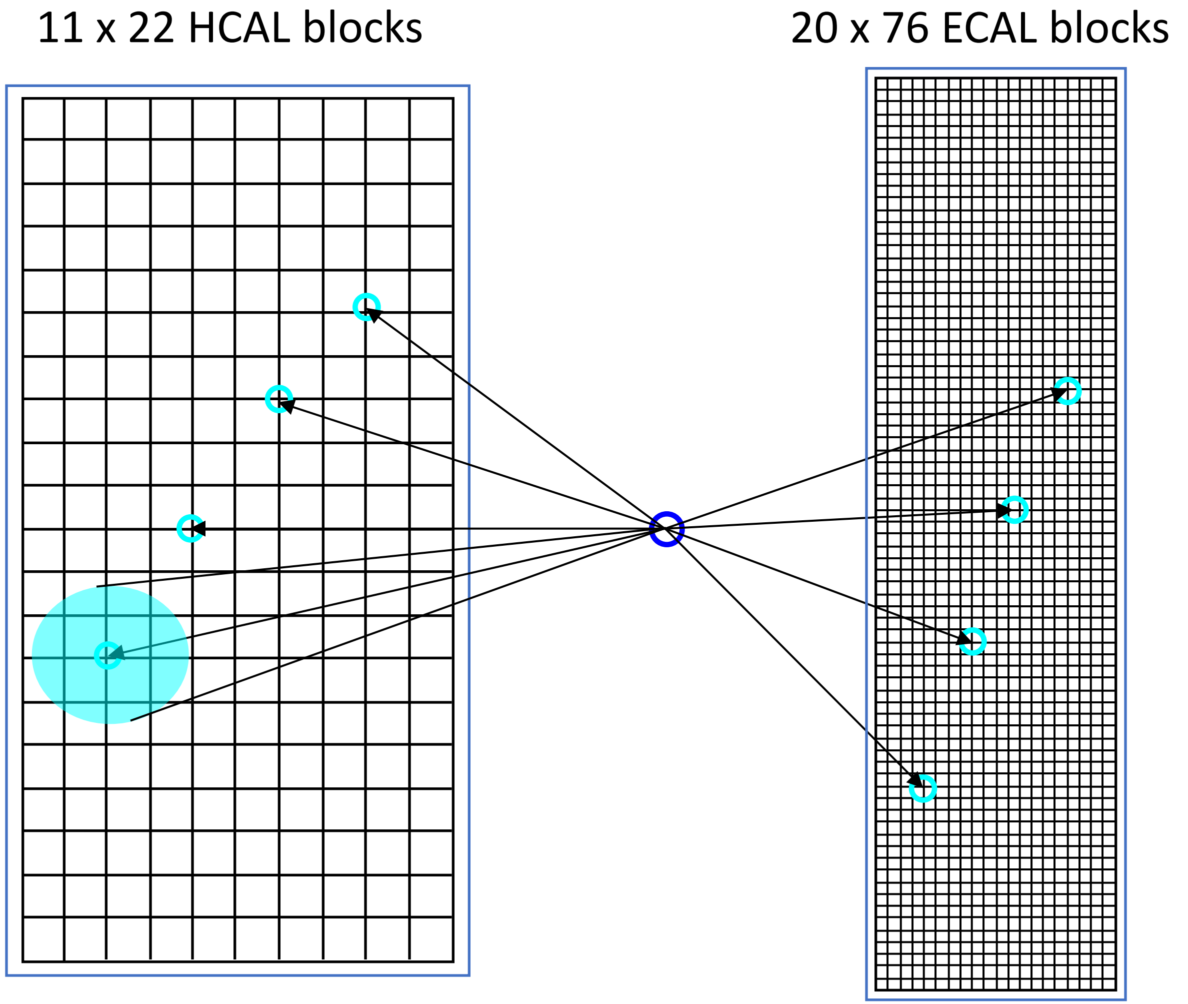


HCAL threshold = 50% of elastic peak



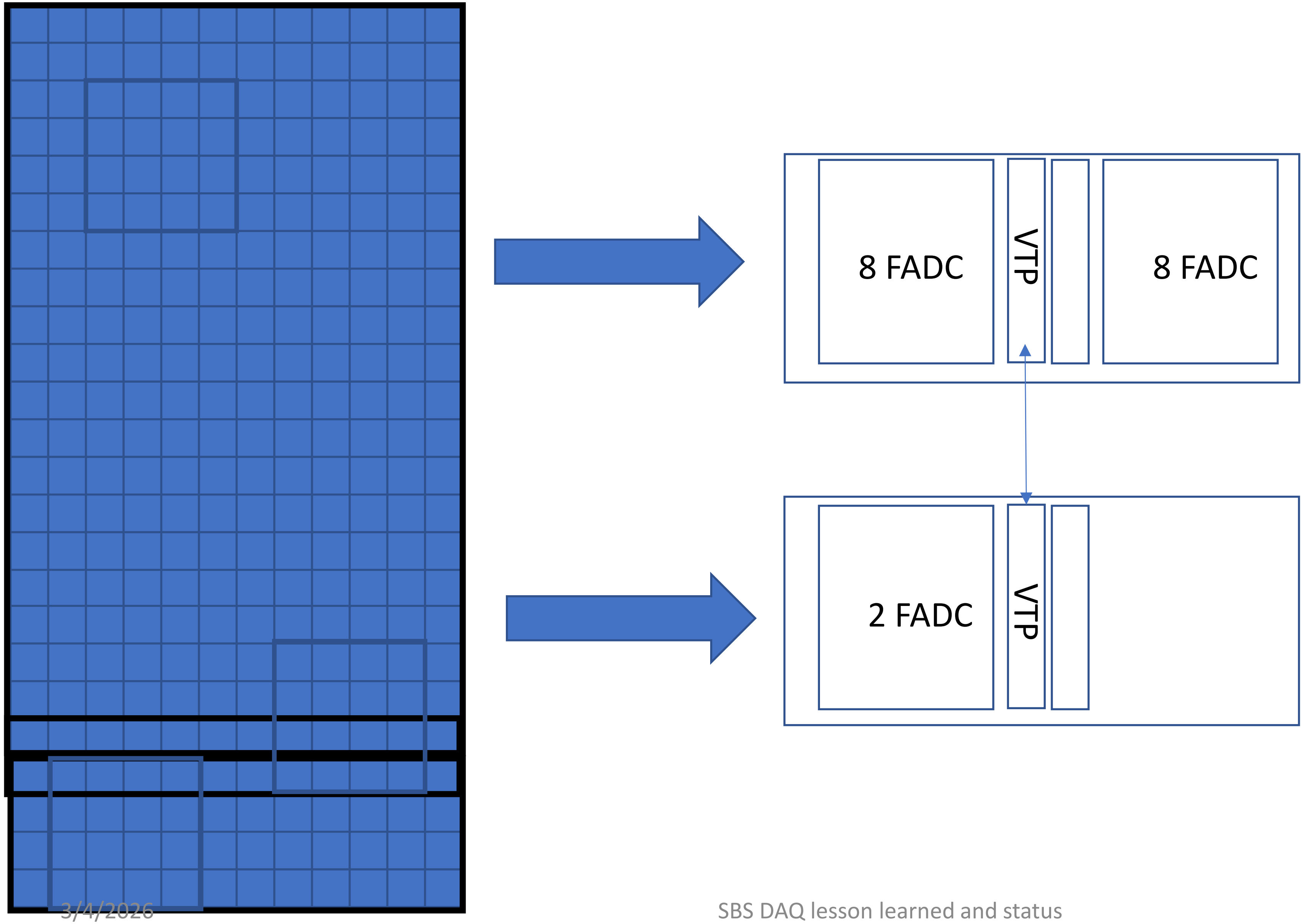
Expected Coincidence Rate (L2) up to **5 kHz** (including accidentals)

e’-p Kinematic Correlation



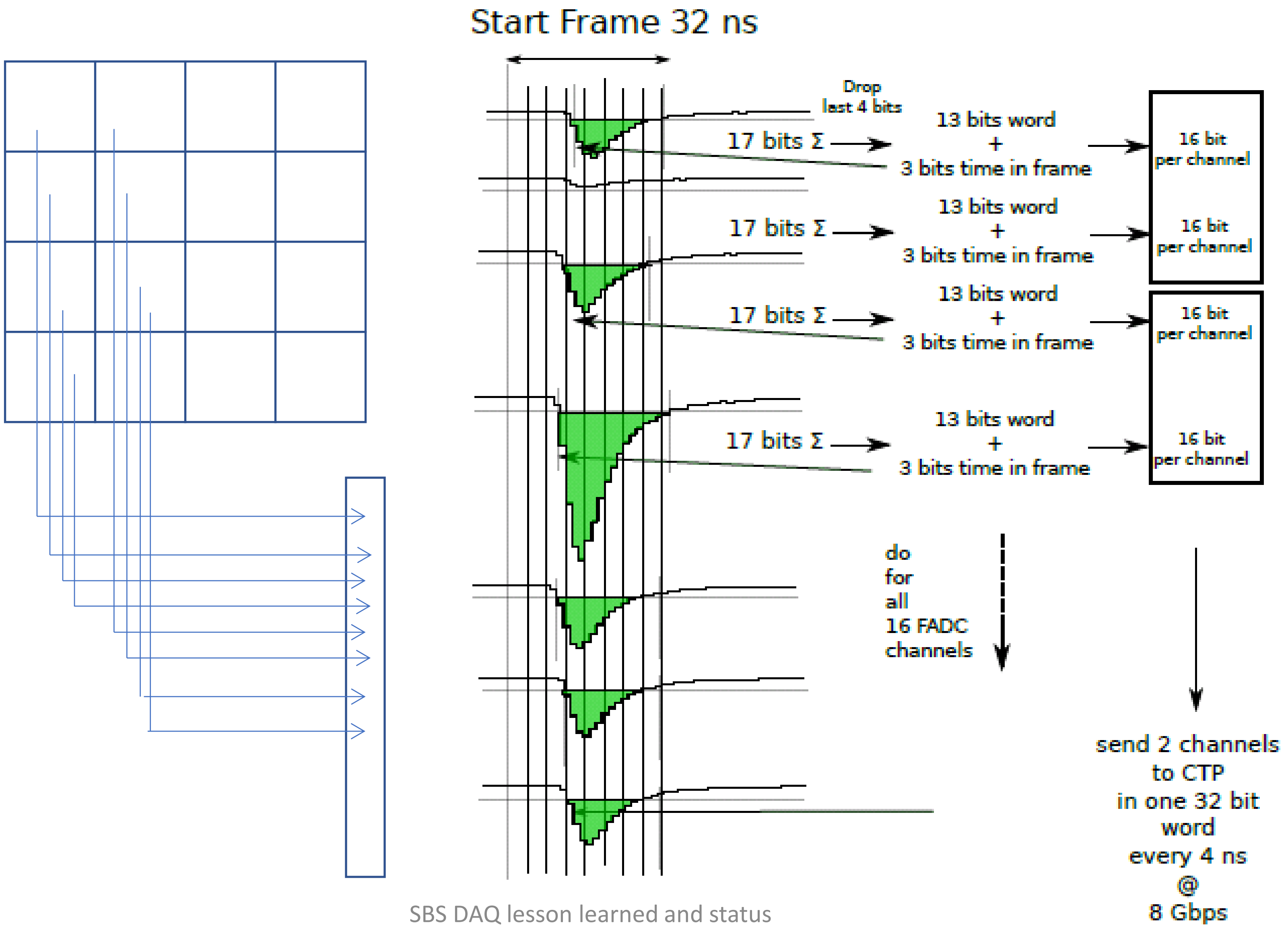
Using geometric correlations from elastic kinematic one can reduce final rate by a factor of 5 and tracker data by at least a factor of 3

SBS HCAL



- 12 x 24 = 288 blocks
- 2 VXS crates
- 18 FADCs
- 2 VTP
- Transfer blocks at crate interface through 10 Gbps optical link

Clustering HPS like



SBS HCAL trigger status

- Single crate 4 x 4 blocks cluster trigger implemented

- Clustering on two crates to be implemented

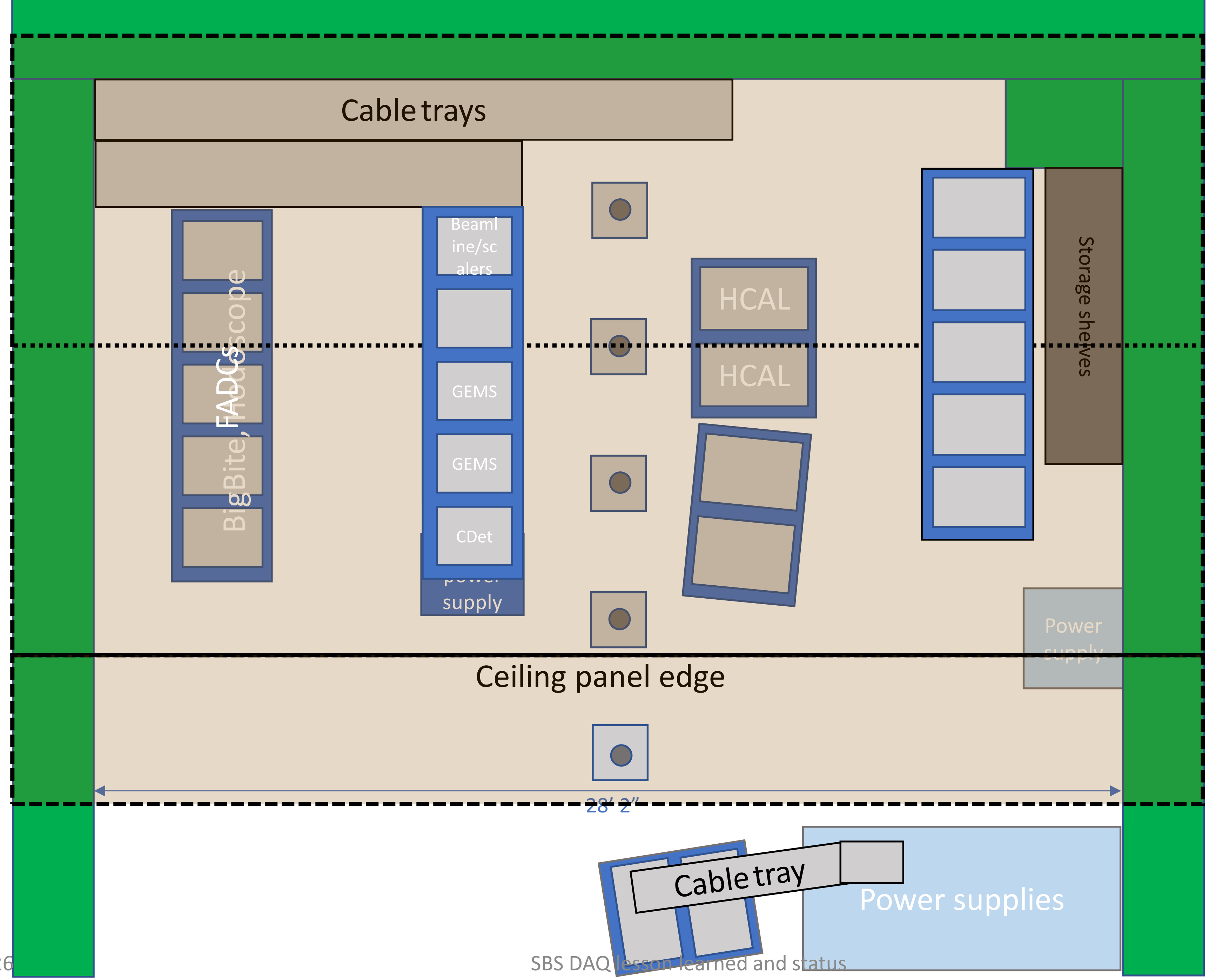
- Same algorithm for ECAL with 3x3 or 5x5 sums trigger

Ecal readout

- 1656 calorimeter channels
  - Bigbite : 256 channels
  - 1400 channels
    - FADC250 : 1400 /16 = 88 modules = 6 VXS crates

  - Order for physics electronics :
    - 104 FADCs
    - 32 VTPs
    - 32 VXS crates
  - Should cover Gep5 Ecal even with NPS running

DAQ Bunker in Hall



Current layout

Reconfiguration steps

1. Move storage shelves and install 5 racks for HV in their place. Install HV crates and modules in racks (Summer 2023)
2. Move HCal racks slightly to give more room.
3. De-install BigBite and Hodoscope electronics, HV and cabling (April 2024)
4. Consolidate GEM electronics in two racks (April 2024)
5. Move central racks and power supply outward to allow 3 racks for CDET
6. Install Patch Panels, VME crates for FADCs and Trigger supervisor and install scaler crate.
7. Run cables and connect everything up.
8. Add ceiling panels?

1656 Channels VME FADCs

CDet

2352 channels of scintillating fiber

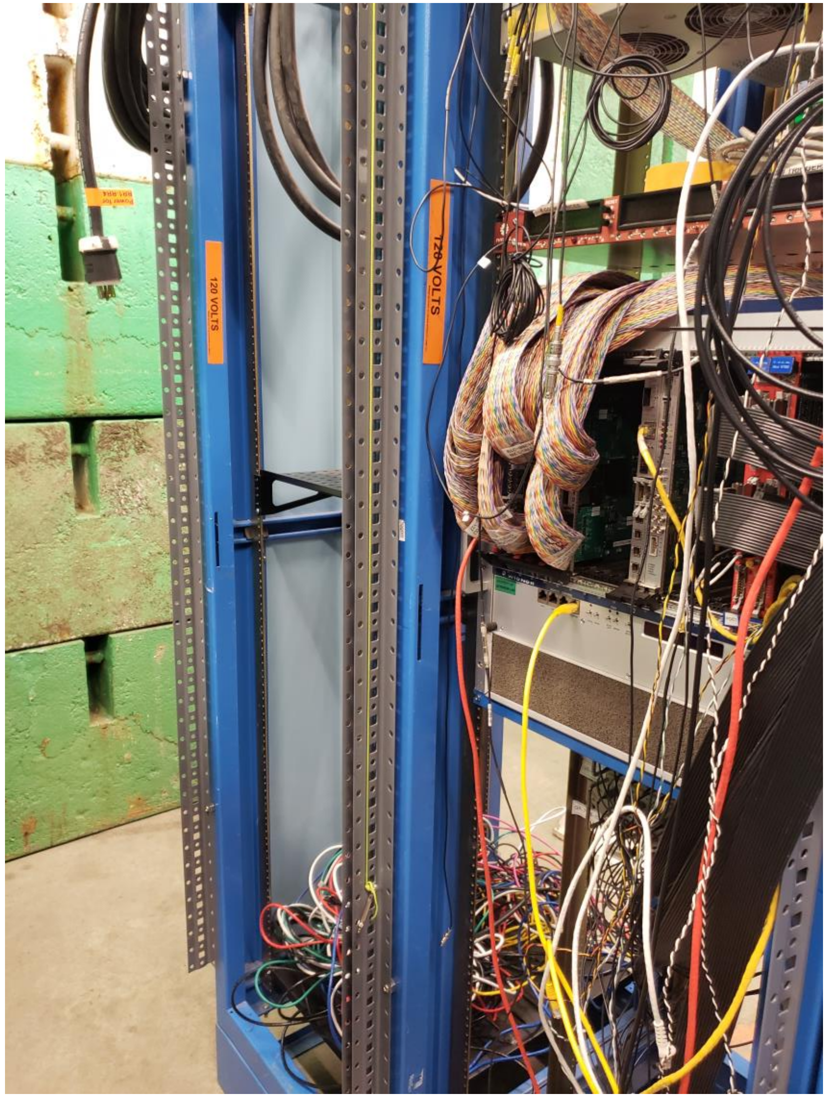
Readout with VETROC in one VXS crate

192 channels per VETROC, 128 in front and 64 in back

Use 13 VETROCs modules

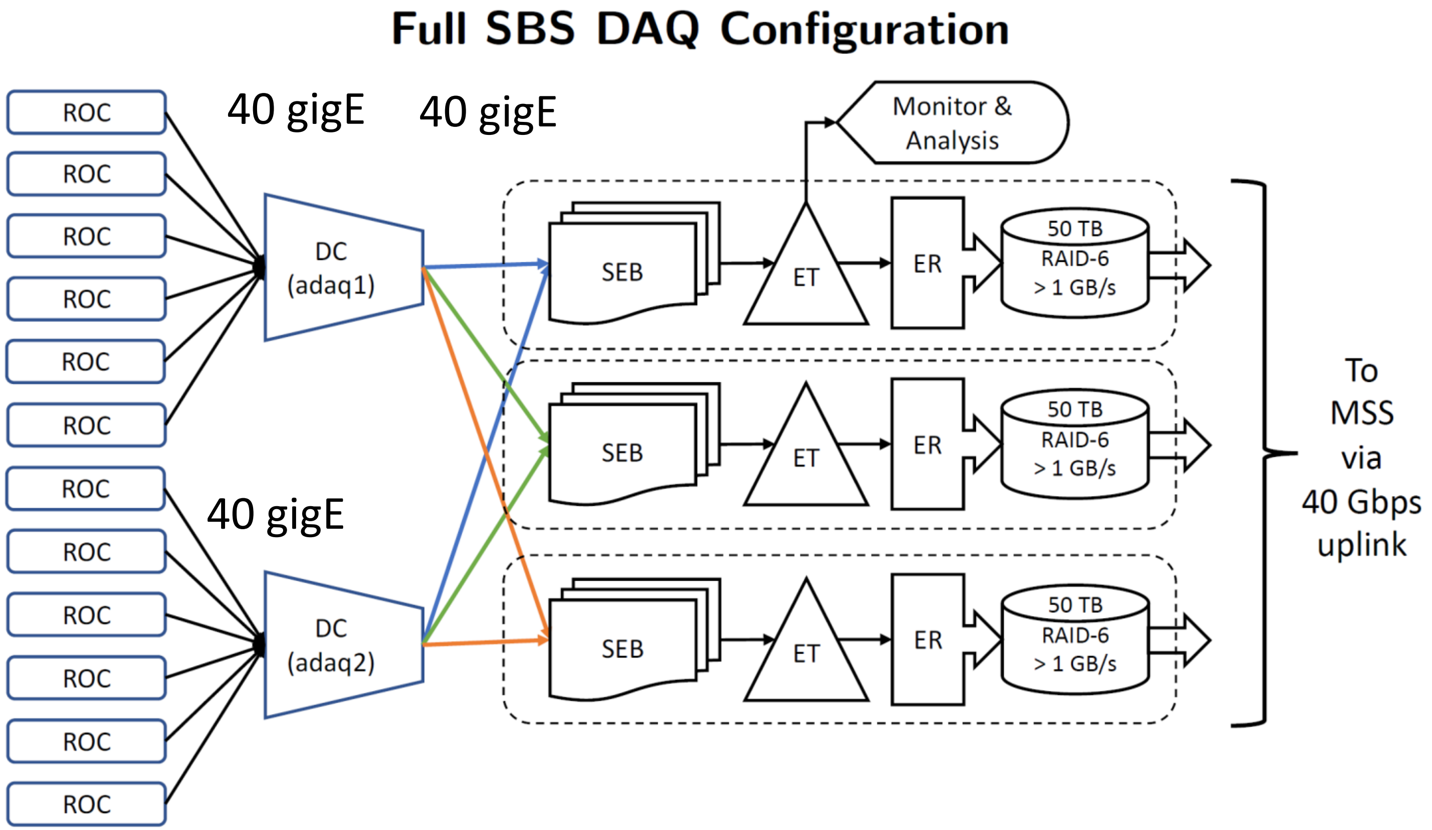
VETROC already used for GRINCH during GMn and GeN

Crate setup in LHRS



CODA3

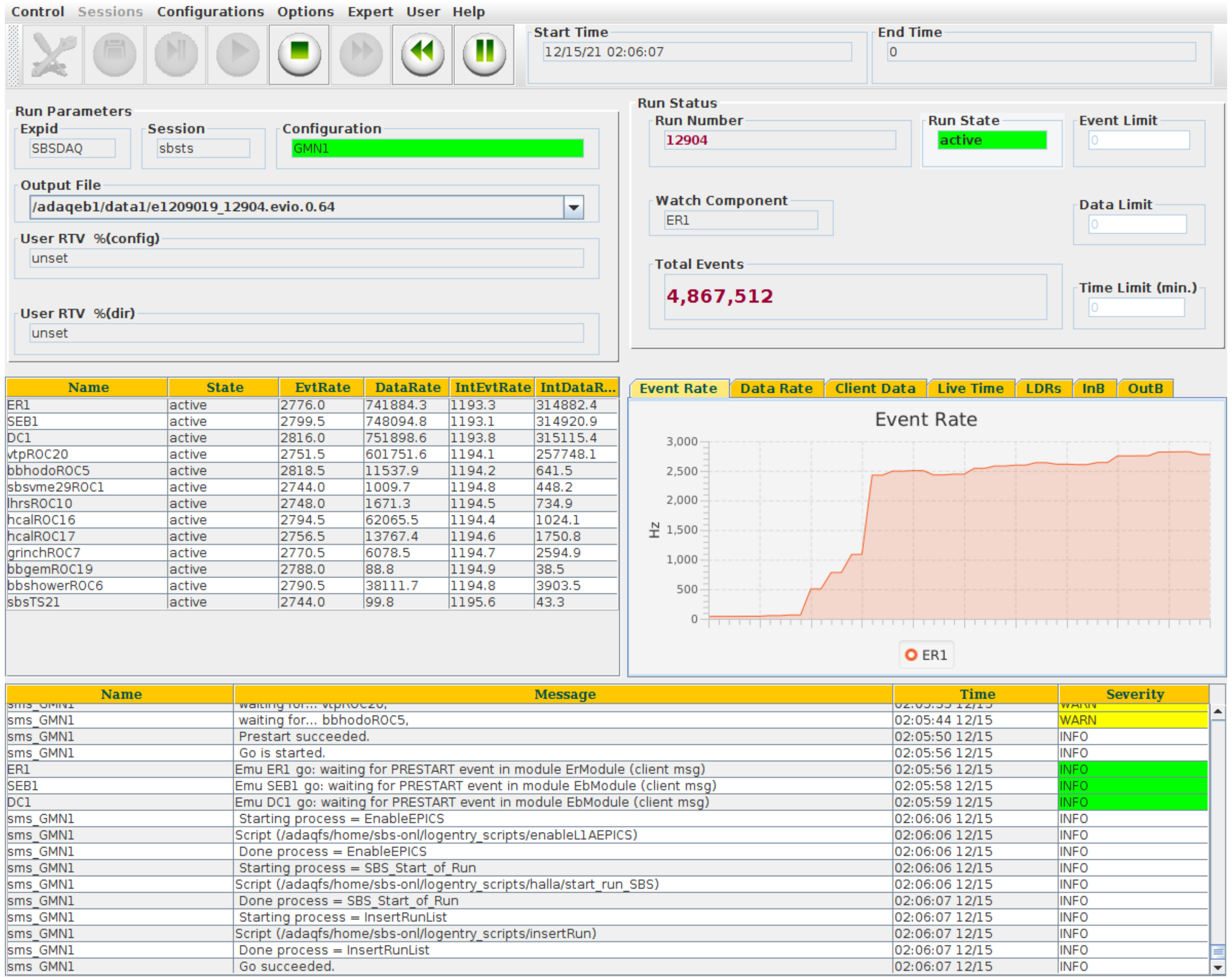
- TS/TI Fiber based
- Support for VTP
- Support for multiple stream



Production data during GMn

- Typical rate around 3 kHz
- 90% livetime with one event builder
- 600 MB/s from BigBite GEM
- 240 MB/s HCAL, shower FADCs
- 800 MB/s to disk

- Up to 2.4 GB/s using 3 event builder



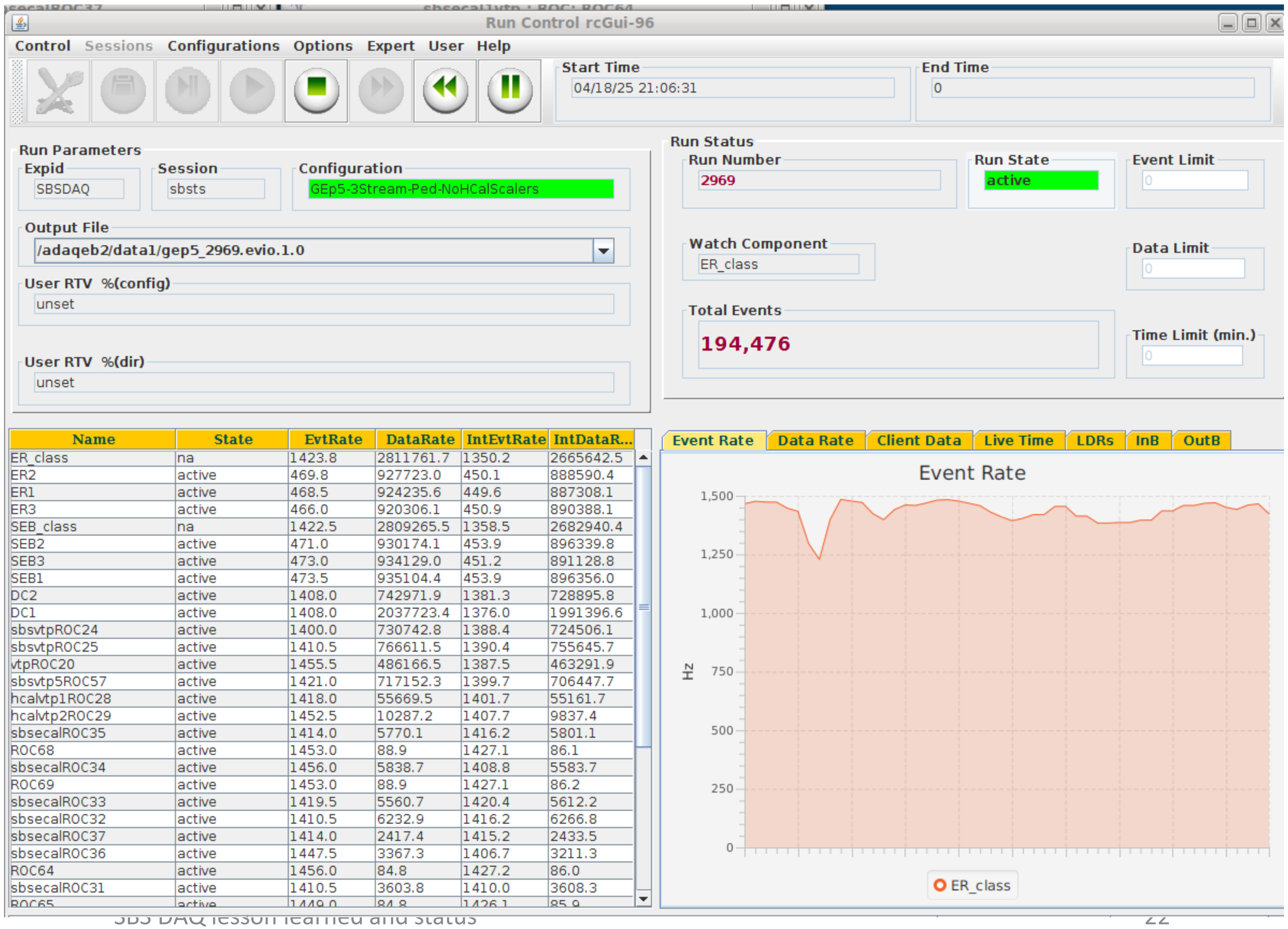
GEp5 configuration

- Pedestal with pulser
- Maximum data rate 2.8 GB/s (reached EB/ER limit)
- Can do more with additional computers and VTP

- MPD to VTP bottlenect at 5 KHz

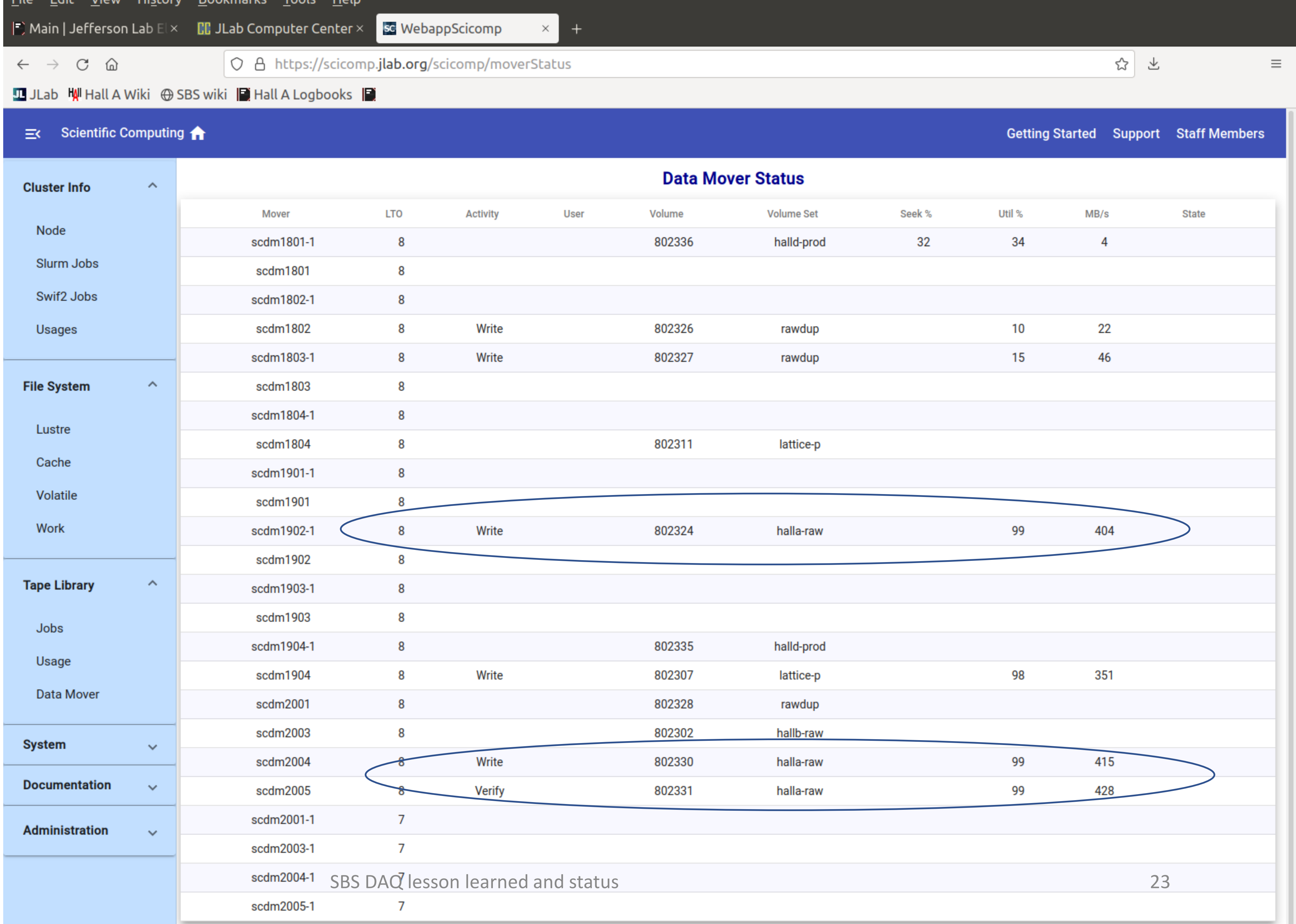
- New VME MPD design up to 10 KHz

- New MPD with 10gigE – should reach APV rate limit – 47 KHz with 6 samples



Silo performance

- Achieved 800 MB/s continuous
- Peak at 2GB/s with
  5 tape drives to catch up the high data rate during GEp



Mover	LTO	Activity	User	Volume	Volume Set	Seek %	Util %	MB/s	State
scdm1801-1	8			802336	halld-prod	32	34	4	
scdm1801	8								
scdm1802-1	8								
scdm1802	8	Write		802326	rawdup		10	22	
scdm1803-1	8	Write		802327	rawdup		15	46	
scdm1803	8								
scdm1804-1	8								
scdm1804	8			802311	lattice-p				
scdm1901-1	8								
scdm1901	8								
scdm1902-1	8	Write		802324	halla-raw		99	404	
scdm1902	8								
scdm1903-1	8								
scdm1903	8								
scdm1904-1	8			802335	halld-prod				
scdm1904	8	Write		802307	lattice-p		98	351	
scdm2001	8			802328	rawdup				
scdm2003	8			802302	hallb-raw				
scdm2004	8	Write		802330	halla-raw		99	415	
scdm2005	8	Verify		802331	halla-raw		99	428	
scdm2001-1	7								
scdm2003-1	7								
scdm2004-1	7								
scdm2005-1	7								

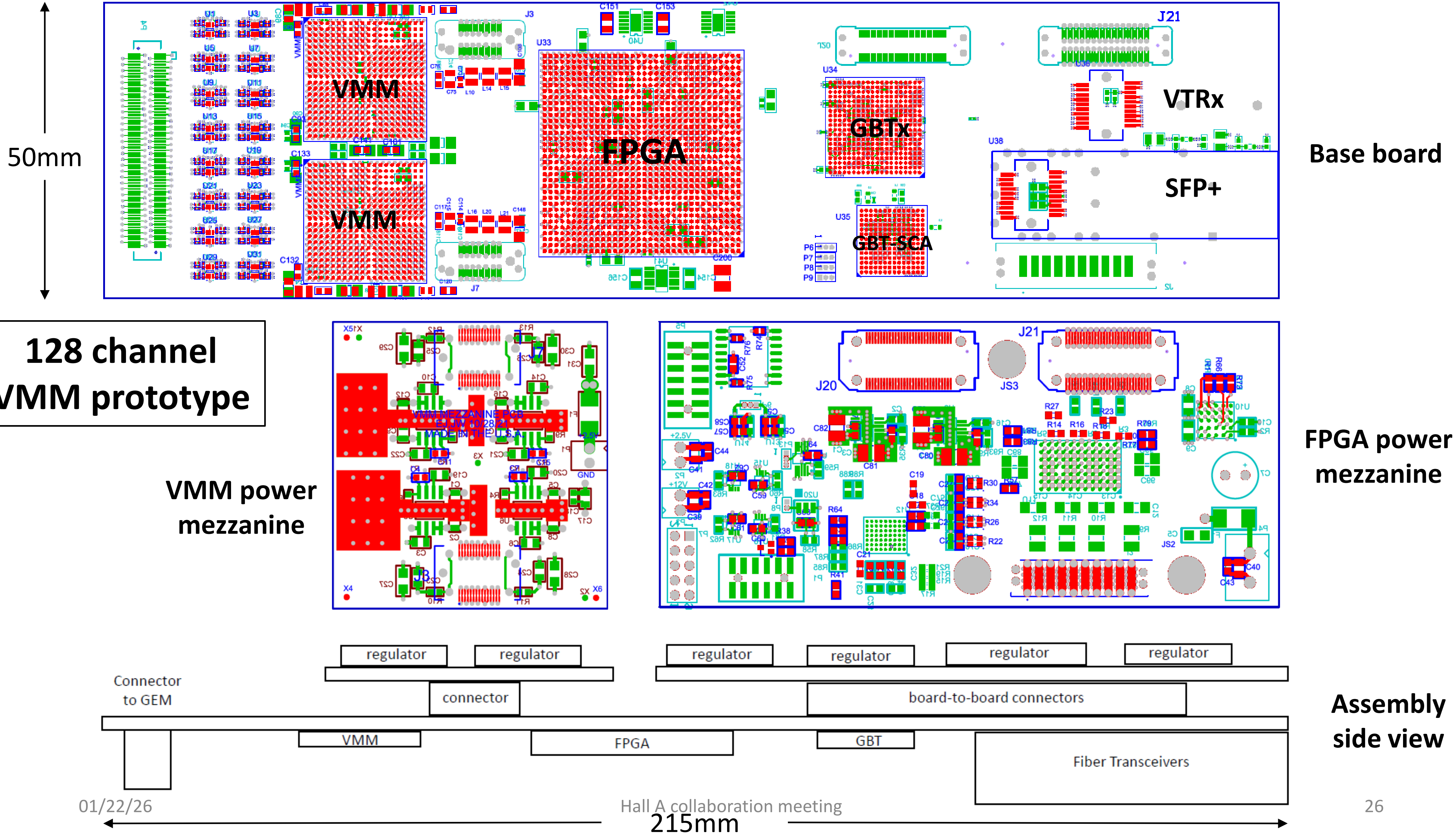
GEp5

- Developements
  - FADC trigger calorimeter trigger
    - Cluster trigger
    - Geometrical matching Ecal – Hcal
  - 3 VTP crates for GEM readout
  - Up to 2 GB/s with 3 event recorder
  - Data taking around 1 GB/s
- Issues
  - GEM occupancy high : ran at 20 uA
  - GEMs DAQ hang-ups : maybe radiation upsets and some sparking
  - Data rate : decide to forego geometrical matching to avoid down time
  - 5 KHz limit from old MPD was an issue with Ecal rate due to low threshold and calibration
  - Silo marginal at 2 GB/s (more arms, data reduction)
- Future improvement
  - New chip for GEM readout with faster shaping
  - Faster MPD
  - Increase granularity for GEMs
  - Online data reduction

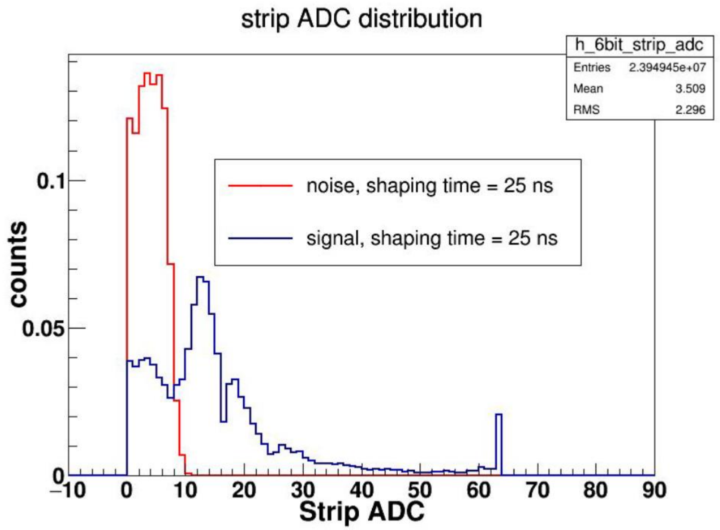
VMM test

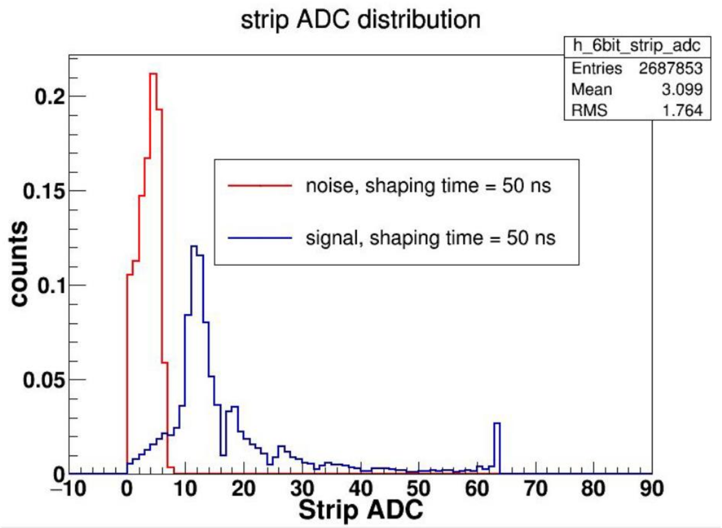
- Build 6 SoLID prototype boards
- Evaluation board : can look at data with detector small subset of channels
  - Issue with external trigger but waiting for new firmware
  - Can check pedestal width
  - Signal to noise with detector with source and cosmics
  - Look at direct readout signals for 12 channels of detector

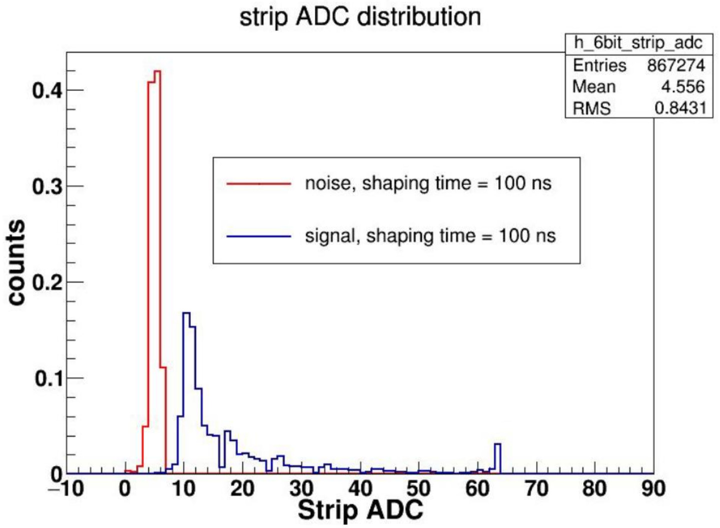
128 channel VMM prototype

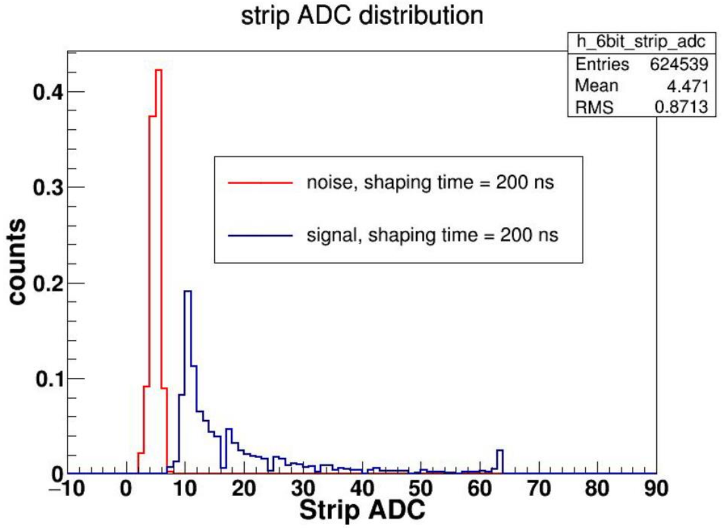


Noise 6 bit 16mV/fC Sr90







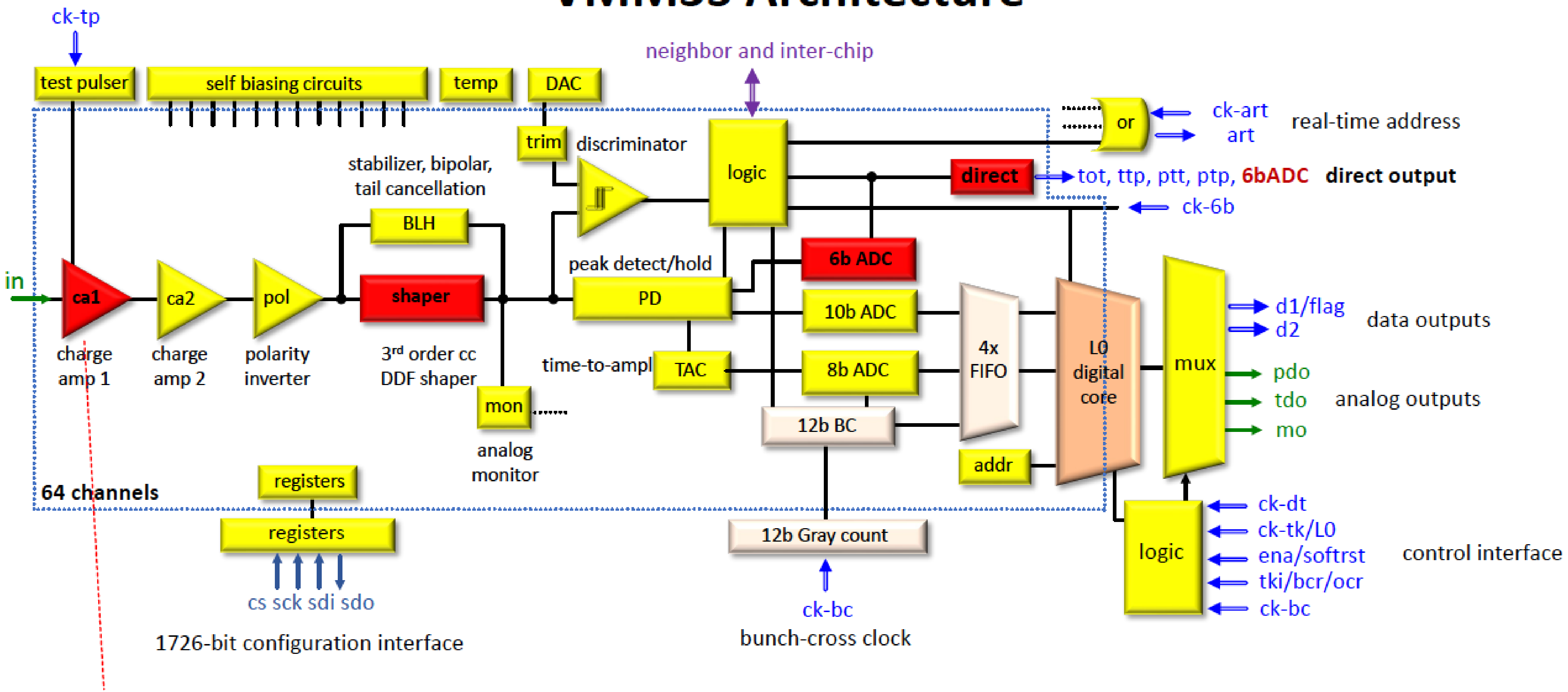


- Amplitude for MIP not change much
- Pedestal width dependent on peaking time

Conclusion VMM testing so far

- 90 ns dead time in 6 bit mode
- Some noise seen in prototype
- Noise larger with decreasing integration time
- MIP a bit low in dynamic range of 6 bit prototype
- Implementing 10 bit to cross compare with evaluation board
- 250 ns for 10 bit mode
- Investigating new VMM with high gains for GEM and uRWell (~500 K$) Hall B interested, need to reach out to SRS community
- Need implement Rad Hard DC DC converter and lpGBT radiation hard readout

VMM3S Architecture



SoLID MPGDs will initially operate with charges up to ~100,000e⁻:

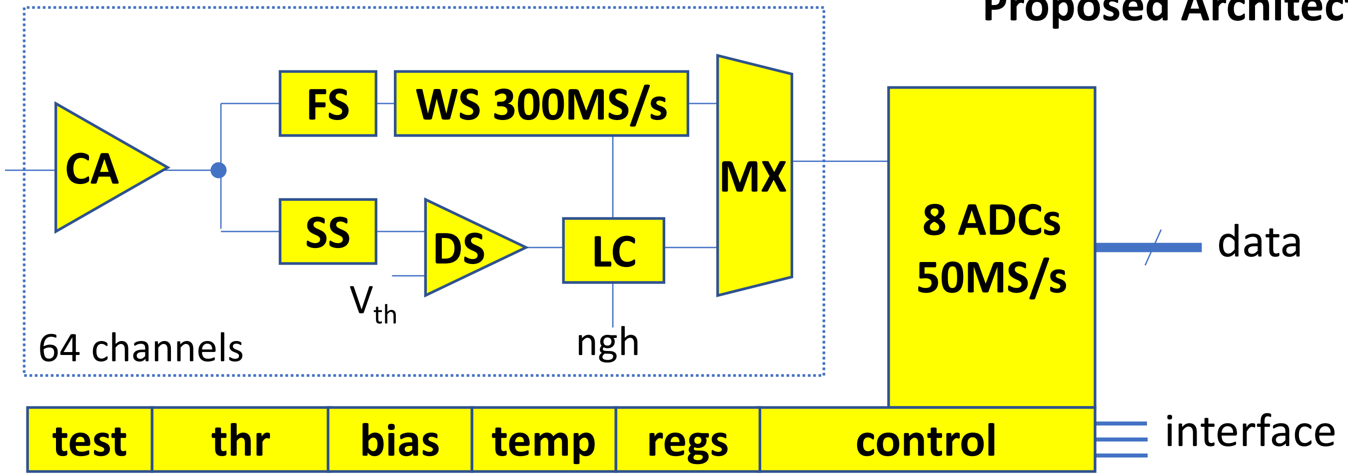
- will integrate a higher gain setting 64mV/fC
- will deliver ENC ~1,500e⁻ @ 50pF, 25ns (ADC contribution ~450e⁻)

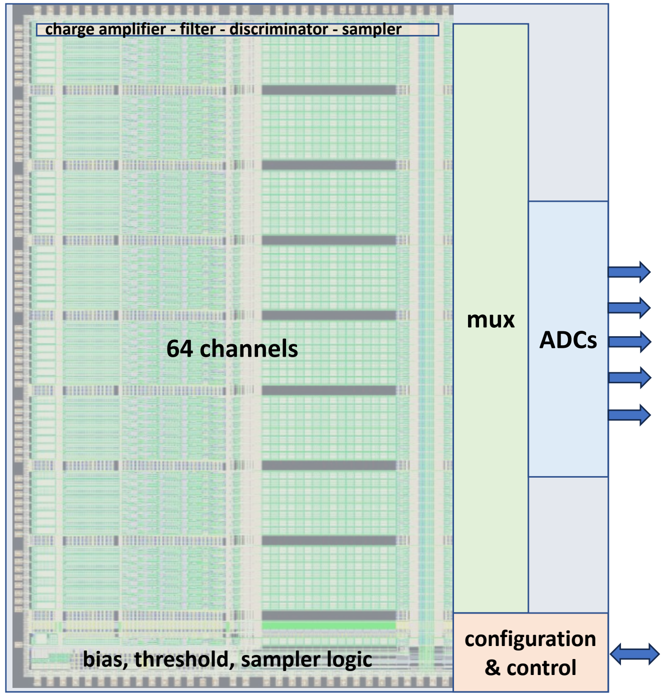
New potential dedicated ASIC

- High luminosity running need to run
- Pile-up and deadtime can be significant

- Dedicated chip
  - Optimized gain and dynamic range
  - Optimize shaping time for high rate operation : from 50 ns to 25 ns or better
  - Zero dead time
  - High speed links to allow streaming

Proposed Architecture





CA: charge amplifier
- optimized for 50-200pF
- programmable gain 25fC to 250fC

FS: fast shaper
- programmable 5-20ns

SS: slow shaper
- for discrimination (zero suppression)
- programmable 20-100ns

DS: discriminator
- trimmable per channel
- external trigger option

WS: waveform sampler
- 128 sampling cells (127 effective)
- continuous sampling until trigger
- 300MS/s → ~ 400ns waveform
- programmable pre-post trigger samples

LC: local control logic
- internal or external trigger
- neighbor (sub-threshold) logic

ADCs
- 8 operating at 10-bit 100MS/s
- waveform conversion time ~ 2.5µs

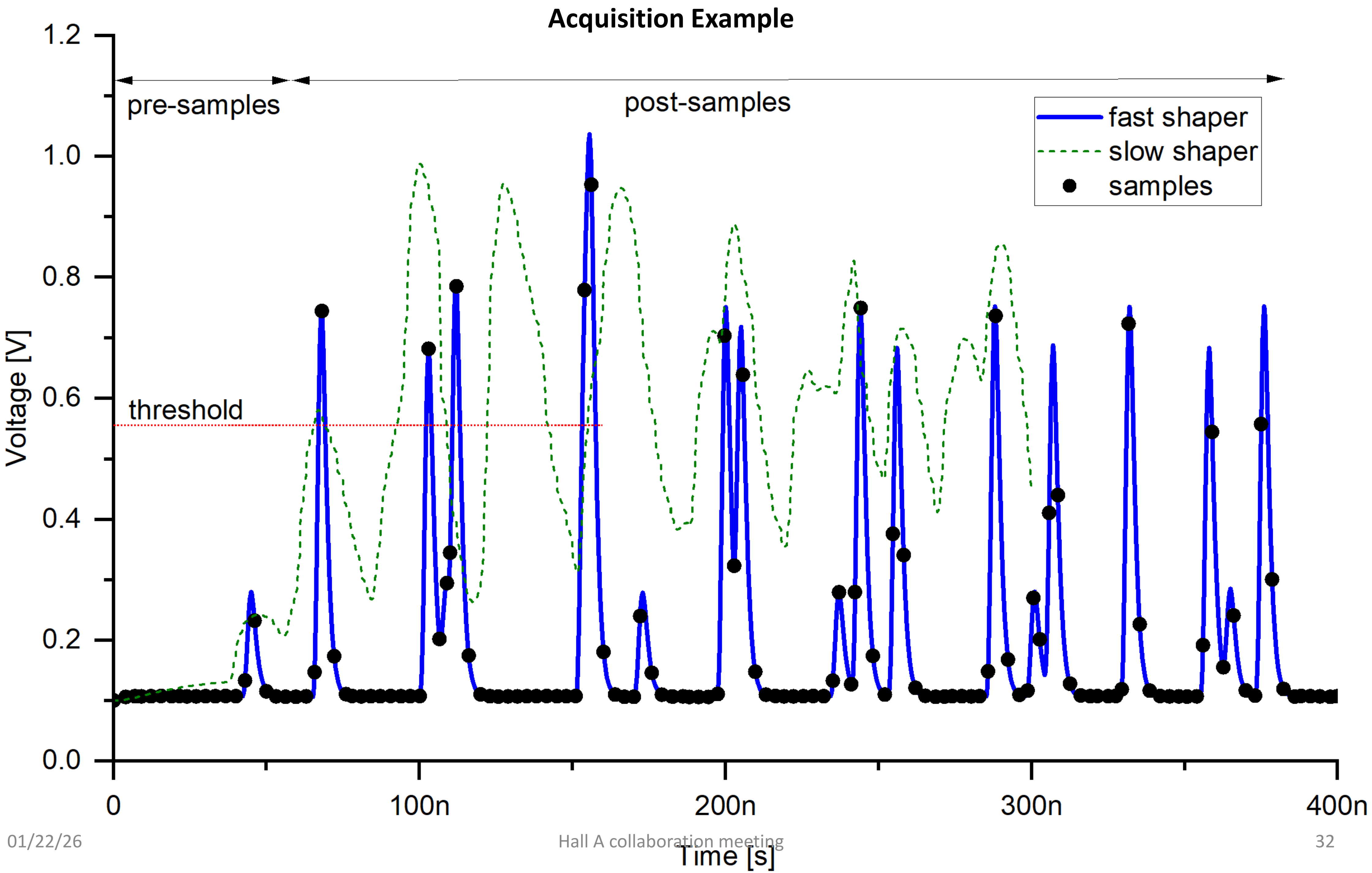
Data
- channel, trigger, 127 samples = 1,280 bits per waveform
- up to 8 waveforms with sub-threshold neighbors = 10,240 bits
- up to 8 SLVS outputs operating in DDR at ~ 500MS/s
- conversion/readout time (dead time) ~ 2.5µs per event
- maximum event rate ~ 330kHz
- maximum data rate ~ 4Gb/s

Architecture
- event-driven analog/digital with acquisition/readout
- SEU tolerant register and logic
- DSP-ready

Power, Size, Technology, Schedule
- power consumption below 3mW/channel
- anticipated die size ~ 6x8 mm²
- technology TSMC 65nm 1.2V
- development time ~ 24 months (1st proto in 12 months)

Design
- charge amplifier, shapers and samplers based on verified architectures
- ADCs from collaborative effort
- first prototype design time
  - ~ 12-13 months plus ADCs
  - ADC can be parallel effort
- second prototype design time
  - ~ 4-5 months

Key Features
- power-efficient analog zero-suppression
- efficient data generation and transfer
- highly flexible, highly programmable


Acquisition Example
pre-samples
post-samples
threshold
fast shaper
slow shaper
samples
Voltage [V]
Time [s]
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0
100n
200n
300n
400n

Conclusion

- SBS program complete with many DAQ developments
  - First use of CODA3 in Hall A
  - Optical readout from MPD (one issue of noise discovered in board limiting max rate to 5 KHz instead of 10 KHz)
  - VTP readout for GEMs and FADC
  - Calorimeter trigger with calorimeter matching
- DAQ worked ok for experiment with done time and some detector issues should aimed for full replay of data during experiment to catch subtle effects
- Major down time from GEMs
  - Not clear reason
    - GEM sparks
    - Radiation upsets
- Luminosity limited by GEM occupancy
  - Doubling channels would help
  - Better chip (VMM or sampling chip) with faster shaping time
- Online background suppression would reduce data footpring