Streaming Readout PET

LDRD Q1 Report – January 21, 2026

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JSA

Q1 Accomplished Goals

A) Detector prototype development

- Front end boards in hand and scalers tested
- 3D printed housings, cooling, and assembly
- Synch distribution board received, in progress

B) SRO data processing system development

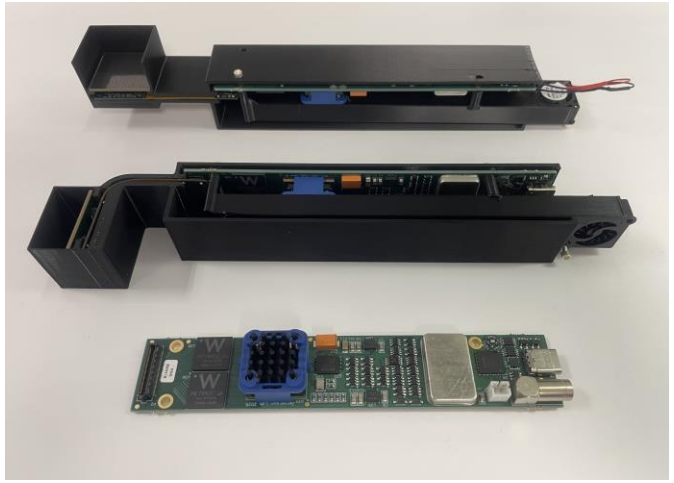
- Successfully factorized analysis into ERSAP
- Multi-node horizontal parallelization added
- Delayed synch distribution board procurement has <u>delayed Q1 SRO system integration step</u>

C) Broader scope project work

- 2nd provisional patent filed, IEEE RT Abstract
- Contract P.R. placed with UMAB PET facility
- Trained to use NERSC Spin and Perlmutter

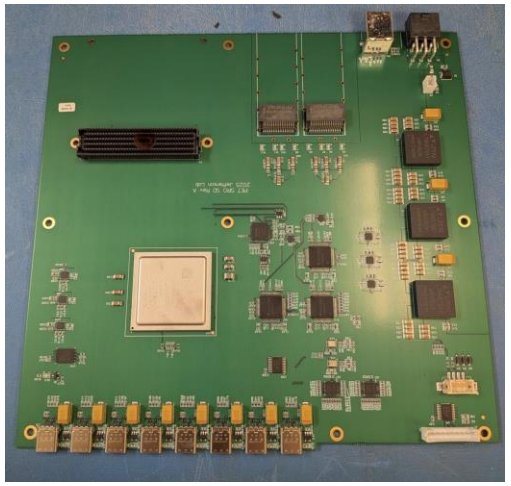
<u>ISP Challenge: EPSCI's Mike Goodrich</u>
<u>Solution: NERSC support and re-allocate FTE as AmSC settles</u>

FY 2025 Starting Points



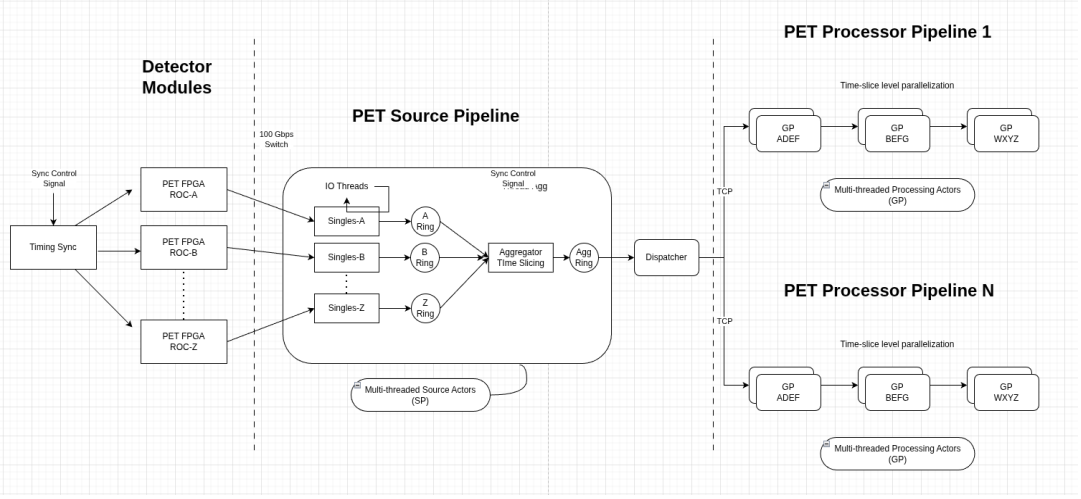
- Front-end boards in-hand and testing underway

FY 26 Q1 Implementation Progress



- SD Board in-hand and firmware on-track

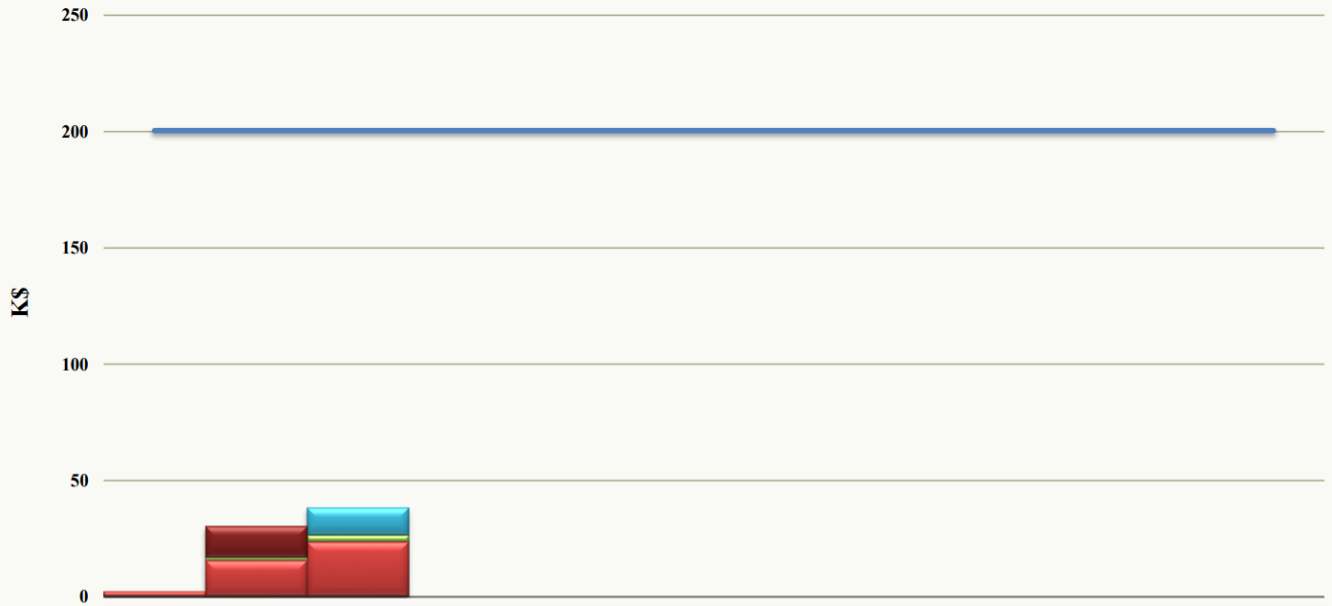
Updated streaming architecture for multi-node horizontal scaling



SPENDING

- **Spending is generally on target** – electronics finalized, software on track, UMAB contract P.R. placed
  1) Labor: Spent ~$24k on labor
  2) Equipment: Spent ~$12k on signal/synchronization distribution board procurement delayed from last year
  3) Travel: Cancelled IEEE meeting attendance, retracted 2 papers, due to government shutdown chaos

SCALABLE STREAMING READOUT DATA ACQUISITION AND ANALYSIS ARCHITECTURE FOR MEDICAL IMAGING: TOWARDS MODULAR HUMAN TOTAL-BODY POSITRON-EMISSION TOMOGRAPHY
C. Clarke (LD2604)
WBS 1.03.LD.018 (Loaded $k)



	Oct-25	Nov-25	Dec-25	Jan-26	Feb-26	Mar-26	Apr-26	May-26	Jun-26	Jul-26	Aug-26	Sep-26
YTD Spending	2	30	38	0	0	0	0	0	0	0	0	0
Pending	0	13	0	0	0	0	0	0	0	0	0	0
Open Obligations	0	0	12	0	0	0	0	0	0	0	0	0
Expenses	0	1	3	0	0	0	0	0	0	0	0	0
Labor	2	15	24	0	0	0	0	0	0	0	0	0
Funding	200	200	200	200	200	200	200	200	200	200	200	200
3-Mo Avg Projection												

BACKUPS

DELIVERABLES

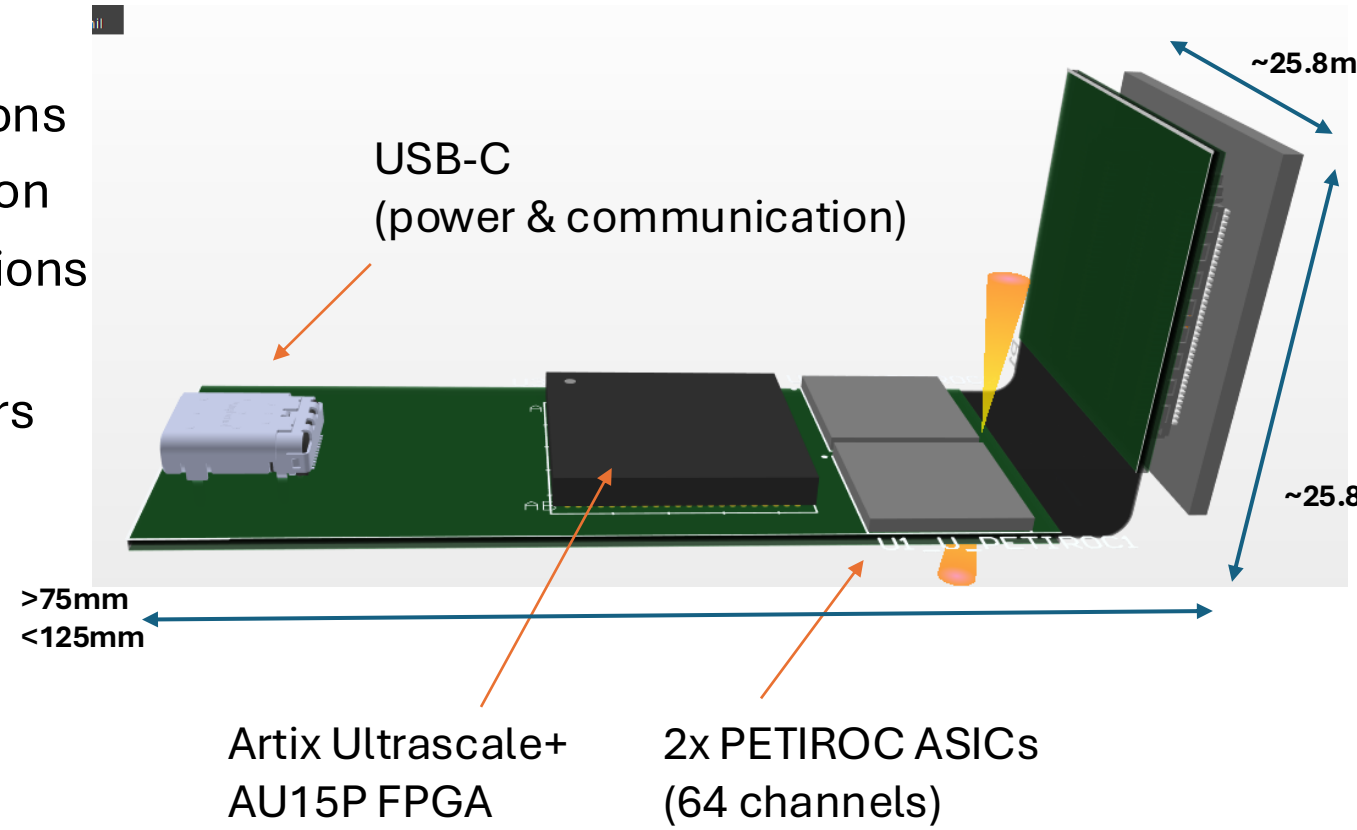
Deliverables – milestones and timeline:

- Three primary aims
  1) Implement ERSAP to existing SRO PET detectors, DAQ, and analysis system in FY 25
  2) Design and build improved version of modular PETIROC ASIC PET detectors in FY 25
  3) Deploy detector array, perform imaging and parallelized scaling tests with distributed computing in FY 26

Year 1			Year 2		
1)	**Implement ERSAP in FY 25:** ☐ (✓) Implement FPGA based PETIROC signal digitization ☐ (✓) Factorize analysis components into ERSAP microservices ☐ (✓) Reproduce old system performance with ERSAP system ☐ (✓) Vertical multi-threaded, horizontal multi-node scaling	**FY 2025:** • Month 3 • Month 6 • Month 9 • Month 12	3)	**Deploy detector array, imaging and parallelized scaling tests in FY 26:** ☐ (✓) Procure and test new detector front-ends ☐ (O) Integrate modular 8-detector array with new SRO system ☐ Verify detector and imaging performance for new system ☐ Deploy the system and perform phantom imaging tests at UMAB ☐ NERSC streaming with JIRIAF control plane ☐ Finalize reports on local and farm streaming scalability tests	**FY 2026:** • Month 3 • Month 3 • Month 6 • Month 6 • Month 9 • Month 12
2)	**Design and build modular PETIROC ASIC PET detectors in FY 25:** ☐ (✓) Optimize FPGA multi-detector readout firmware ☐ (✓) Optimize detector power supply and readout cabling ☐ (✓) Design and order new PETIROC modular detector PCBs ☐ (✓) Get electronics parts, build, and test 8 new detectors	**FY 2025:** • Month 3 • Month 3 • Month 6 • Month 12			

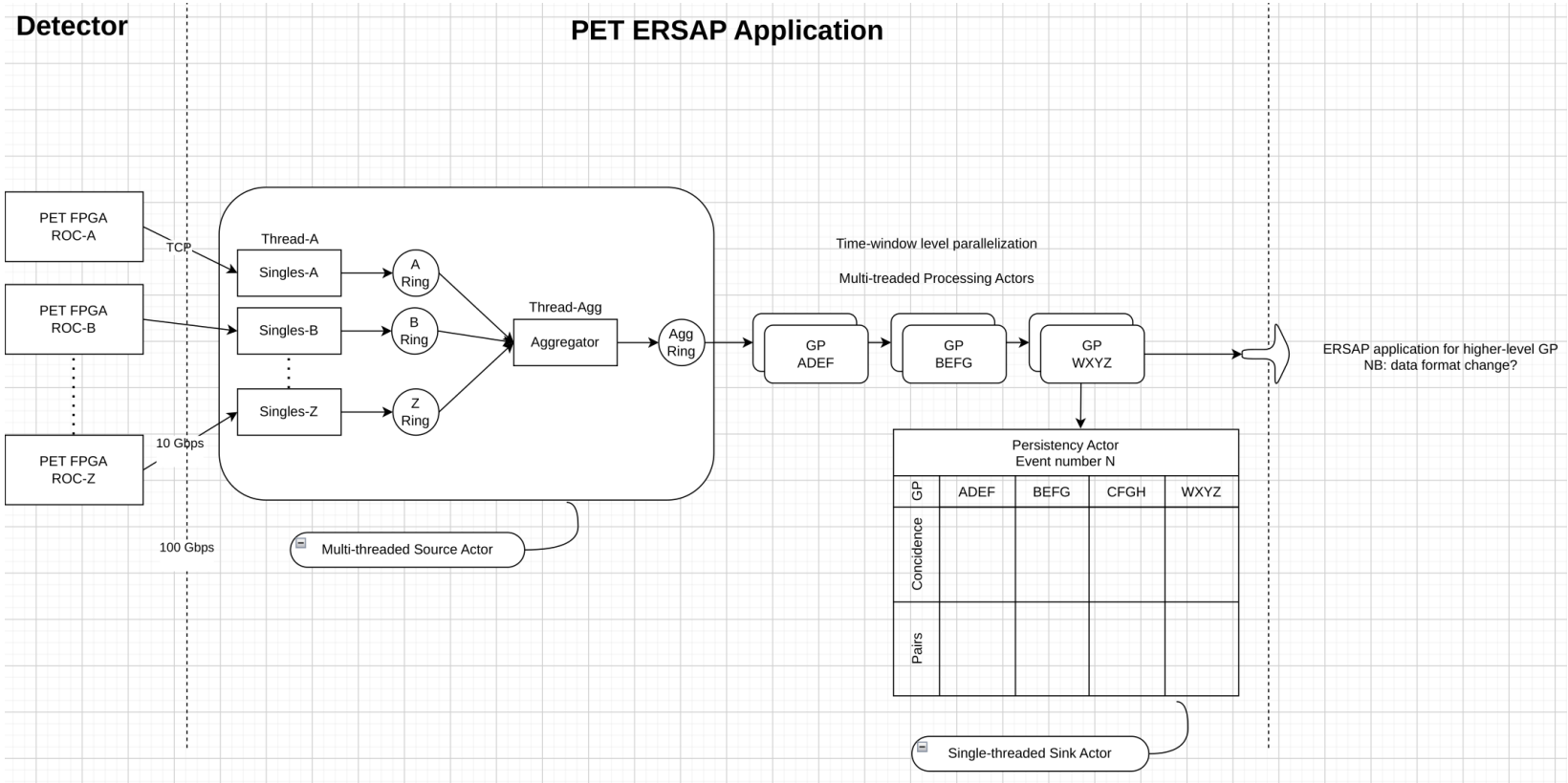
Detector Prototype Development

- Designed concept for v2.0 front end layout
  - Modular detector design
  - Aiming for 4-side buttable
  - SiPM and scintillator separated
  - Flex cable permits multiple orientations
  - & permits thermal and optical isolation
  - USB-C connector simplifies connections
  - Communication board (not shown) synchronizes and powers all detectors



SRO Platform Development

- Explored SRO analysis architecture options
  - Event-based processing from FPGA
  - Time-windowing at singles or geometry processor
  - Potential for time-windowing in the FPGA
  - Updated diagram for one potential architecture
    - All time-interleaving in a single actor option



- Finalized ERSAP-based software development
  - Completed GitLab CD/CI implementation
  - Finished converting KMax singles and geometry processors into ERSAP actors

SUMMARY

- We are on track to meeting deliverable goals
  - SRO platform development is proven, under iterative refinement
  - Detector front-end design work is underway, finishing up the details now
  - Sub-contracted imaging studies are on track for FY26
  - Talks at conferences are being planed