DG CIRCUITS
ASICs for Radiation Detectors

Prospects for SoLID Front-End ASICs

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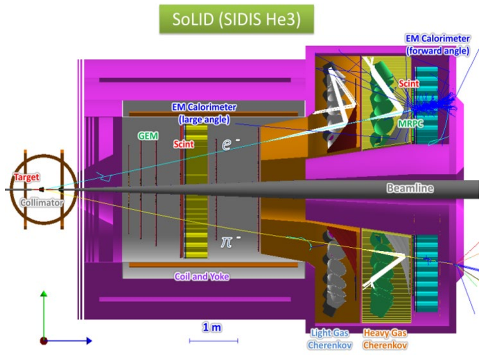
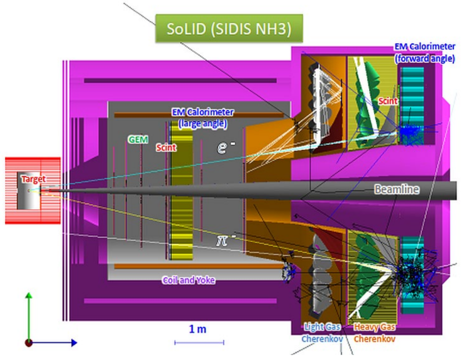
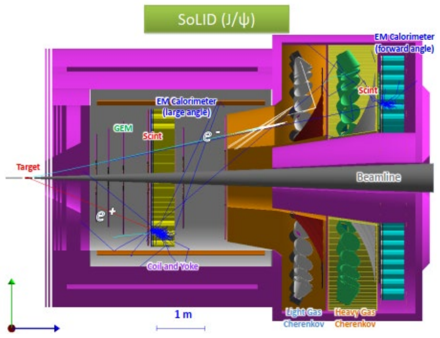
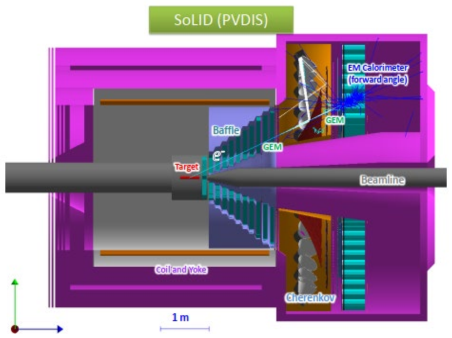
SoLID from a Front-End Electronics Perspective









SoLID configurations will make large use of micro-pattern gas detectors (MPGDs) operating at **very high luminosity**:

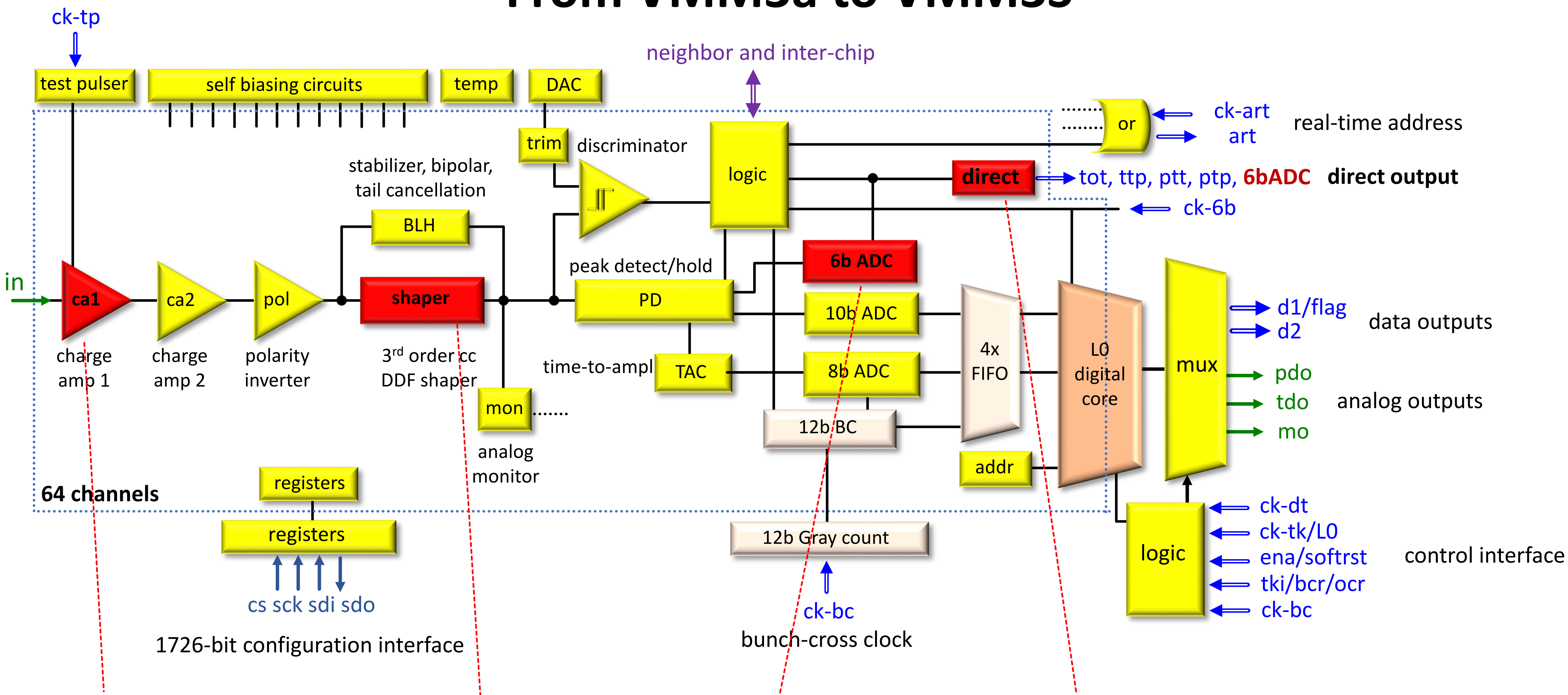
- very few valid hits (physics) merged in a continuous ~10MHz background
- valid hit rate per channel << 0.1 on average (peak-case 30%/ASIC)
- level-1 trigger rate ~25-300kHz
- charge collection time ~20ns, plus low-impact ion-tail >800ns
- charge resolution to preserve S/N>10-20 (full-range ~10-30fC or 60-180k electrons)

Objective of this Work

Evaluate ASIC architectures capable of coping with SoLID high-luminosity environment

- analog front-end requirements and specifications
- optimized ASIC readout architectures
- ASIC design timeline

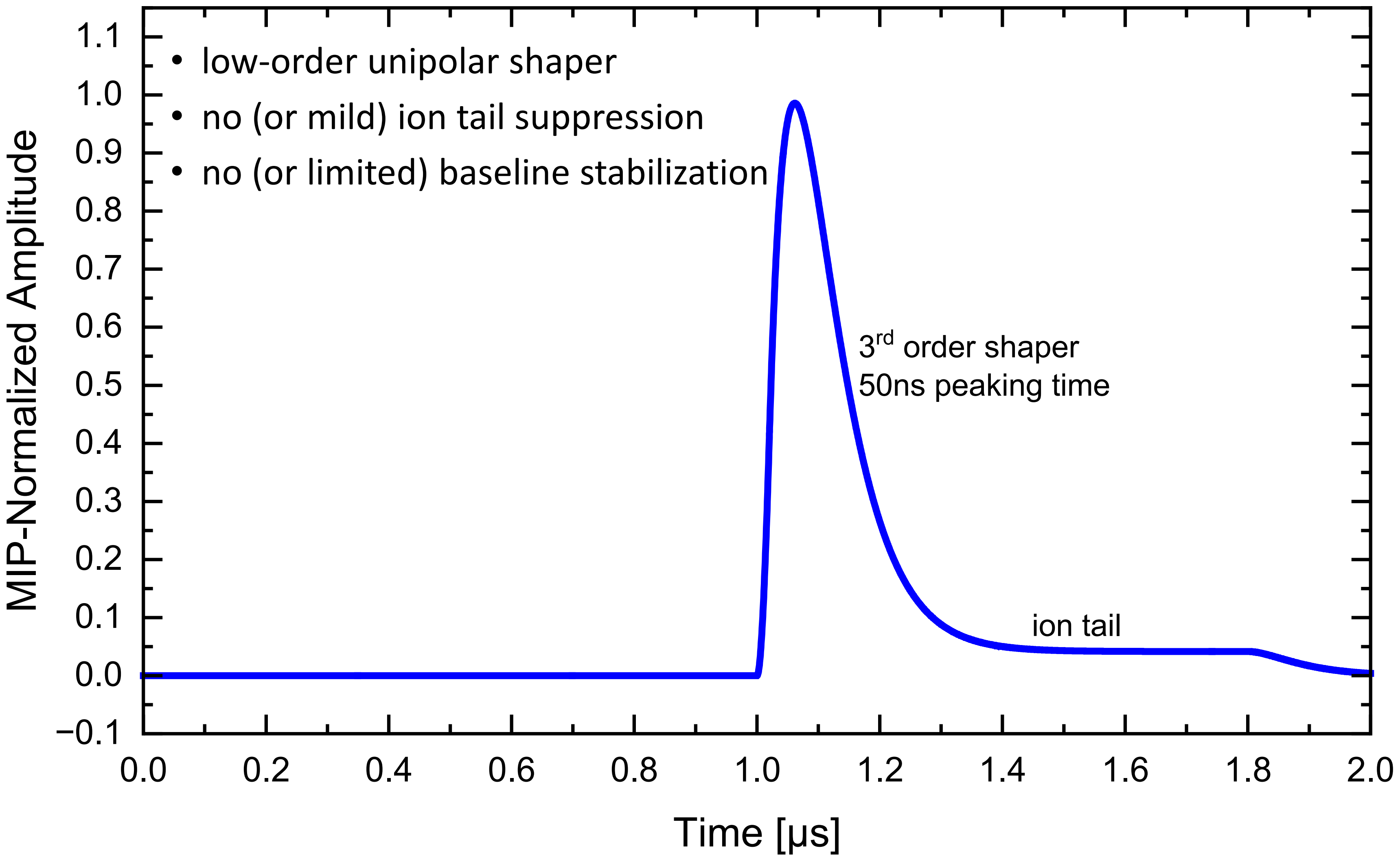
From VMM3a to VMM3S



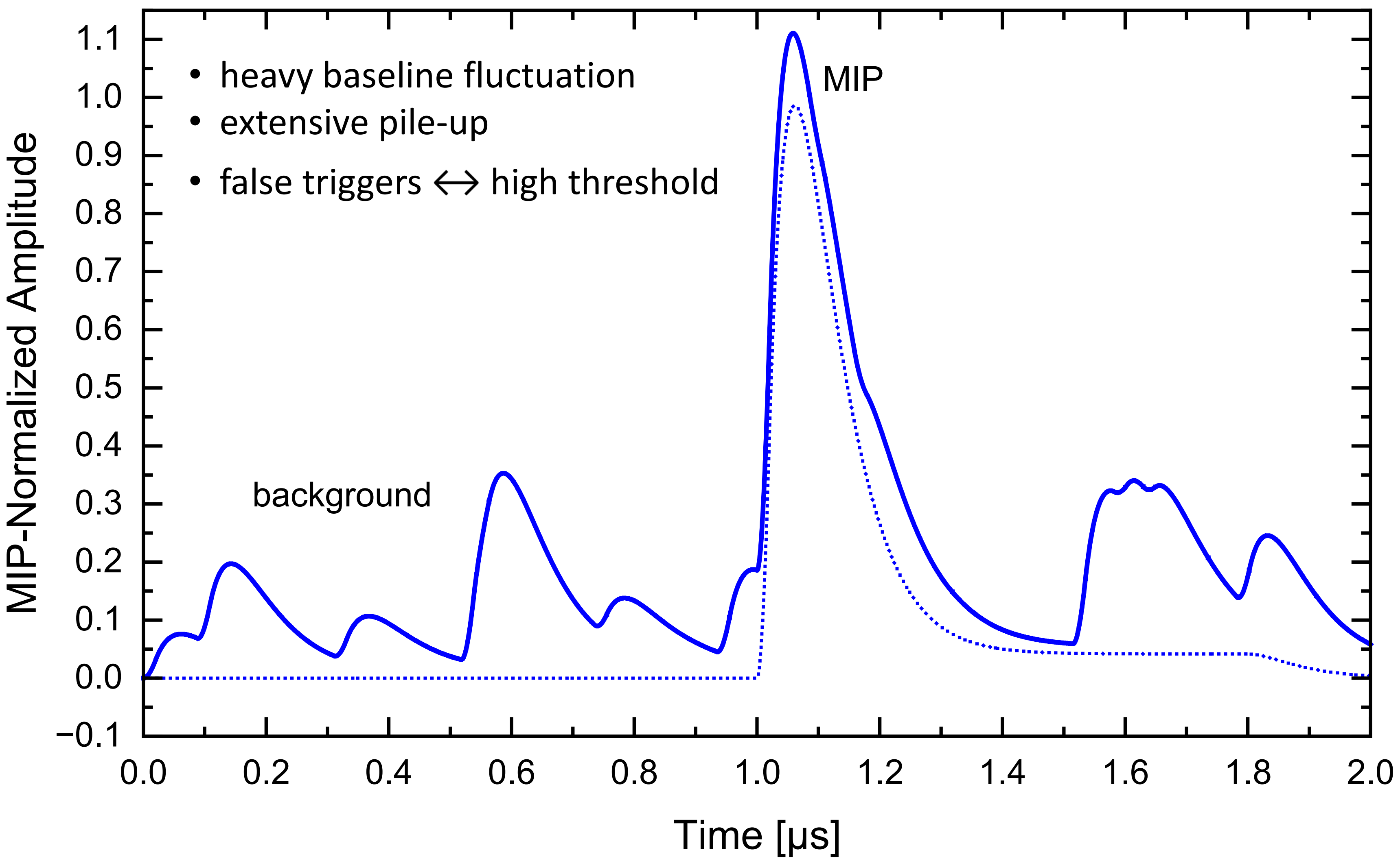
higher gain 64mV/fC **5th order cc** **~35ns conversion time** **~ 20ns readout time**

will deliver ENC ~1,500e^{-} @ 50pF, 25ns (6-bit ADC contribution ~450e^{-})

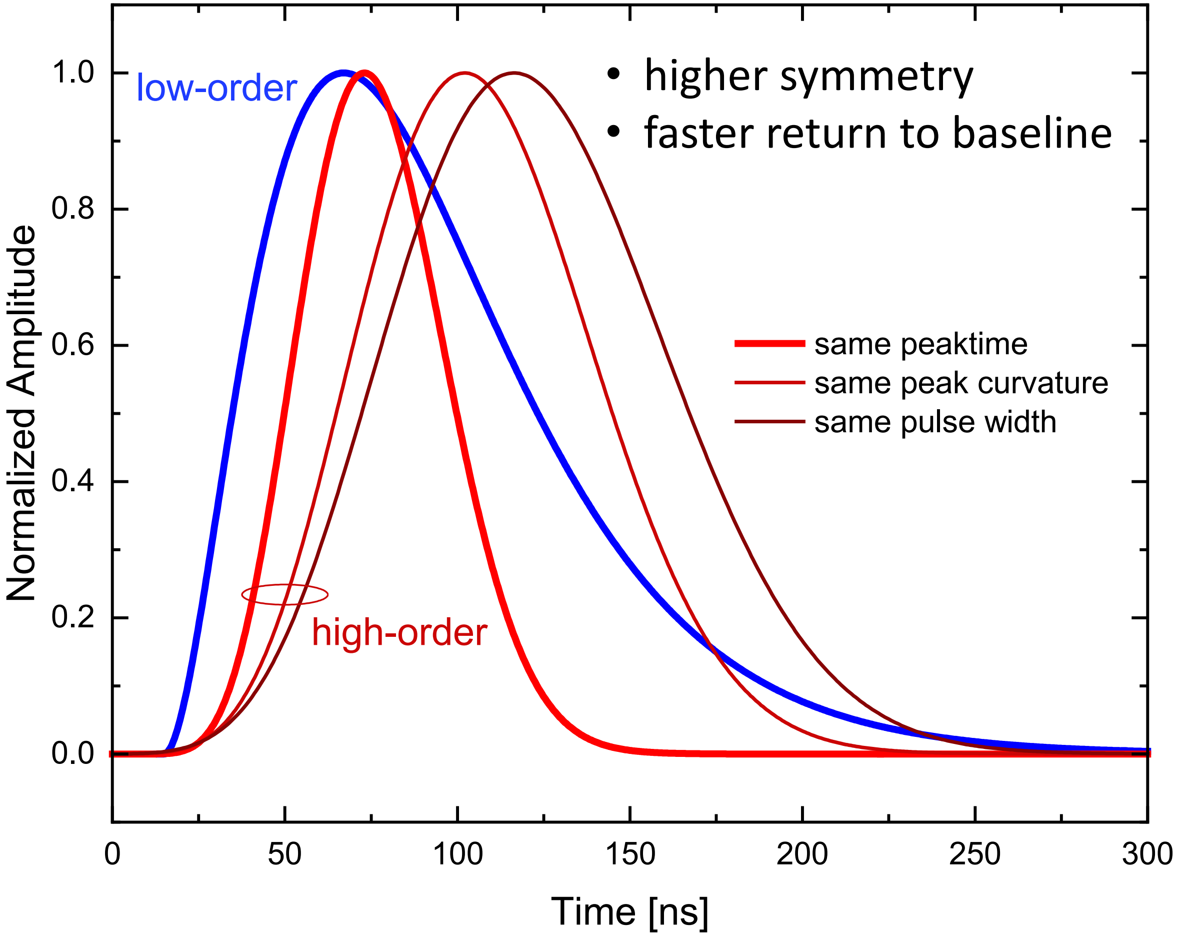
Low-Order Shaping (Off-The-Shelf ASICs)

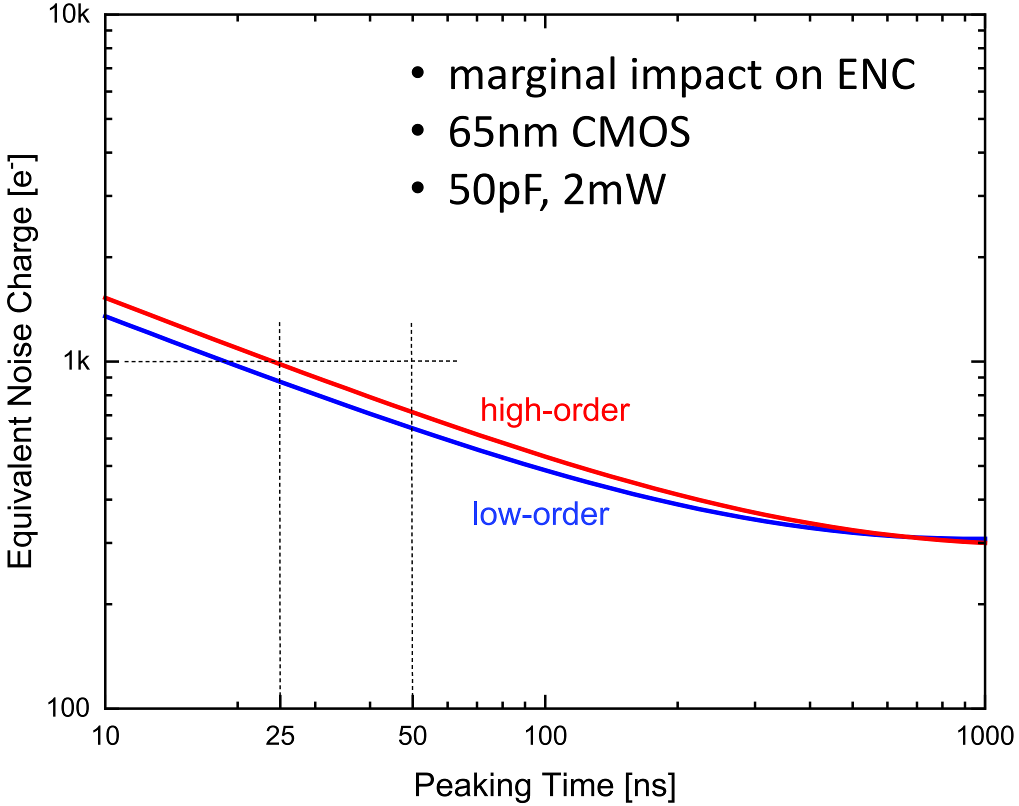


Low-Order Shaping in SoLID



High-Order Shaping

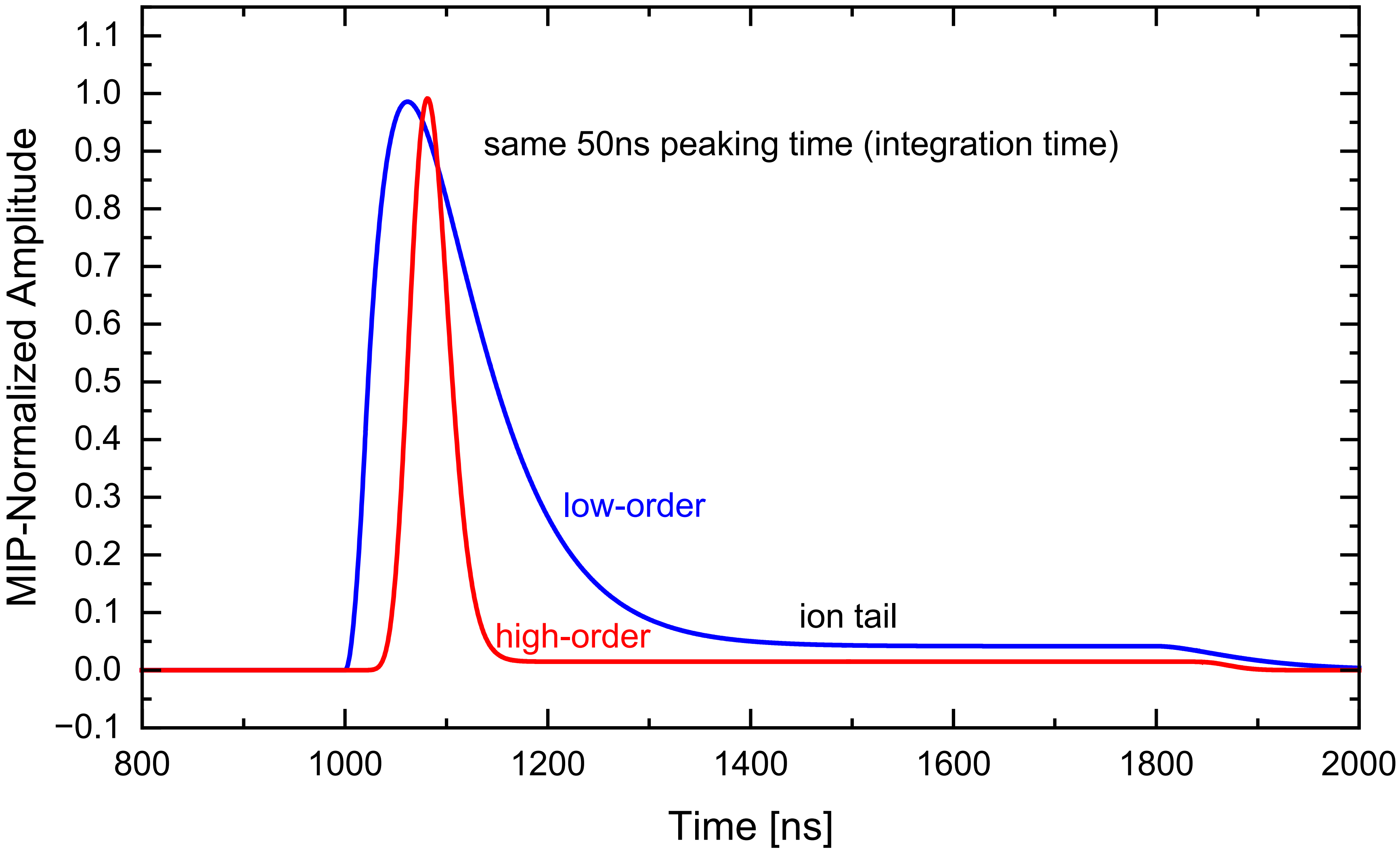




- At equal rise time (peaking time) → comparable ENC, higher ballistic deficit, much lower pile-up
- At equal ballistic deficit (peak curvature) → lower ENC, lower pile-up
- At equal pile-up (pulse width) → much lower ENC, lower ballistic deficit

see: IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 54, NO. 2, APRIL 2007

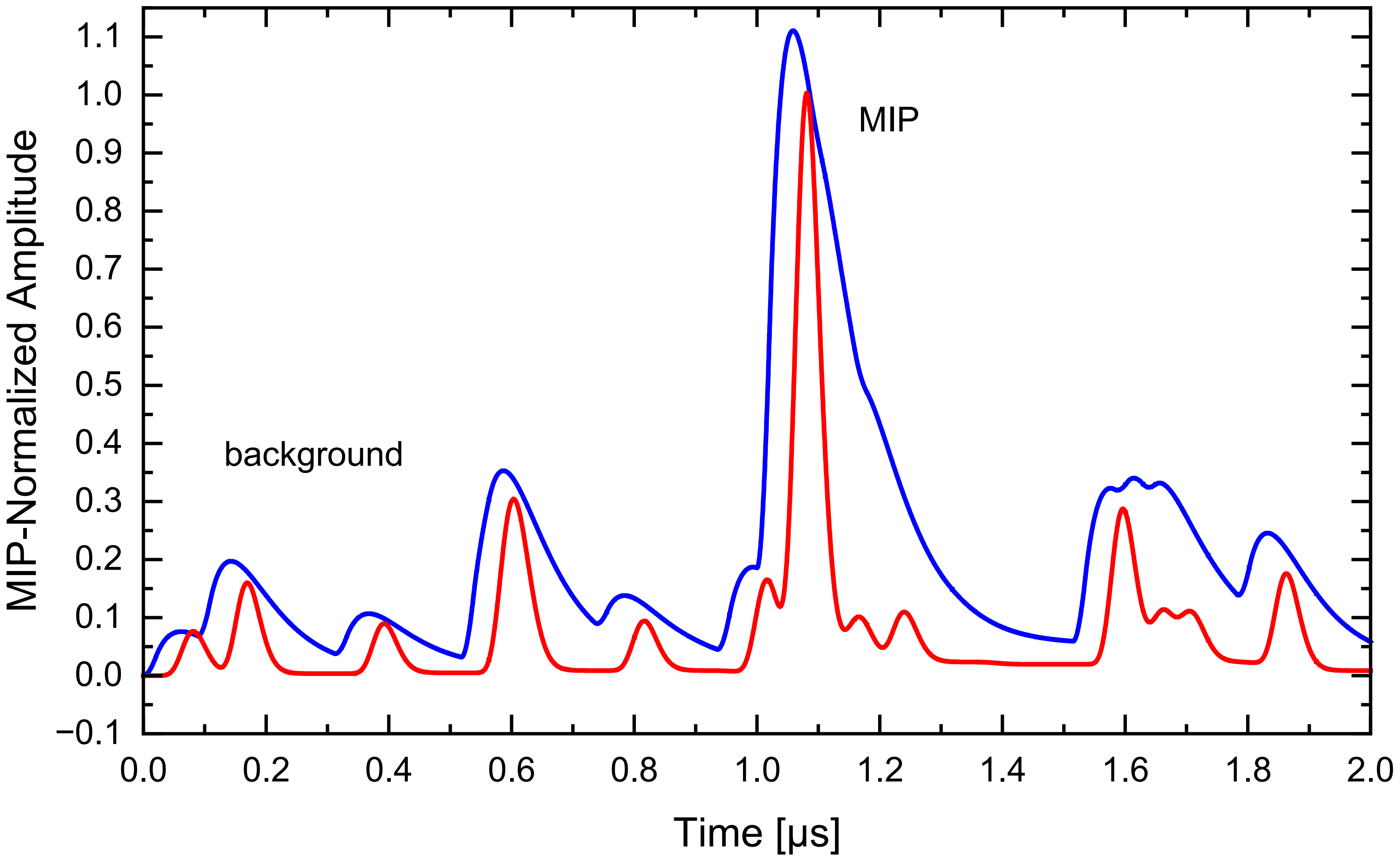
High-Order Applied to MPGD Signals



→ Better separation between electrons and ion-tail contributions

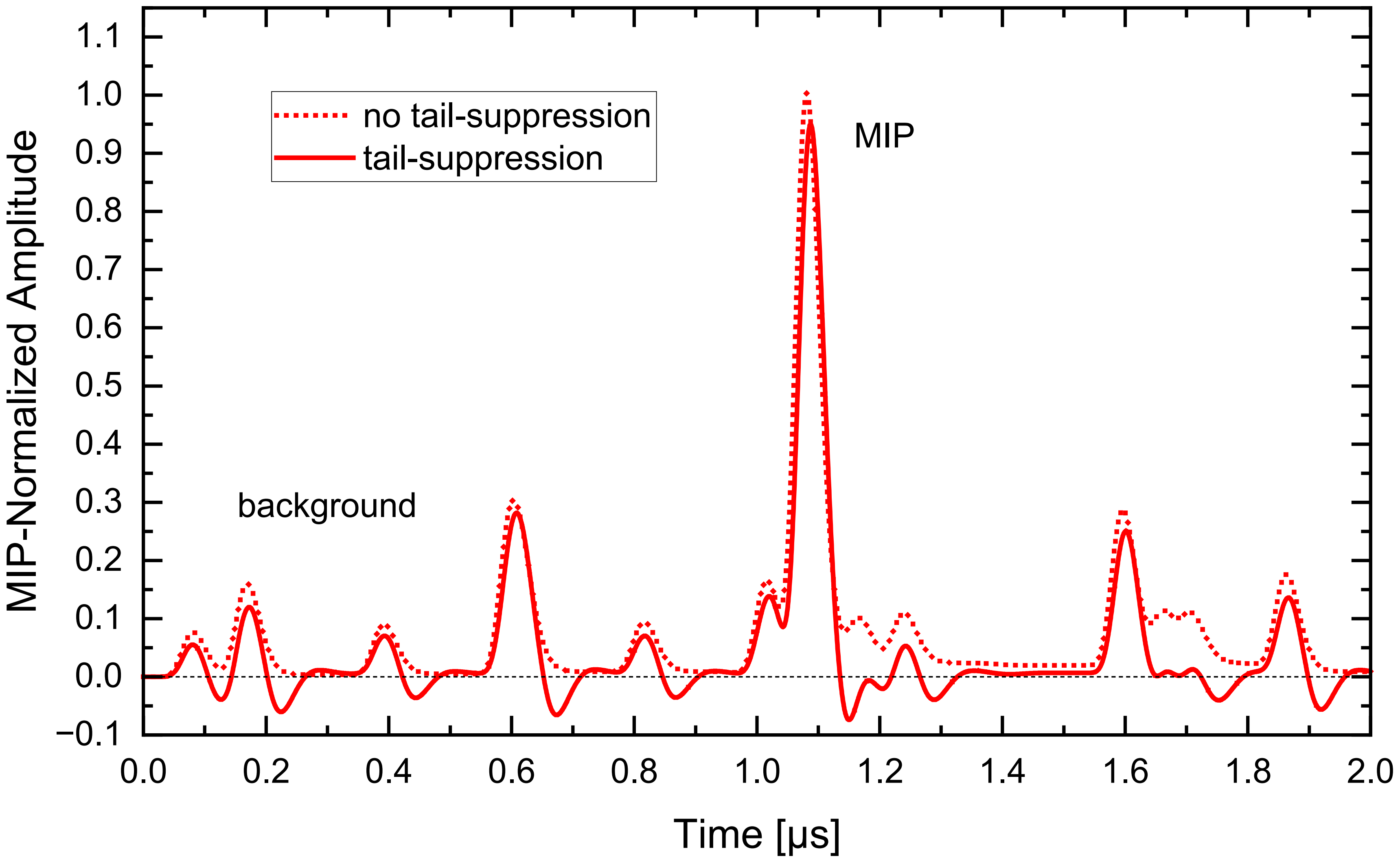
→ Programmable peaking time for optimal ballistic-deficit ↔ pile-up trade-off

High-Order Impact in Presence of High Background



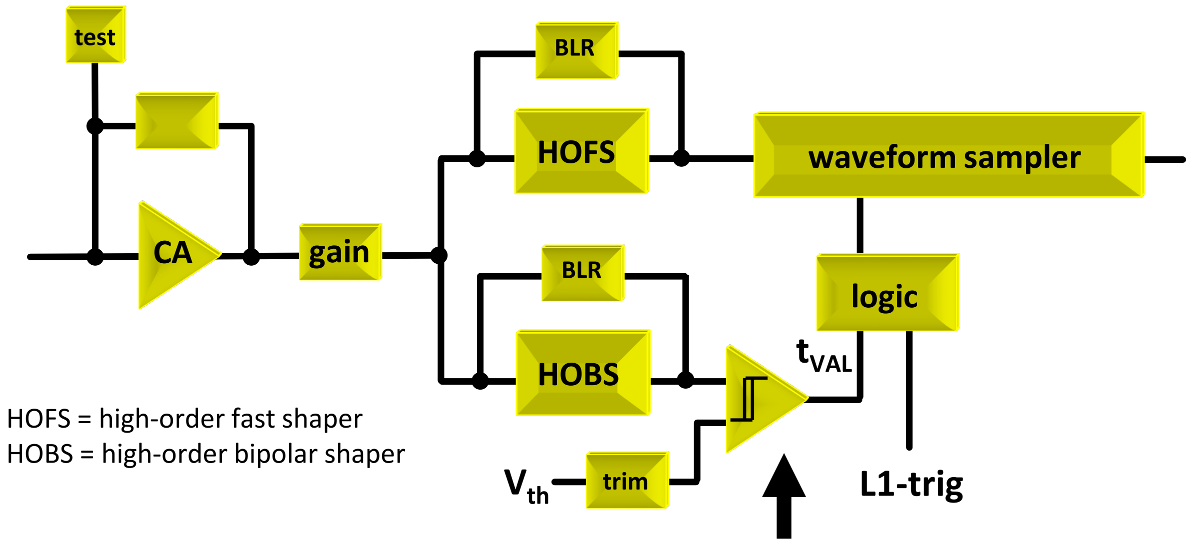
→ Higher event-peak isolation with marginal increase in ENC

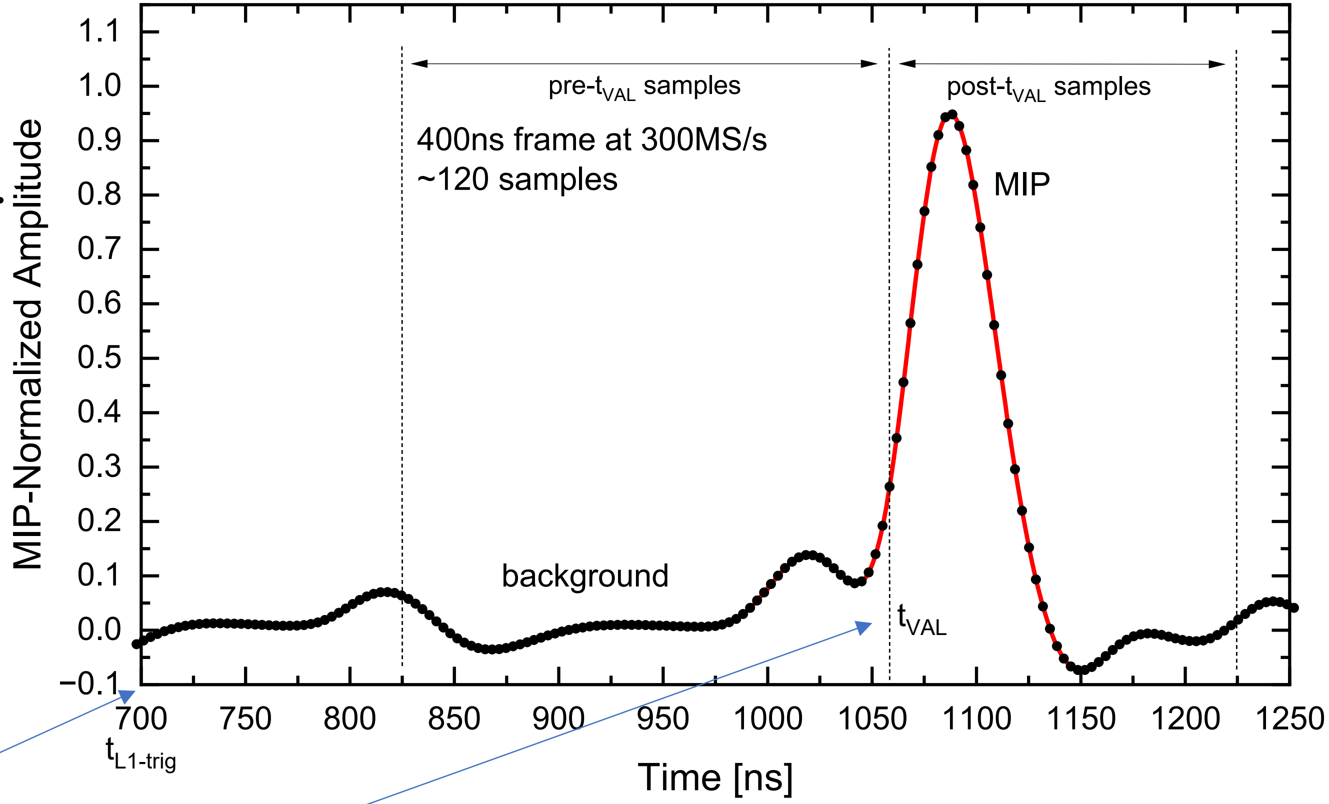
Ion Tail Suppression (Baseline Restoration)

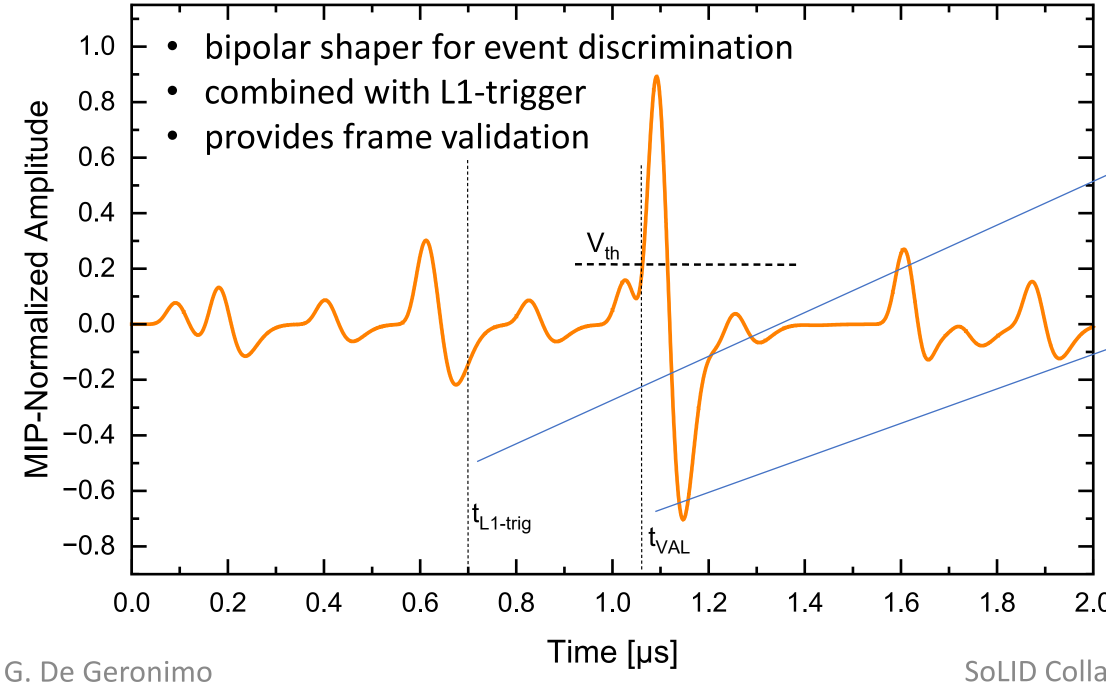


→ Optional tail suppression for strong baseline stabilization

Fast Sampling Channel Architecture

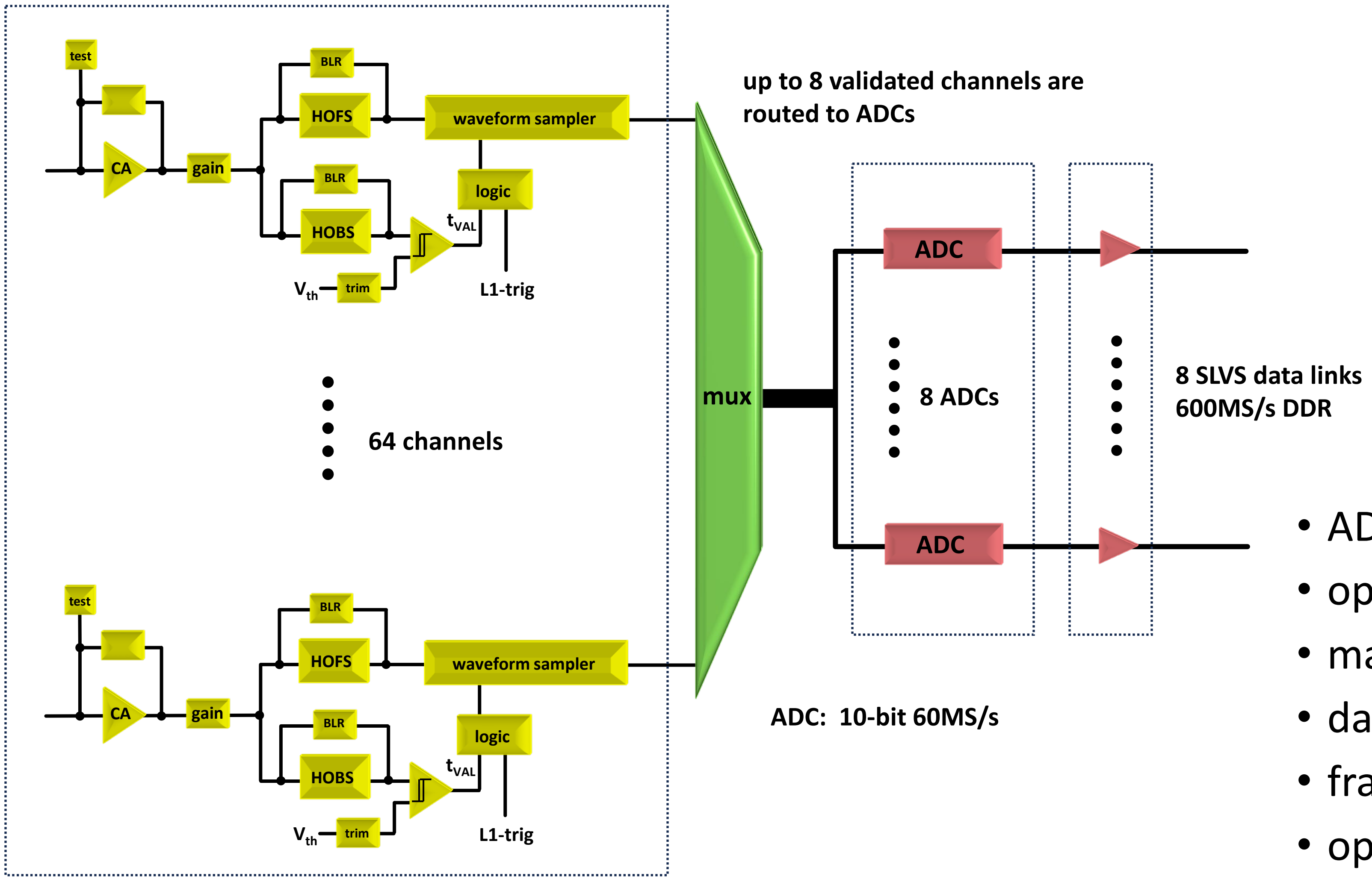






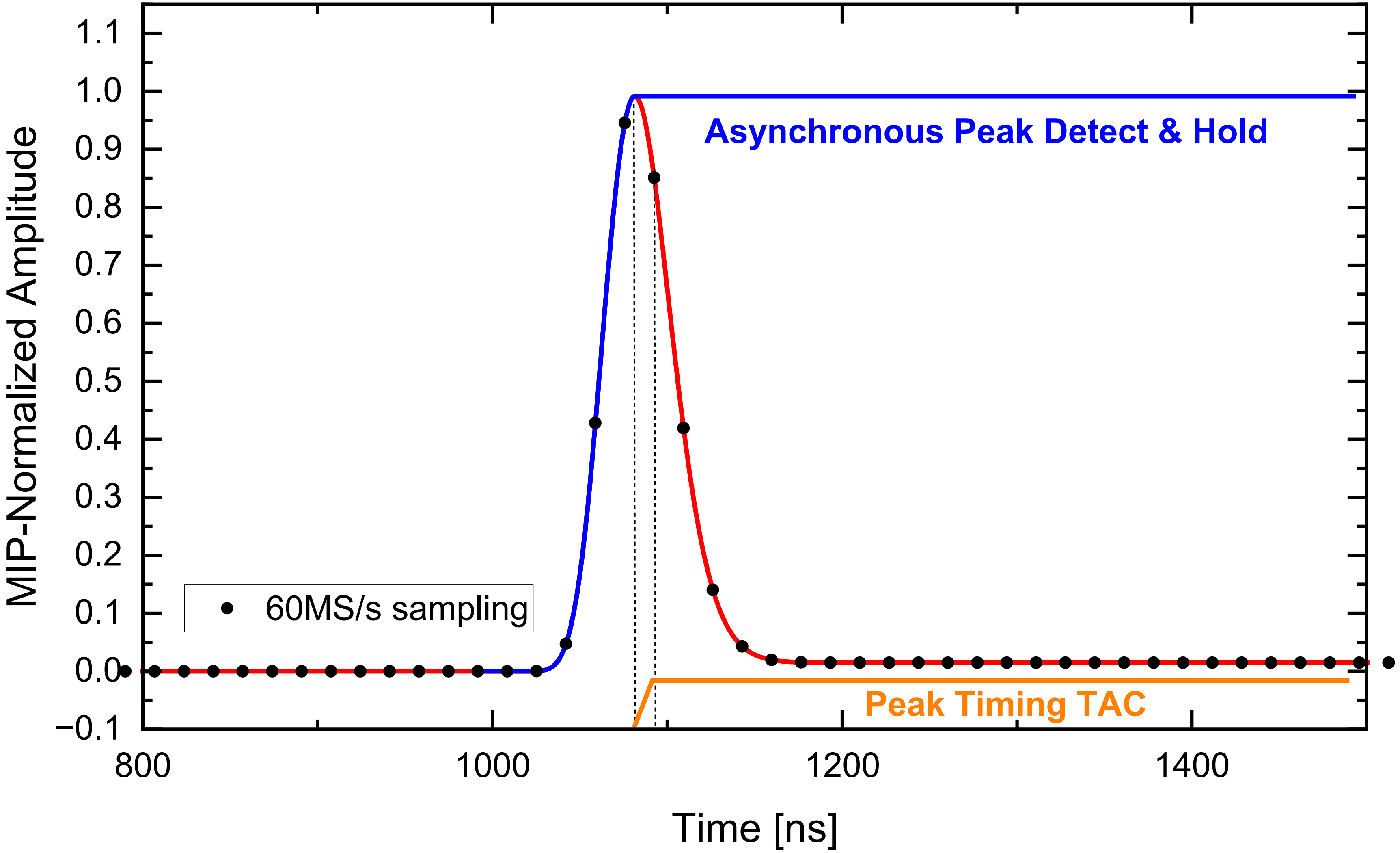
- ~ 400ns frame at 300MS/s (Nyquist)
- up to 120 samples
- programmable number of pre- and post-t_{VAL} samples
- option to collect sub-threshold neighbors

Fast Sampling ASIC Readout Architecture



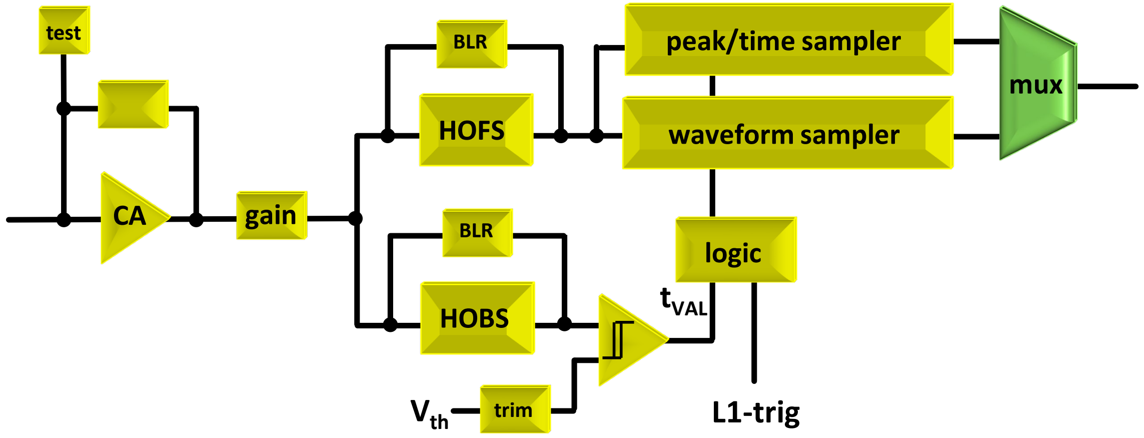
- ADC/readout of validated frames only
- option of subthreshold neighbors
- maximum 8 frames per L1-trigger
- data conversion + readout ~ 2µs
- frame rates up to ~ 400 kHz
- optimized analog front-end
- **high resolution**
- **power-efficient (~6-7mW/ch)**

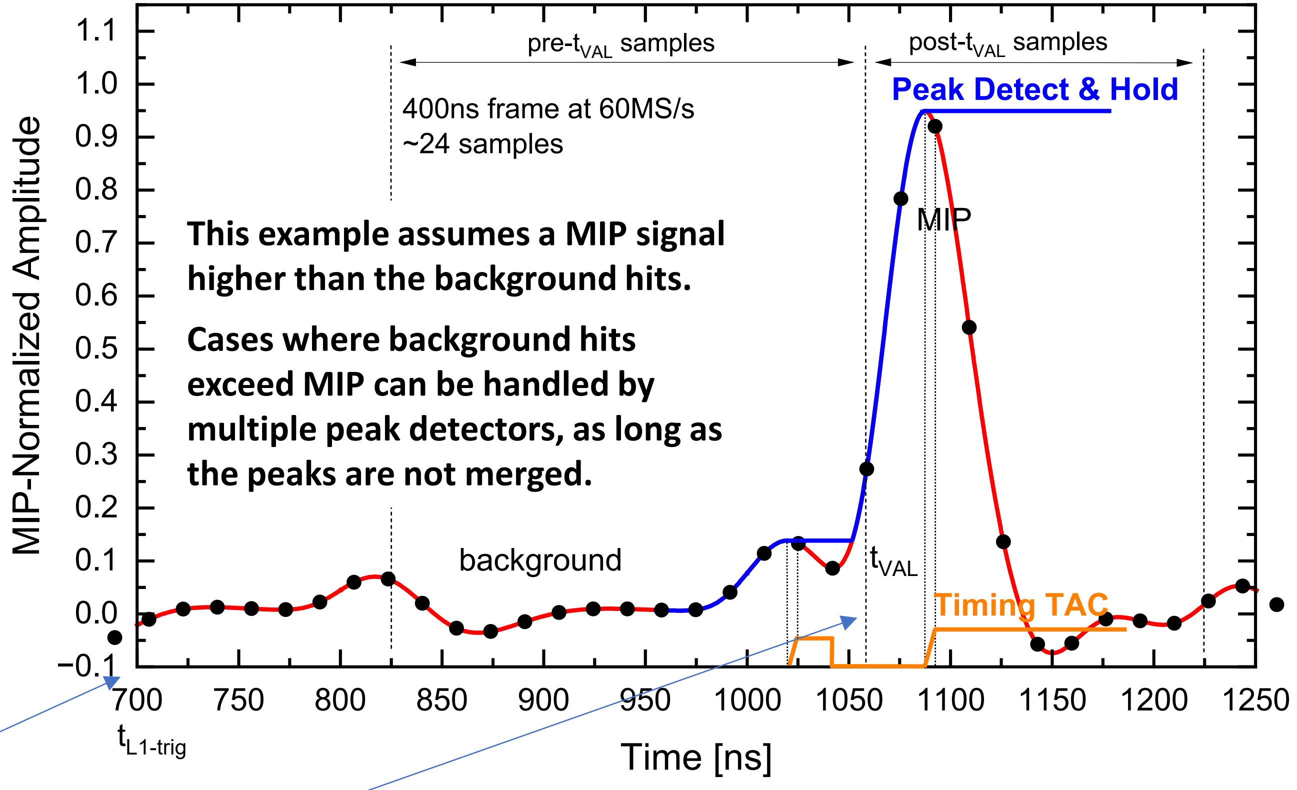
Optional or Alternative: Peak/Time Detection

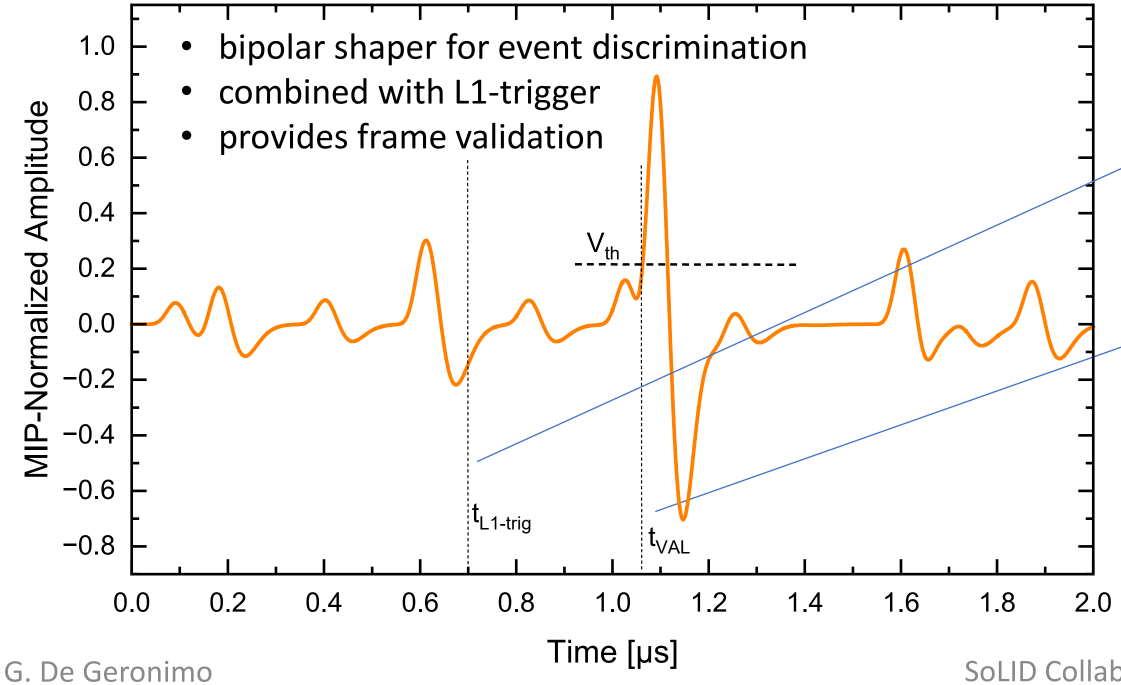


→ Combines slower waveform sampling with peak/time detection for more efficient data generation

Peak-Detect & Sampling Channel Architecture

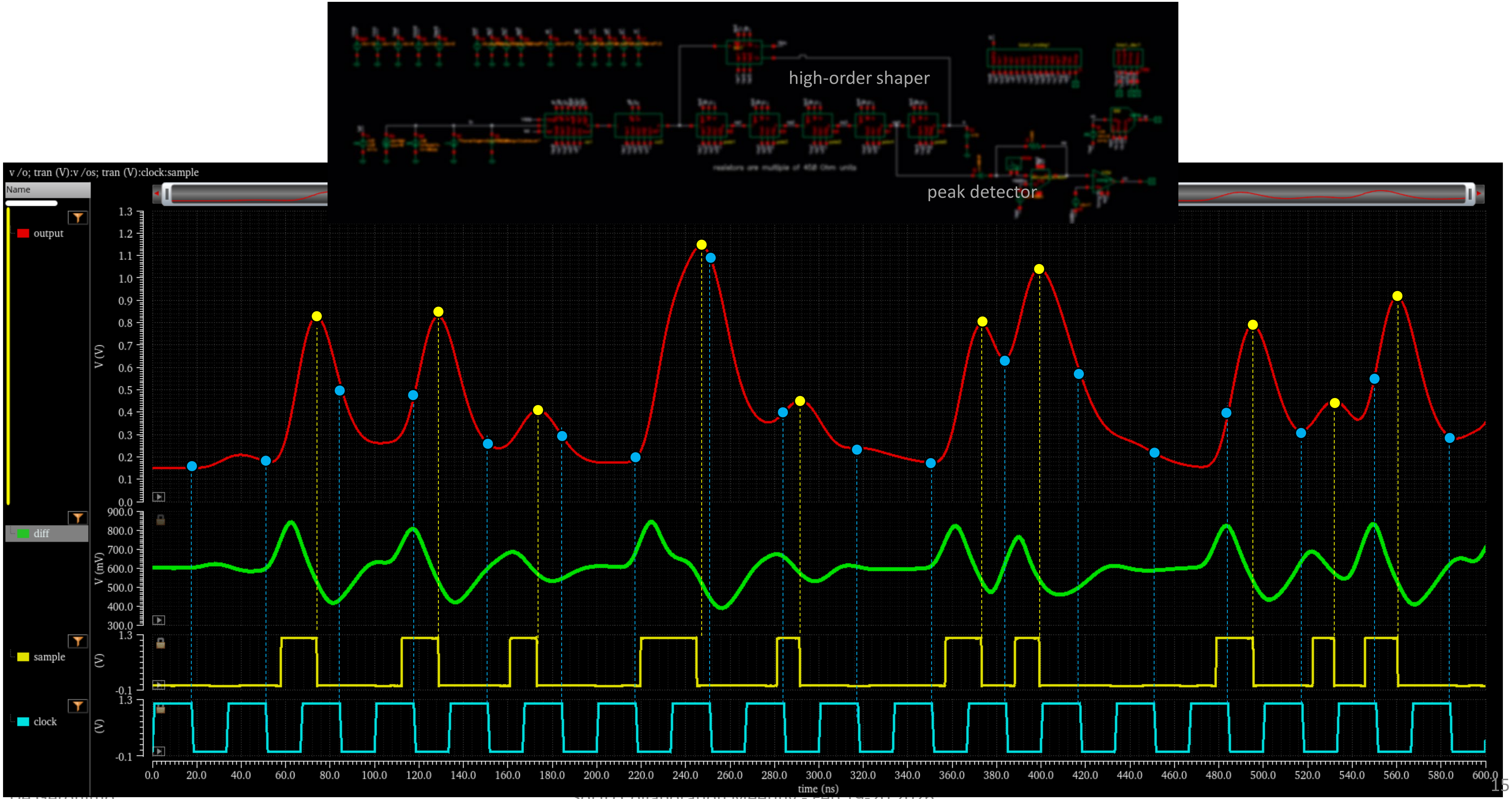




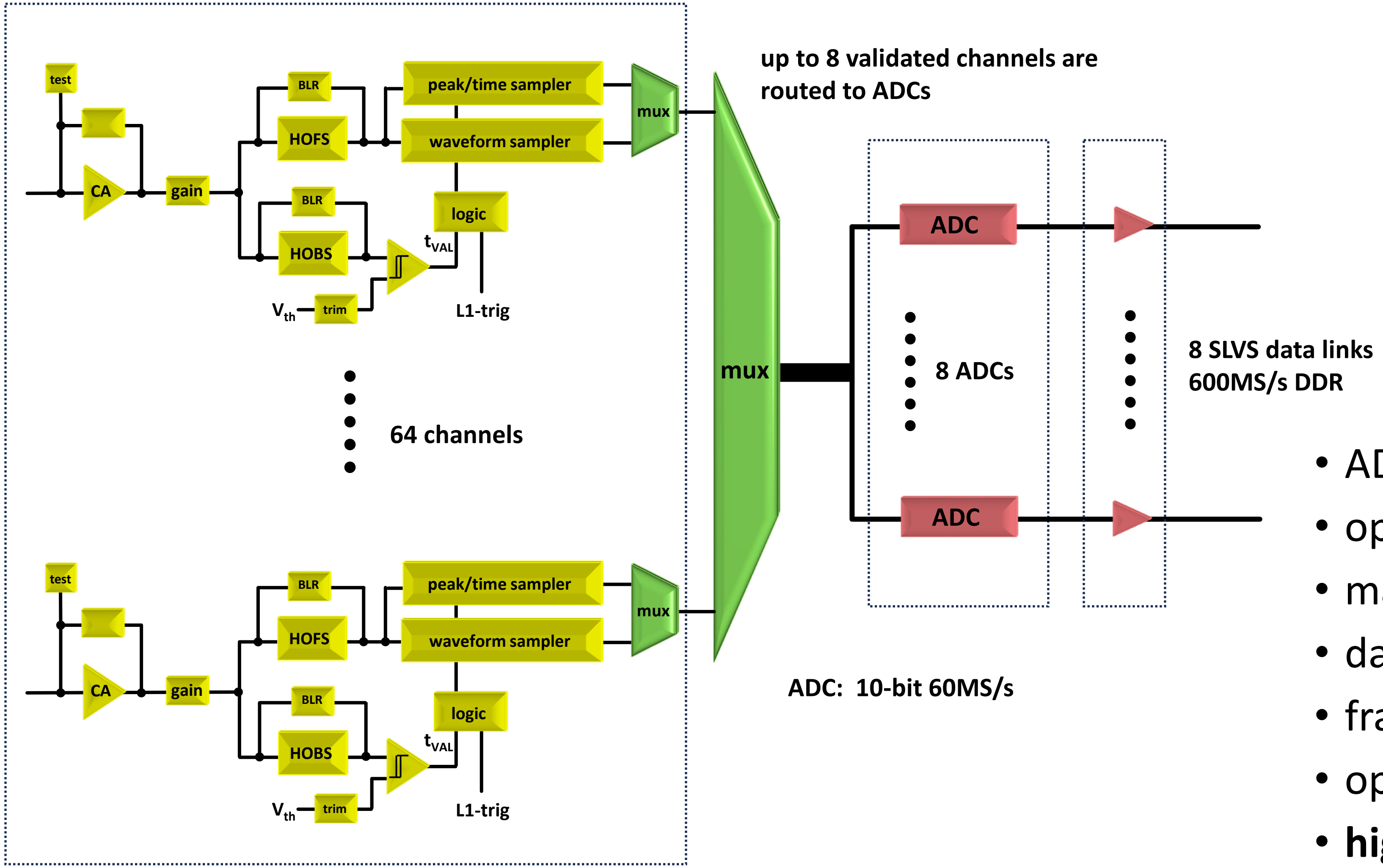


- ~ 400ns frame at 60MS/s plus peak/time detection
- sampling rate satisfies our case of defined shapes
- up to 24 samples
- programmable number of pre- and post-t_{VAL} samples
- option to collect sub-threshold neighbors

Actual Transistor-Level CMOS Simulation



Peak Detect & Sampling ASIC Readout Architecture



- ADC & readout of validated frames
- option of subthreshold neighbors
- maximum 8 frames per L1-trigger
- data conversion + readout ~ 400ns
- frame rates ~ 1.25 MHz
- optimized analog front-end
- **high resolution**
- **power-efficient (~4-5mW/ch)**
- **data-efficient**

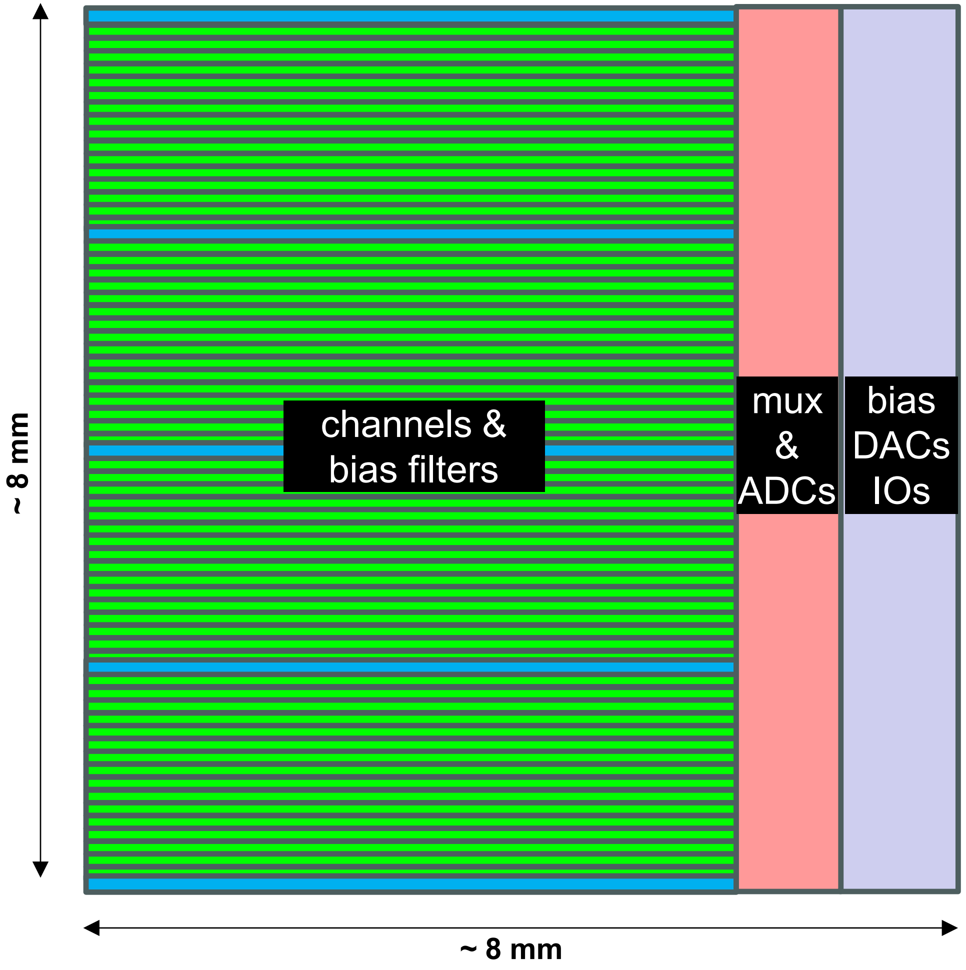
Two ASIC Architecture Options for SoLID

Parameter	Fast Waveform Sampling (300 MS/s)	Peak/Time Detection (60 MS/s)
Samples per validated frame	~120	8–24 (or fewer)
Max frame rate	~400 kHz	> 1.25 MHz
Data volume per hit	High	Very low (data-efficient)
Power per channel	Higher	Lower (<5 mW/ch target)
Pile-up handling	Excellent (full waveform)	Very good + peak dominance
Complexity	Slightly higher	Moderate
Best for	Highest-rate / complex pile-up	Balanced high-rate operation

→ Both architectures can be integrated in the same ASIC

Technology, Floorplan, Design Time

- Largely based on proven CMOS architectures
- Estimated die size: die size ~ 8x8 mm²
- Technology TSMC 65nm 1.2V
- First prototype design time ~ 12-14 months
- Fabrication time ~ 10-12 weeks
- BGA packaging ~4-6 weeks
- DSP core can be integrated after FPGA validation



Summary

Primary path: SoLID-specific ASIC architecture

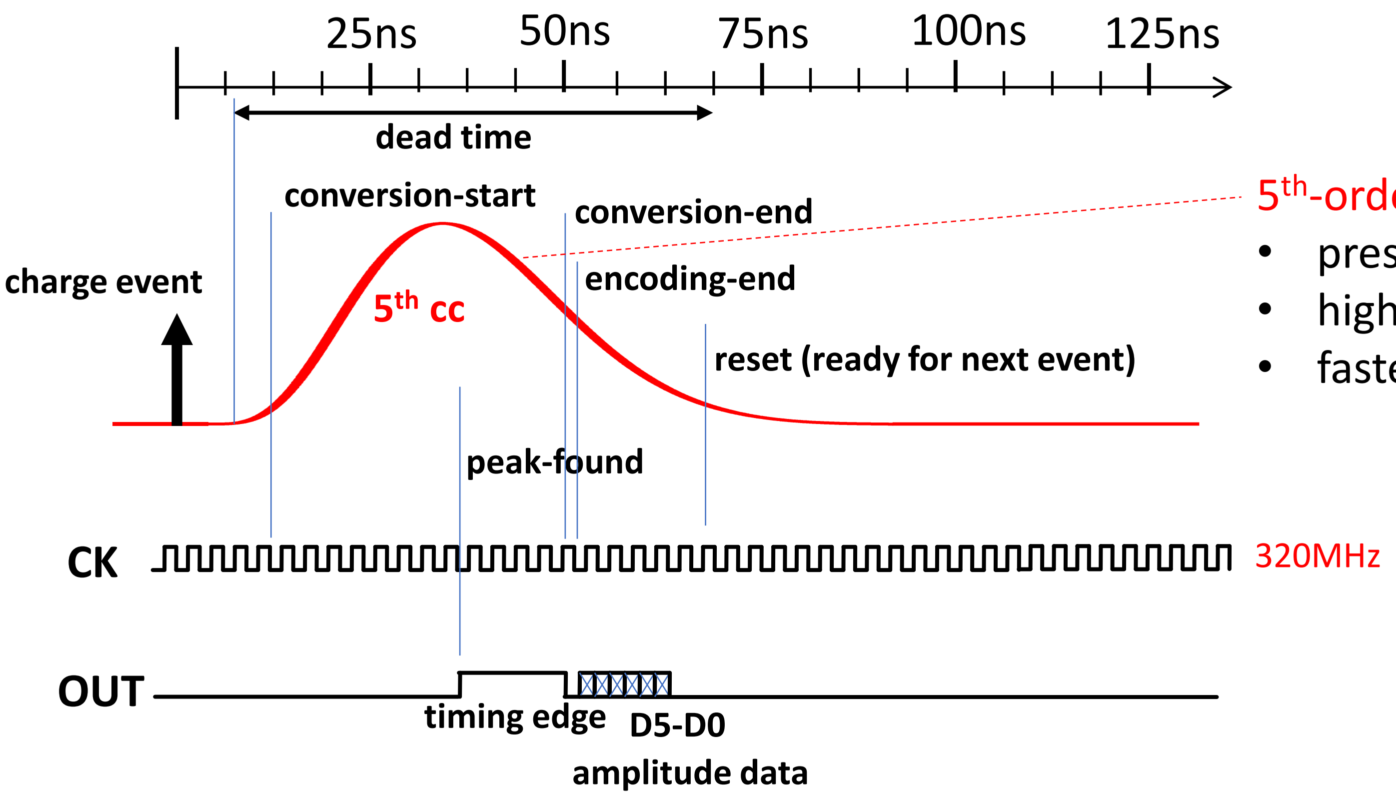
- Specific for high-luminosity high-background
- Very low-noise charge amplifier with programmable gain
- Very high-order shaper with programmable peaking time
- Programmable baseline restoration for high stability
- Dedicated sub-channel for discrimination
- Power-efficient high-rate (Nyquist) waveform sampling
- or Power/Data efficient moderate-rate sampling plus peak/time detection
- **Final architecture selected after detailed detector-CMOS co-simulations**
- Frame rate capability > 1.25 MHz
- ~ 12-14 months design (first prototype)
- Will advance state-of-the-art in ASICs for MPGDs

Fast-track option: VMM3S

- Improved gain/rate capability, peak detect only
- ~ 5-6 months design total

Backup Slides

6-Bit Direct Output in VMM3S

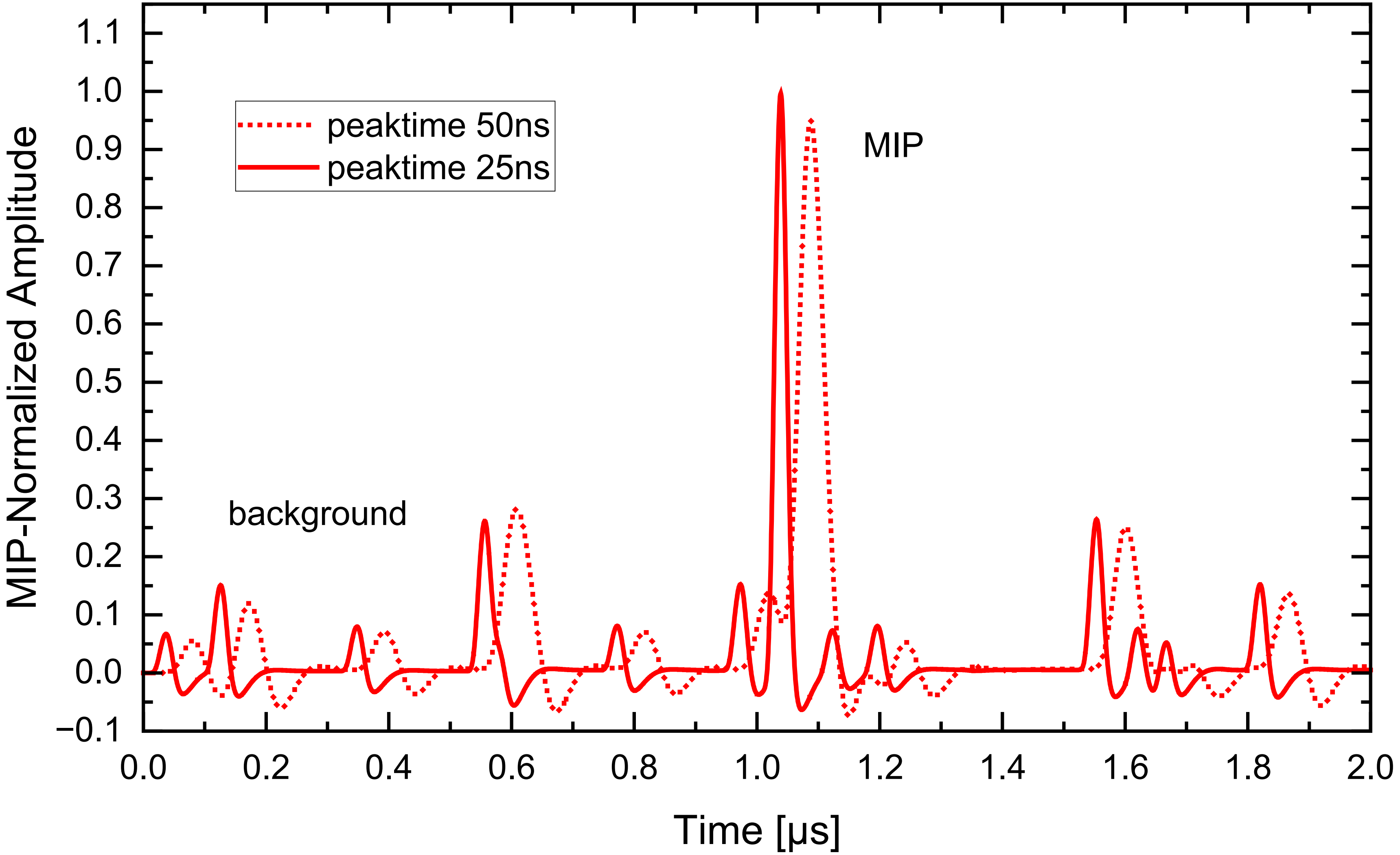


5th-order cc shaper

- preserves charge resolution
- higher symmetry
- faster return to baseline

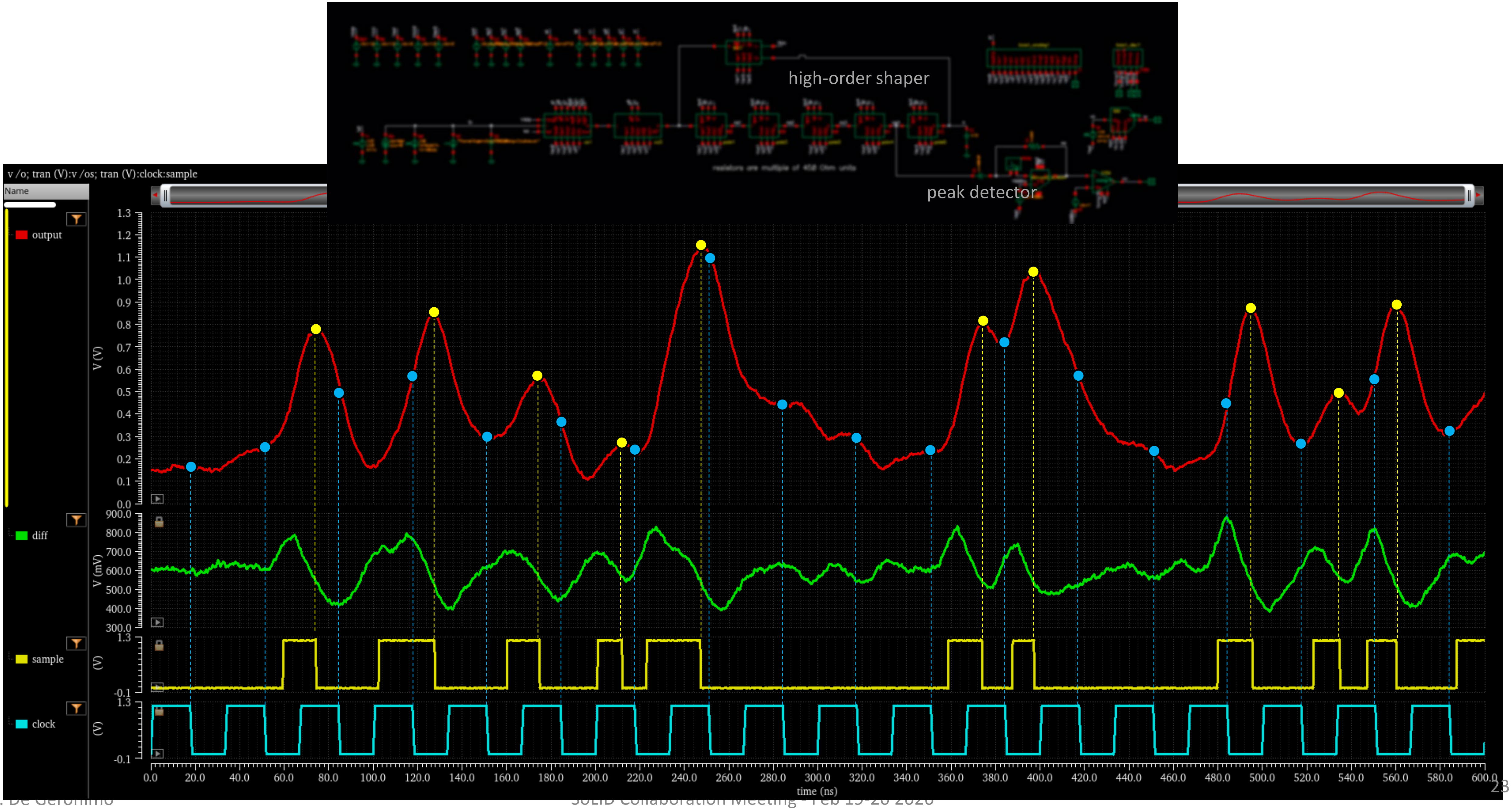
- ADC conversion time ~ 35ns
- Dead time per event ~ **60ns** (~30% improvement vs VMM3a)
- D5-D0 shifted at 320MHz DDR in SLVS
- Estimated power increase ~500µW/channel

Programmable peaking time

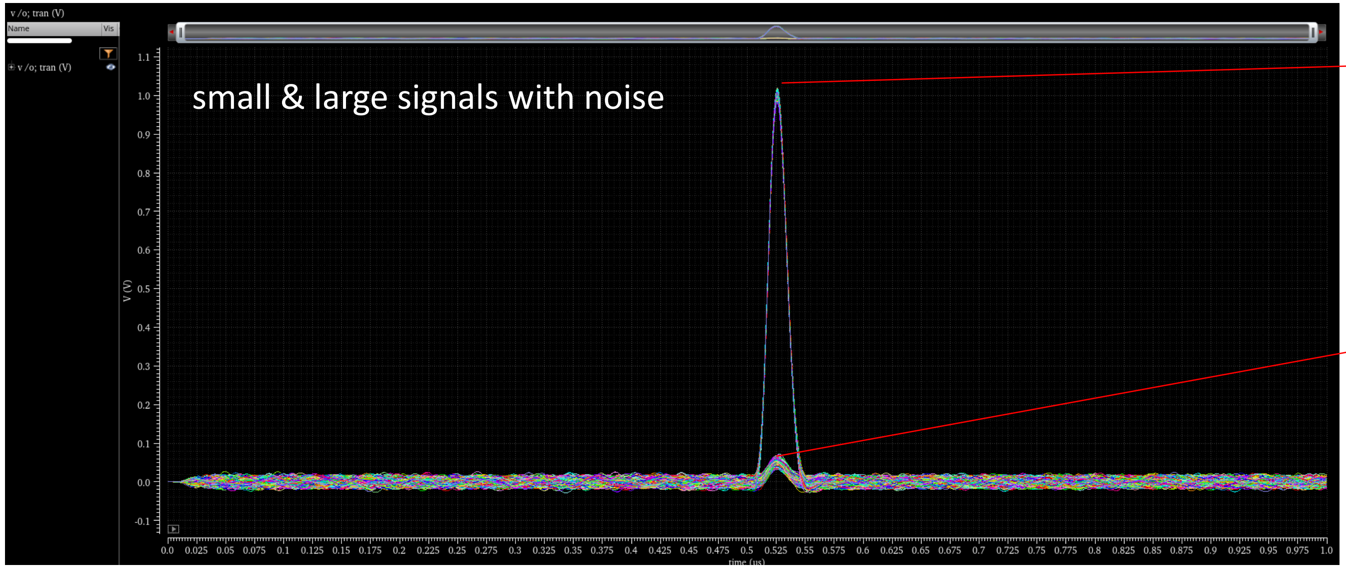


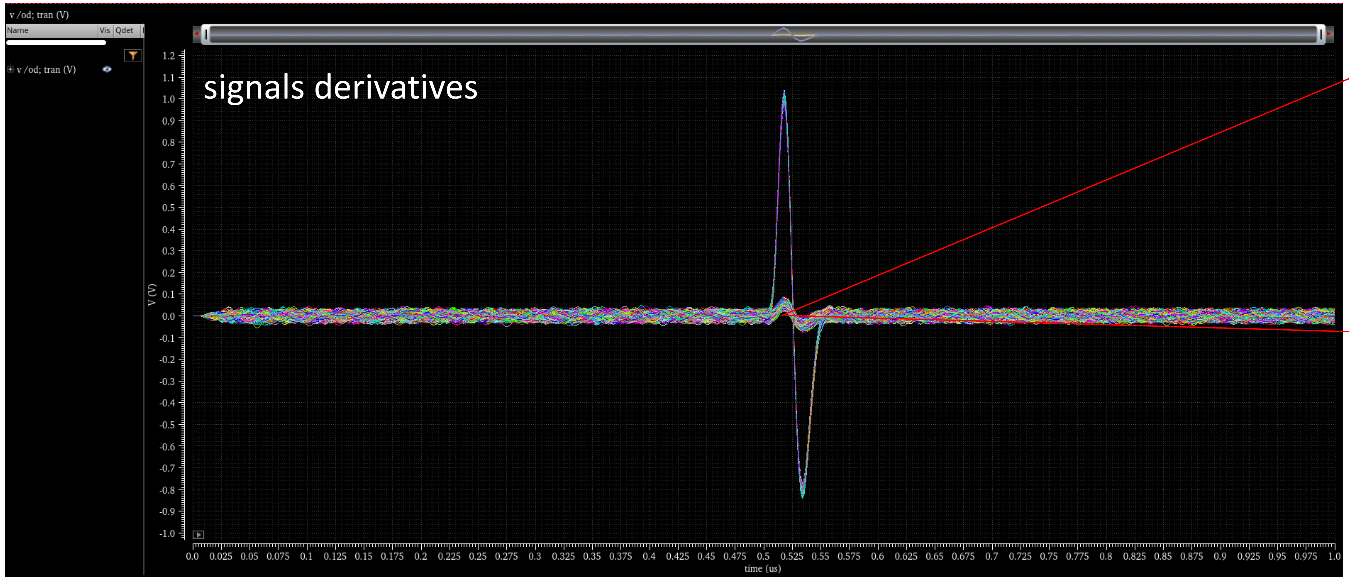
→ **Detailed detector-CMOS co-simulations will determine available peaktime selection**

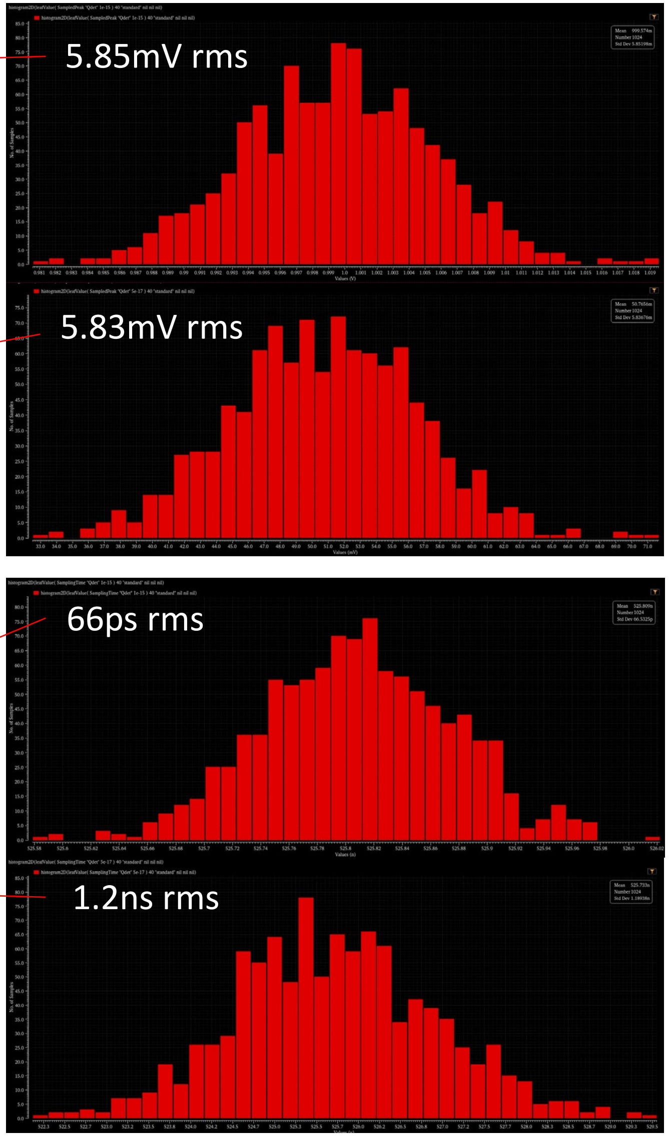
Actual Transistor-Level CMOS Simulation with Transient Noise



Peak Detection for Streaming: Noise







The timing follows the peak: this peak-sampling technique **does not add noise**!